RELIABILITY REPORT

FOR

MAX809LEUR+T

PLASTIC ENCAPSULATED DEVICES

April 28, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
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Conclusion

The MAX809LEUR+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX803/MAX809/MAX810 are microprocessor (µP) supervisory circuits used to monitor the power supplies in µP and digital systems. They provide excellent circuit reliability and low cost by eliminating external components and adjustments when used with +5V, +3.3V, +3.0V, or +2.5V powered circuits. These circuits perform a single function: they assert a reset signal whenever the VCC supply voltage declines below a preset threshold, keeping it asserted for at least 140ms after VCC has risen above the reset threshold. Reset thresholds suitable for operation with a variety of supply voltages are available. The MAX803 has an open-drain output stage, while the MAX809/MAX810 have push-pull outputs. The MAX803's open-drain active-low RESET output requires a pullup resistor that can be connected to a voltage higher than VCC. The MAX803/MAX809 have an active-low RESET output, while the MAX810 has an active-high RESET output. The reset comparator is designed to ignore fast transients on VCC, and the outputs are guaranteed to be in the correct logic state for VCC down to 1V. Low supply current makes the MAX803/MAX809/MAX810 ideal for use in portable equipment. The MAX803 is available in a 3-pin SC70 package, and the MAX809/MAX810 are available in 3-pin SC70 or SOT23 packages.

II. Manufacturing Information

A. Description/Function:	3-Pin Microprocessor Reset Circuits
B. Process:	B3
C. Number of Device Transistors:	300
D. Fabrication Location:	Oregon
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	Pre 1997

III. Packaging Information

A. Package Type:	3-pin SOT23
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-1701-0199
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Jb:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	336°C/W
M. Multi Layer Theta Jc:	110.1°C/W

IV. Die Information

A. Dimensions:	31X44 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	3.0 microns (as drawn)
F. Minimum Metal Spacing:	3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 4340 \times 155 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 1.36 \times 10^{-9}$

$\lambda = 1.36$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the B3 Process results in a FIT Rate of 0.25 @ 25C and 4.22 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (ESD lot NRHAD30A4F D/C 0811, Latch-Up lot IRHACQ001H D/C 9948)

The PW54 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX809LEUR+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	75	0	NRHBB2199C, D/C 0418
	Biased	& functionality	80	0	NRHABA980K, D/C 0240
	Time = 1000 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.