RELIABILITY REPORT

FOR

MAX8559ExAxx

PLASTIC ENCAPSULATED/CHIP SCALE DEVICES

10/27/08

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX8559 sucessfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX8559 dual, low-noise, low-dropout (LDO) linear regulator operates from a 2.5V to 6.5V input voltage and delivers at least 300mA of continuous output current. It offers low output noise and low dropout of only 60mV at 100mA. Typical output noise for this device is 32μV_{RMS}, and PSRR is 70dB at 10kHz. Designed with an internal p-channel MOSFET pass transistor, the MAX8559 maintains a low 115µA supply current per LDO, independent of the load current and dropout voltage. Other features include short-circuit protection and thermal-shutdown protection. The MAX8559 includes two independent logic-controlled shutdown inputs and is capable of operating without a bypass capacitor to further reduce total solution size. The MAX8559 is available in a miniature 8-bump UCSP™ (2mm x 1mm) or 8-pin TDFN (3mm x 3mm) package

B. Absolute Maximum Ratings

Item	Rating
INA, INB, SHDNA, SHDNB, BP to GND	-0.3V to +7V
INA to INB	-0.3V to +0.3V
OUTA, OUTB to GND	-0.3V to (VIN + 0.3V)
Output Short-Circuit Duration	Continuous
Continuous Power Dissipation (TA = +70°C)	
8-Bump UCSP (derate 4.7mW/°C above +70°C)	379mW
8-Pin TDFN (derate 24.4mW/°C above +70°C)	1951mW
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
8-Pin TDFN Lead Temperature (soldering, 10s)	+300°C
8-Bump UCSP Solder Profile	(Note 1)

Note 1: For UCSP solder profile information, please refer to the application note APP_1891 on the Maxim website, www.maxim-ic.com.

II. Manufacturing Information

A. Description/Function: Dual, 300mA, Low-Noise Linear Regulator with Independent Shutdown in UCSP or TDFN

B. Process: B8 (Standard 1.2 micron silicon gate CMOS)

C. Number of Device Transistors: 2359

D. Fabrication Location: Texas, USA

E. Assembly Location: Philippines, Thailand or USA

F. Date of Initial Production: January, 2003\4

III. Packaging Information

A. Package Type:	**8-Lead TDFN**	**8-Bump UCSP**
B. Lead Frame:	Copper	N/A
C. Lead Finish:	Solder Plate or 100% Matte Tin	N/A
D. Die Attach:	Silver-Filled Epoxy	N/A
E. Bondwire:	Gold (1.0 mil dia.)	N/A
F. Mold Material:	Epoxy with silica filler	N/A
G. Assembly Diagram:	# 05-9000-0869	# 05-9000-0870
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1	Level 1

IV. Die Information

A. Dimensions: 80 x 42 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Copper/Silicon

D. Backside Metallization: None

E. Minimum Metal Width: .8 microns (as drawn)

F. Minimum Metal Spacing: .8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Ken Wendel (Director, Reliability Engineering)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 48 \times 2}$$

(Chi square value for MTTF upper limit)

↳ Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 22.62 \times 10^{-9}$ $\lambda = 22.62$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the B8 Process results in a FIT Rate of 2.71 @ 25C and 17.30 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PN43 die type has been found to have all pins able to withstand a transient pulse of +/-1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX8559ExAxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TDFN UCSP	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	TDFN UCSP	77 N/A	0 N/A
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010 (Note 3)	DC Parameters & functionality	TDFNX UCSP	77 77	0 0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
Note 3: UCSP Temperature Cycle performed at -40°C/125°C, 1000 Cycles, ramp rate 11°C/minute, dwell=15 minutes, One cycle/hour

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

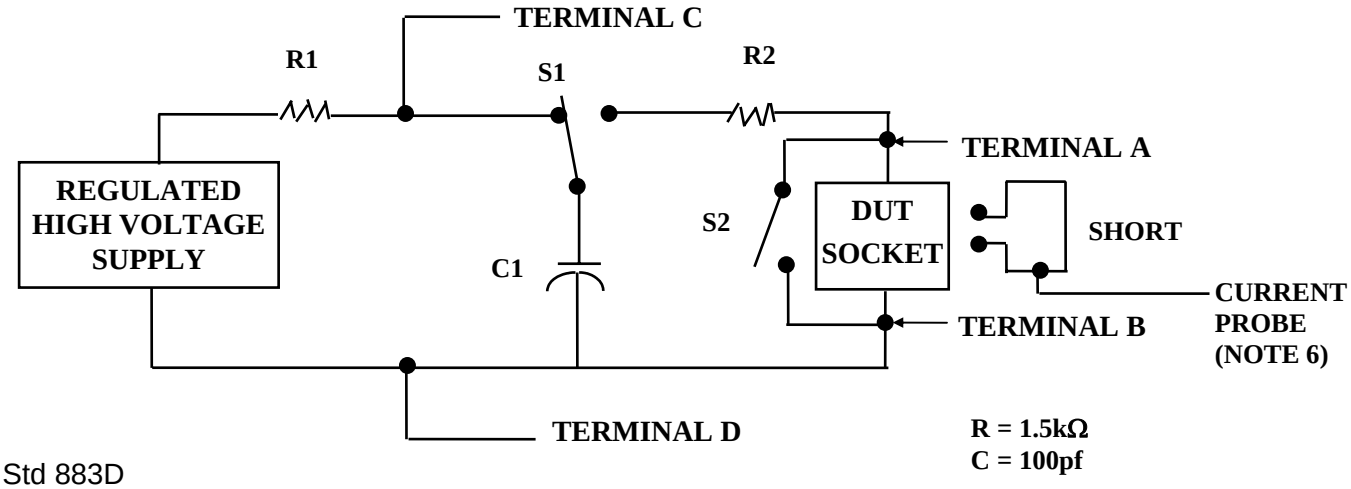
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8