RELIABILITY REPORT

FOR

MAX8662ETM+T

PLASTIC ENCAPSULATED DEVICES

October 2, 2012

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

Conclusion

The MAX8662ETM+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX8662/MAX8663 power-management ICs (PMICs) are efficient, compact devices suitable for smart cellular phones, PDAs, Internet appliances, and other portable devices. They integrate two synchronous buck regulators, a boost regulator driving two to seven white LEDs, four low-dropout linear regulators (LDOs), and a linear charger for a single-cell Li-ion (Li+) battery. Maxim's Smart Power Selector(tm) (SPS) safely distributes power between an external power source (AC adapter, auto adapter, or USB source), battery, and the system load. When system load peaks exceed the external source capability, the battery supplies supplemental current. When system load requirements are small, residual power from the external power source charges the battery. A thermal-limiting circuit limits battery-charge rate and external power-source current to prevent overheating. The PMIC also allows the system to operate with no battery or a discharged battery. The MAX8662 is available in a 6mm x 6mm, 48-pin TQFN package, while the MAX8663, without the LED driver, is available in a 5mm x 5mm, 40-pin TQFN package.

II. Manufacturing Information

A. Description/Function:	Power-Management ICs for Single-Cell, Li+ Battery-Operated Devices
B. Process:	S4
C. Number of Device Transistors:	33204
D. Fabrication Location:	Japan, Texas, California
E. Assembly Location:	China
F. Date of Initial Production:	February 15, 2007

III. Packaging Information

A. Package Type:	48L TQFN
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (2 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2259 / B
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	38°C/W
K. Single Layer Theta Jc:	1°C/W
L. Multi Layer Theta Ja:	27°C/W
M. Multi Layer Theta Jc:	1°C/W

IV. Die Information

A. Dimensions:	140 X 140 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 142 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 7.7 \times 10^{-9}$

$\lambda = 7.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S4 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (Latch-Up lot EU40IA014A, D/C 0818)

The PP46 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 500V per JEDEC JESD22-A114	Lot EU40HA004C, D/C 0809
ESD-CDM:	+/- 750V per JEDEC JESD22-C101	Lot TBT630202, D/C 0927

Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX8662ETM+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	47 48 47	0 0 0	TU44DQ003H, D/C 0830 SU40GA165D, D/C 0650 SU44BA072C, D/C 0634

Note 1: Life Test Data may represent plastic DIP qualification lots.