MAX8880EUT
Rev. A

RELIABILITY REPORT

FOR

MAX8880EUT

PLASTIC ENCAPSULATED DEVICES

March 28, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX8880 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX8880 is an ultra-low supply current, low-dropout linear regulator, capable of delivering up to 200mA. It is designed for battery-powered applications where reverse battery protection and long battery life are critical.

These regulators' low 3.5µA supply current extends battery life in applications with long standby periods. Unlike PNP-based designs, a 2-ohm PMOS device maintains ultra-low supply current throughout the entire operating range and in dropout. The parts are internally protected from output short circuits, reverse battery connection, and thermal overload. An internal power-OK (POK) comparator indicates when the output is out of regulation.

The MAX8880 output is adjustable from 1.25V to 5V using an external resistor-divider. The devices is available in a miniature 6-pin SOT23 packages.

B. Absolute Maximum Ratings

Item	Rating
IN to GND	-14V to +14V
SHDN to GND	-0.3V to (VIN + 0.3V), -0.3V to +0.3V when VIN < 0V
OUT, FB to GND	-0.3V to +6V when VIN > 5.7V,-0.3V to (VIN + 0.3V) when 0V = VIN = 5.7V, -0.3V to +0.3V when VIN < 0V
POK to GND	-0.3V to +14V
OUT Continuous Current	200mA
OUT Short Circuit	Indefinite
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature	-65°C to +165°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
6-Pin SOT23	696Mw
Derates above +70°C	
6-Pin SOT23	8.7mW/°C

II. Manufacturing Information

A. Description/Function: 12V, Ultra-Low-IQ, Low-Dropout Linear Regulators with POK

B. Process: B8 (Standard 0.8 micron silicon gate CMOS)

C. Number of Device Transistors: 134

D. Fabrication Location: California, USA

E. Assembly Location: Malaysia

F. Date of Initial Production: April, 200

III. Packaging Information

A. Package Type: **6-Pin SOT23**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Non-Conductive Epoxy

E. Bondwire: Gold (1.0 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05-2301-0032

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: Level 1

IV. Die Information

A. Dimensions: 60 x 41 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 0.8 microns (as drawn)

F. Minimum Metal Spacing: 0.8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

B.

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 240 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 4.52 \times 10^{-9}$

$\lambda = 4.52$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5553) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PY17 die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX8880EUT

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		240	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT23	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

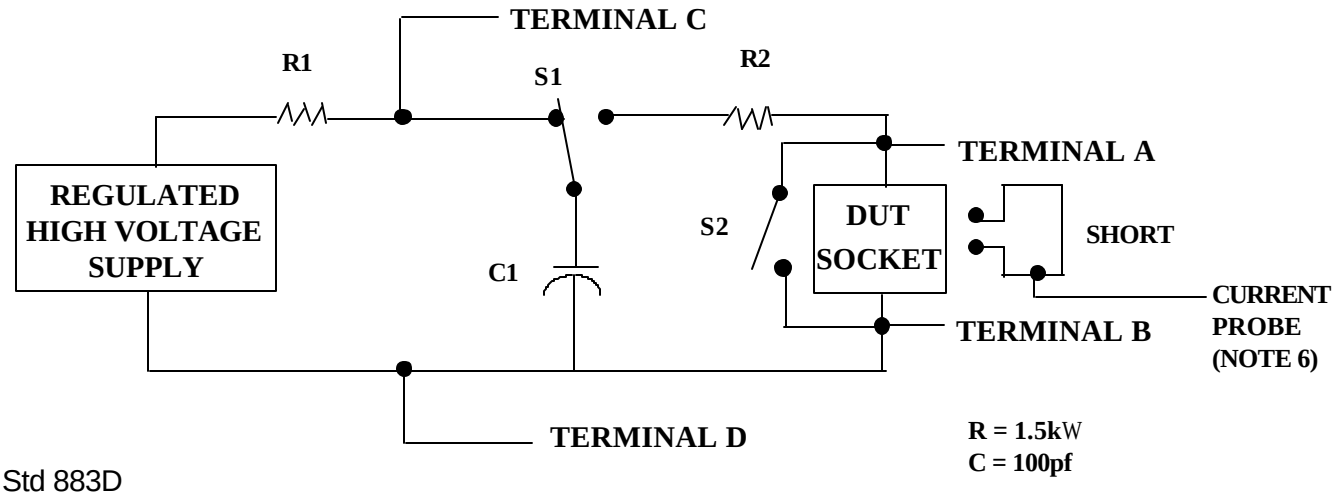
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

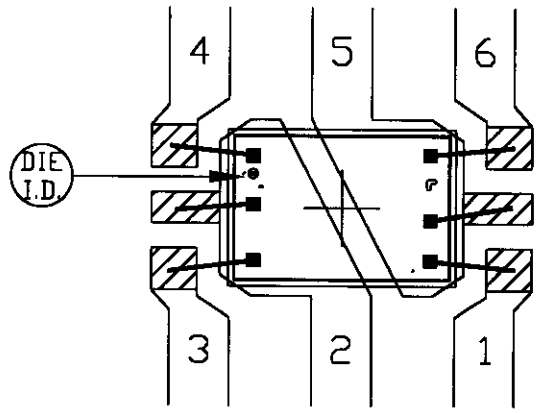
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



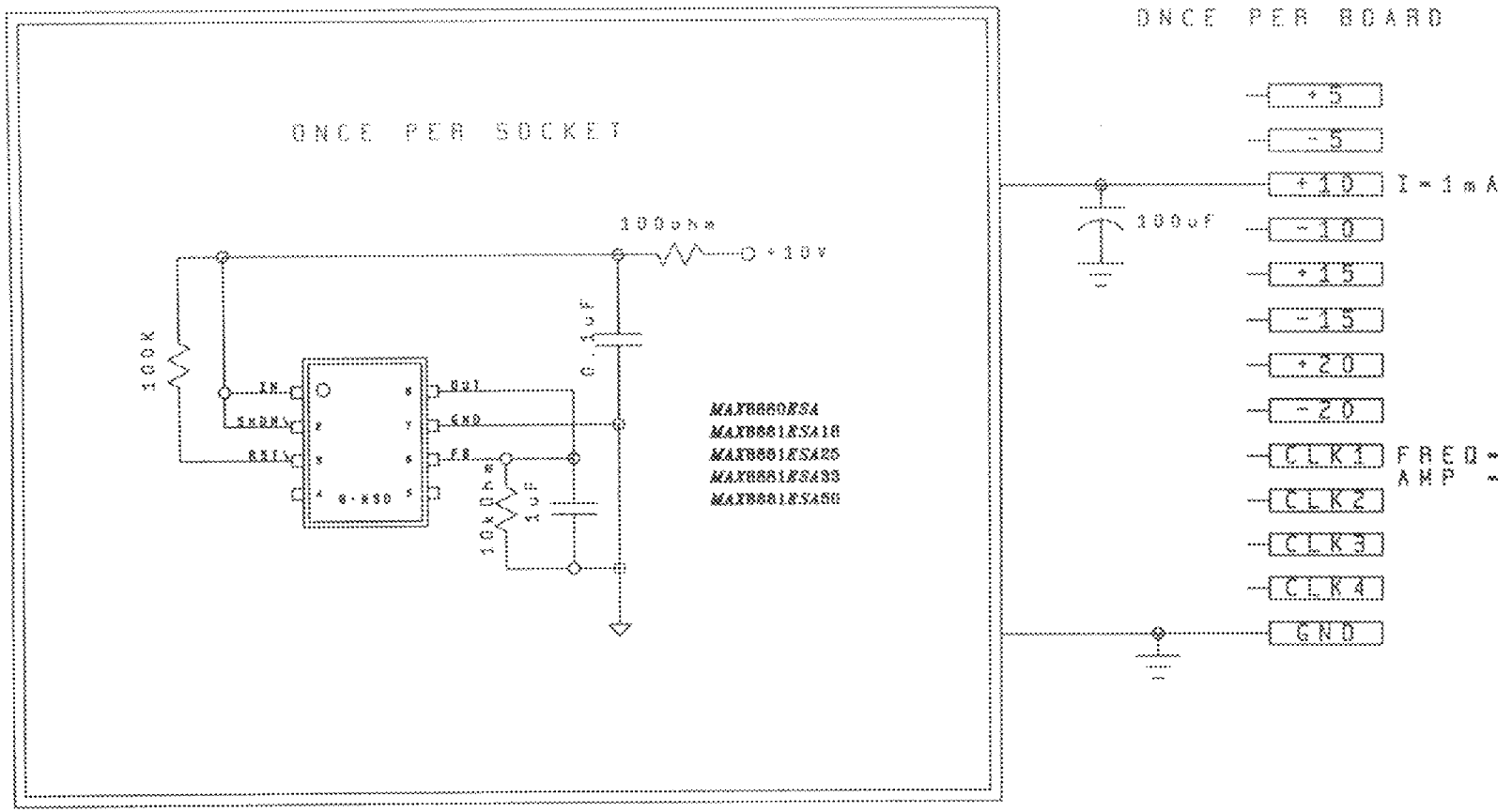
Mil Std 883D
Method 3015.7
Notice 8



NOTE: USE NON-CONDUCTIVE EPOXY ONLY

BONDABLE AREA

PKG. CODE: U6S-3		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 64x46	PKG. DESIGN			BOND DIAGRAM #: 05-2301-0032 / REV: A



Notes:

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	LAST SAVED: 11-24-1998_11:35		SIZE B	REVISION A 24-JUL-98	DWG NO. 06-5553
BRNINCKT	PROJECT: PY37				
	DESC: PIXY BURN IN SCHEM		FILE: BRNINCKT		SHEET 1 OF 2