RELIABILITY REPORT

FOR

MAX9152ESE+

PLASTIC ENCAPSULATED DEVICES

October 29, 2008

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Conclusion

The MAX9152ESE+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX9152 2 x 2 crosspoint switch is designed for applications requiring high speed, low power, and low-noise signal distribution. This device includes two LVDS/LVPECL inputs, two LVDS outputs, and two logic inputs that set the internal connections between differential inputs and outputs. The MAX9152 can be programmed to connect any input to either or both outputs, allowing it to be used in the following configurations: 2 5 2 crosspoint switch, 2:1 mux, 1:2 demux, 1:2 splitter, or dual repeater. This flexibility makes the MAX9152 ideal for protection switching in fault-tolerant systems, loopback switching for diagnostics, fanout buffering for clock/data distribution, and signal regeneration for communication over extended distances. Ultra-low 120psPK-PK (max) PRBS jitter ensures reliable communications in high-speed links that are highly sensitive to timing error, especially those incorporating clock-and-data recovery, or serializers and deserializers. The high-speed switching performance guarantees an 800Mbps data rate and less than 50ps (max) skew between channels. LVDS inputs and outputs are compatible with the TIA/EIA-644 LVDS standard. The LVDS inputs are designed to also accept LVPECL signals directly, and PECL signals with an attenuation network. The LVDS outputs are designed to drive 75 or 100 loads, and feature a selectable differential output resistance to minimize reflections. The MAX9152 is available in 16-pin TSSOP and SO packages, and consumes only 109mW while operating from a single +3.3V supply over the -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	800Mbps, LVDS/LVPECL-to-LVDS 2 x 2 Crosspoint Switch
B. Process:	0.35UM 2 Poly 3 Metal CMOS
C. Number of Device Transistors:	
D. Fabrication Location:	TSMC
E. Assembly Location:	Carsem Malaysia, NSEB/UTL Thailand, Unisem Malaysia
F. Date of Initial Production:	April 28, 2001

III. Packaging Information

A. Package Type:	16-pin SOIC (N)
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Ag Filled Epoxy
E. Bondwire:	1.0 (mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Multi Layer Theta Ja:	82.2°C/W
K. Multi Layer Theta Jc:	32°C/W

IV. Die Information

A. Dimensions:	57 X 65 mils
B. Passivation:	Silicon Dioxide/Silicon Nitride
C. Interconnect:	Al/Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35 um
F. Minimum Metal Spacing:	0.35 um
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	Silicon Dioxide
I. Die Separation Method:	Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are pending. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.59 \times 10^{-9}$

$\lambda = 13.59$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the TS352P3M Process results in a FIT Rate of 0.43 @ 25C and 7.50 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The HS10 die type has been found to have all pins able to withstand a HBM transient pulse of 7000 V per pin. Latch-Up testing has shown that this device withstands a current of 250 mA.

Table 1
Reliability Evaluation Test Results

MAX9152ESE+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = Biased Time = 192 hrs.	DC Parameters & functionality	80	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data