

RELIABILITY REPORT
FOR
MAX923xxA
PLASTIC ENCAPSULATED DEVICES

September 22, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Conclusion

The MAX923 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX923 dual micropower, low-voltage comparator features the lowest power consumption available. This comparator includes an internal 1.182V $\pm 1\%$ voltage reference, programmable hysteresis, and TTL/CMOS outputs that sink and source current.

Ideal for 3V or 5V single-supply applications, the MAX923 operates from a $\pm 1.25V$ to $\pm 5V$ dual supply, and its input voltage range swings from the negative supply rail to within 1.3V of the positive supply.

The MAX923's unique output stage continuously sources as much as 40mA. By eliminating power-supply glitches that commonly occur when comparators change logic states, the MAX923 minimizes parasitic feedback, which makes it easier to use.

The dual MAX923 provides a unique and simple method for adding hysteresis without feedback and complicated equations, simply by using the HYST pin and two resistors.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
V+ to V-, V+ to GND, GND to V- Inputs	-0.3V, +12V
Current, IN_+, IN_-, HYST	20mA
Voltage, IN_+, IN_-, HYST	(V+ + 0.3V) to (V- - 0.3V)
Outputs	
Current, REF	20mA
Current, OUT_	50mA
Voltage, REF	(V+ + 0.3V) to (V- - 0.3V)
Voltage, OUT_	(V+ + 0.3V) to (V- - 0.3V)
OUT_ Short-Circuit Duration (V+ \leq 5.5V)	Continuous
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
8-Pin PDIP	727mW
8-Pin SO	471mW
8-Pin uMAX	331mW
Derates above +70°C	
5-Pin PDIP	9.09W/°C
8-Pin SO	5.88W/°C
8-Pin uMAX	4.10W/°C

II. Manufacturing Information

A. Description/Function:	Ultra Low-Power, Dual-Supply Comparator
B. Process:	S3 - Standard 3 micron silicon gate CMOS
C. Number of Device Transistors:	267
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Malaysia, or Thailand
F. Date of Initial Production:	July, 1993

III. Packaging Information

A. Package Type:	8-Lead NSO	8-Lead PDIP	8-Lead uMAX
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin (all packages)		
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1501-0129	# 05-1501-0128	# 05-1501-0130
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-c:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	77 x 58 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 640 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 1.72 \times 10^{-9}$$

$$\lambda = 1.72 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5126) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1N**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The CM30-1 die type has been found to have all pins able to withstand a transient pulse of $\pm 2500\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX923xxA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		640	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	PDIP	77	0
			NSO	77	0
			uMAX	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

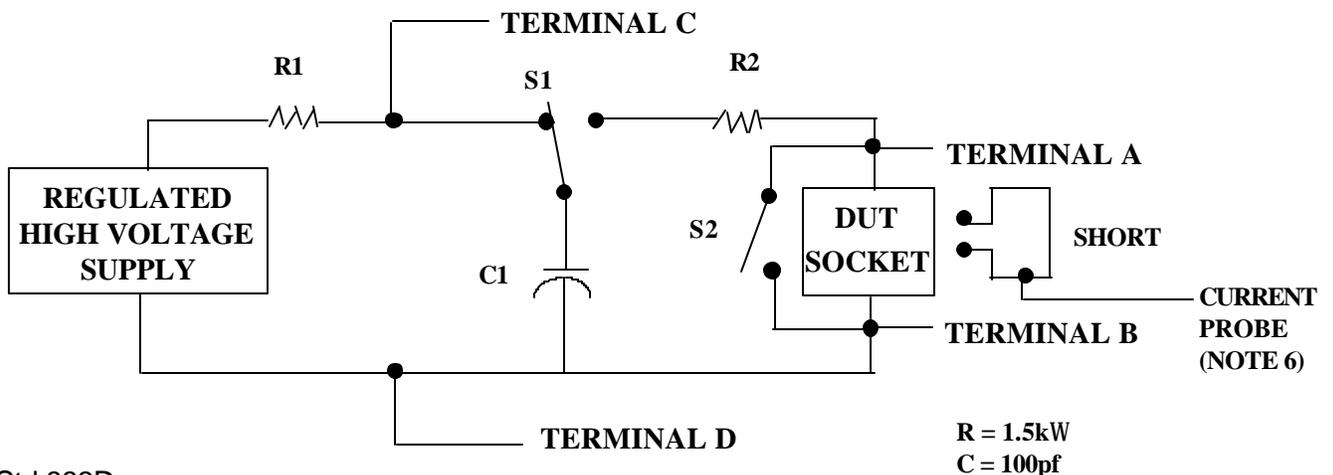
2/ No connects are not to be tested.

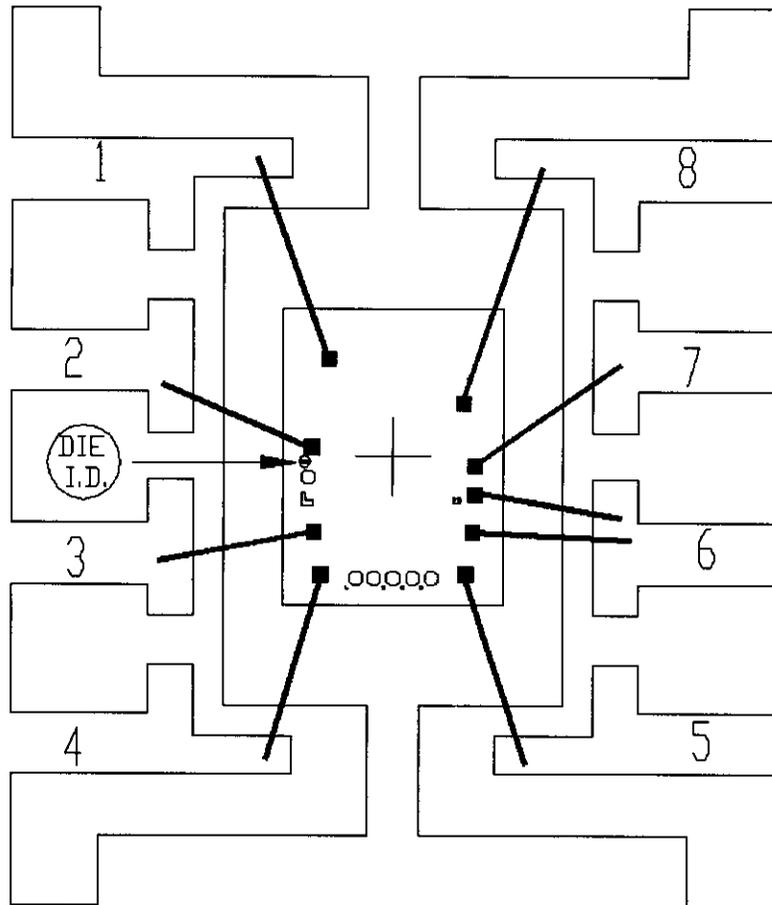
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: S8-4

APPROVALS

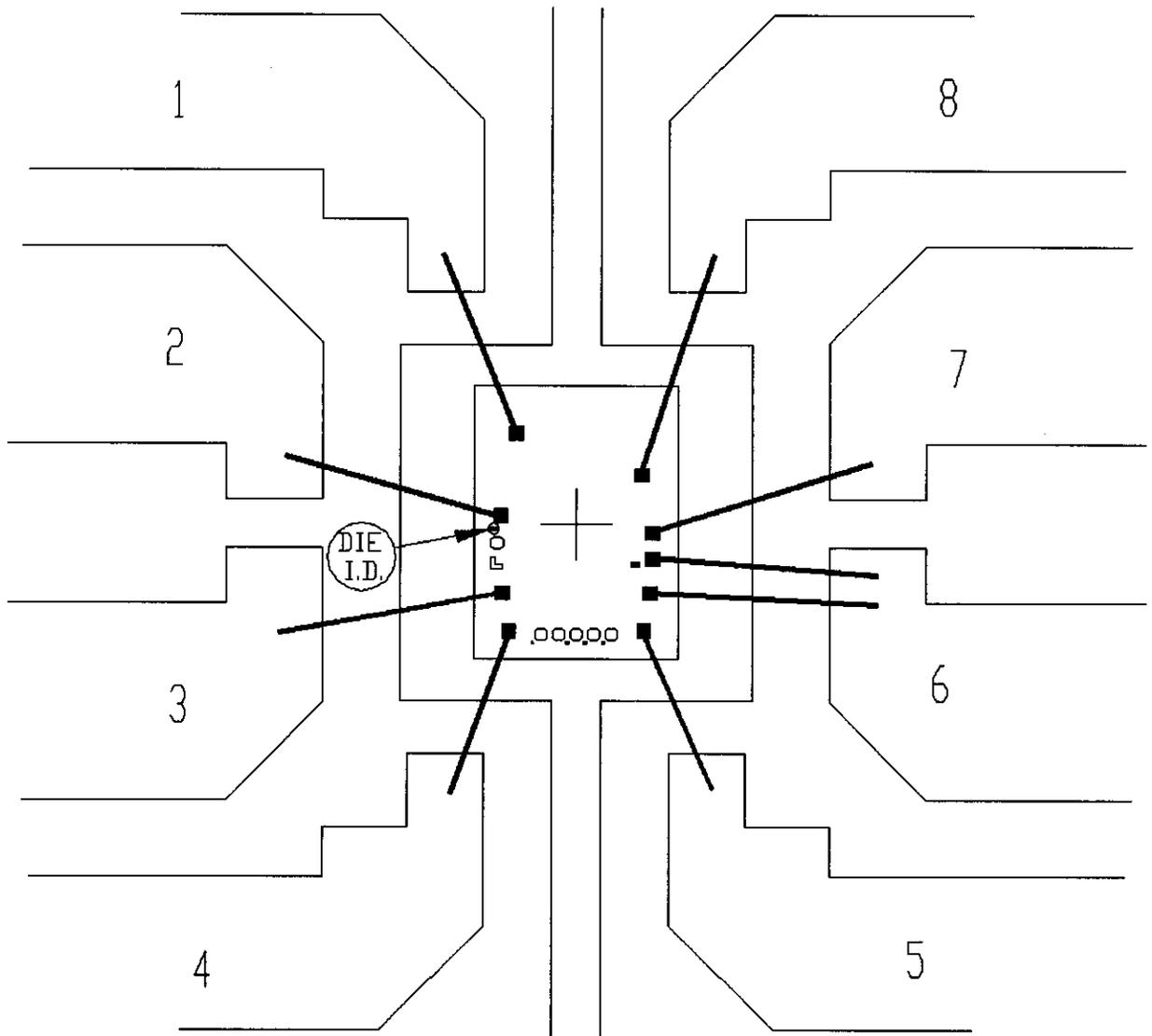
DATE

MAXIM

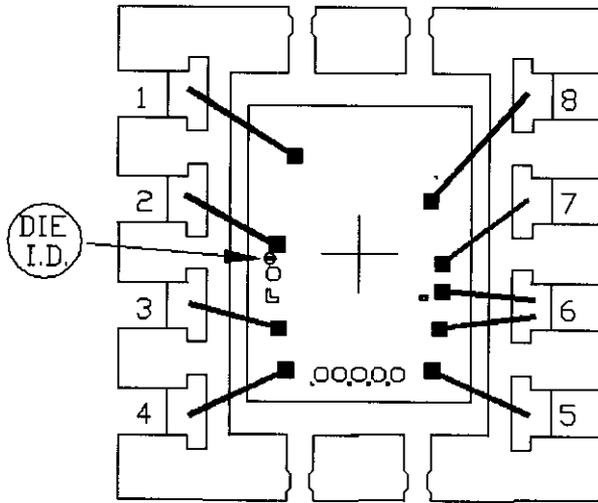
CAV./PAD SIZE:
90 X 130

PKG.
DESIGN

BUILDSHEET NUMBER: 05-1501-0129	REV.: A
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PKG.CODE: P8-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 100 X 100	PKG. DESIGN			BUILDSHEET NUMBER: 05-1501-0128 REV.: A



PKG.CODE: U8-1

APPROVALS

DATE

MAXIM

CAV./PAD SIZE:
68X94

PKG.
DESIGN

BUILDSHEET NUMBER:
05-1501-0130

REV:
A

