RELIABILITY REPORT

FOR

MAX9248ETM+ / MAX9248ECM+

PLASTIC ENCAPSULATED DEVICES

November 15, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

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Conclusion

The MAX9248ETM+ / MAX9248ECM+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX9248/MAX9250 digital video serial-to-parallel converters deserialize a total of 27 bits during data and control phases. In the data phase, the LVDS serial input is converted to 18 bits of parallel video data and in the control phase, the input is converted to 9 bits of parallel control data. The separate video and control phases take advantage of video timing to reduce the serial-data rate. The MAX9248/MAX9250 pair with the MAX9247 serializer to form a complete digital video transmission system. For operating frequencies less than 35MHz, the MAX9248/MAX9250 can also pair with the MAX9217 serializer. The MAX9248 features spread-spectrum capability, allowing output data and clock to spread over a specified frequency range to reduce EMI. The data and clock outputs are programmable for a spectrum spread of ±4% or ±2%. The MAX9250 features output enable input control to allow data busing. Proprietary data decoding reduces EMI and provides DC balance. The DC balance allows AC-coupling, providing isolation between the transmitting and receiving ends of the interface. The MAX9248/MAX9250 feature a selectable rising or falling output latch edge. ESD tolerance is specified for ISO 10605 with ±10kV Contact Discharge and ±30kV Air-Gap Discharge. The MAX9248/MAX9250 operate from a +3.3V ±10% core supply and feature a separate output supply for interfacing to 1.8V to 3.3V logic-level inputs. These devices are available in a 48-lead LQFP package and are specified from -40°C to +85°C or -40°C to +105°C.

II. Manufacturing Information

A. Description/Function:	27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers	
B. Process:	TS35	
C. Number of Device Transistors:		
D. Fabrication Location:	Taiwan	
E. Assembly Location:	China, Malaysia, Taiwan and Thailand	Korea, Malaysia and Taiwan
F. Date of Initial Production:	January 21, 2006	

III. Packaging Information

A. Package Type:	48-pin TQFN 6x6	48-pin LQFP 7x7
B. Lead Frame:	Copper	Copper
C. Lead Finish:	100% matte Tin	100% matte Tin
D. Die Attach:	Conductive	Conductive
E. Bondwire:	Au (1 mil dia.)	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2190	#05-9000-2191
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	38°C/W	°C/W
K. Single Layer Theta Jc:	1°C/W	°C/W
L. Multi Layer Theta Ja:	27°C/W	46°C/W
M. Multi Layer Theta Jc:	1°C/W	10°C/W

IV. Die Information

A. Dimensions:	134 X 117 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2-4 = 0.6 micron (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2-3 = 0.5 / Metal4 = 0.6 micron (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

λ = 22.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the Process results in a FIT Rate of 0.10 @ 25C and 1.8 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The HS48 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2500V per JEDEC JESD22-A114 (lot QS30BA004E, D/C0921)
ESD-CDM:	+/- 750V per JEDEC JESD22-C101 (lot QS30BA004E, D/C0921)
ESD-MM:	+/- 200V per JEDEC JESD22-A115 (lot QPL544667S, D/C 1143)
ESD gun (contact):	+/- 10kV LVDS pins per ISO10605, +/-10kV LVDS pins per IEC61000-4-2
ESD gun (air gap):	+/- 30kV LVDS pins per ISO10605, +/- 15kV LVDS pins per IEC61000-4-2

Latch-Up testing has shown that this device withstands a current of +/- 100mA and overvoltage per JEDEC JESD78 (lot QS30BA004E, D/C0921).

Table 1
Reliability Evaluation Test Results

MAX9248ECM+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.