RELIABILITY REPORT

FOR

MAX9259GTN+

PLASTIC ENCAPSULATED DEVICES

August 1, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX9259GTN/V+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX9259/MAX9260 chipset presents Maxim's gigabit multimedia serial link (GMSL) technology. The MAX9259 serializer pairs with the MAX9260 deserializer to form a complete digital serial link for joint transmission of high-speed video, audio, and control data. The MAX9259/MAX9260 allow a maximum serial payload data rate of 2.5Gbps for a 15m shielded twisted-pair (STP) cable. The 24-bit or 32-bit width parallel interface operates up to a maximum bus clock of 104MHz or 78MHz, respectively. This serial link supports display panels from QVGA (320 x 240) up to XGA (1280 x 768), or dual-view WVGA (2 x 854 x 480). The 24-bit or 32-bit mode handles 21 or 29 bits of data, along with an I²S input, supporting 4- to 32-bit audio word lengths and an 8kHz to 192kHz sample rate. The embedded control channel forms a full-duplex, differential 100kbps to 1Mbps UART link between the serializer and deserializer. The host electronic control unit (ECU) or microcontroller (µC) resides either on the MAX9259 (for video display) or on the MAX9260 (for image sensing). In addition, the control channel enables ECU/µC control of peripherals in the remote side of the serial link through I²C (base mode) or a user-defined full-duplex UART format (bypass mode). The MAX9259 serializer driver preemphasis and channel equalizer on the MAX9260 extend the link length and enhance the link reliability. Spread spectrum is available on the MAX9259/MAX9260 to reduce EMI on the serial and parallel output data signals. The differential link complies with the ISO 10605 and IEC 61000-4-2 ESD-protection standards. The core supplies for the MAX9259/MAX9260 are 1.8V and 3.3V, respectively. Both devices use an I/O supply from 1.8V to 3.3V. These devices are available in a 64-pin TQFP package (10mm x 10mm) and a 56-pin TQFN package (8mm x 8mm x 0.75mm) with an exposed pad. Electrical performance is guaranteed over the -40°C to +105°C automotive temperature range.

II. Manufacturing Information

A. Description/Function:	Gigabit Multimedia Serial Link with Spread Spectrum and Full-Duplex Control Channel
B. Process:	TS18
C. Number of Device Transistors:	245712
D. Fabrication Location:	Taiwan
E. Assembly Location:	Thailand or Taiwan
F. Date of Initial Production:	October 20, 2009

III. Packaging Information

A. Package Type:	56-pin TQFN 8x8
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4285
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	35°C/W
K. Single Layer Theta Jc:	0.6°C/W
L. Multi Layer Theta Ja:	21°C/W
M. Multi Layer Theta Jc:	0.6°C/W

IV. Die Information

A. Dimensions:	139.43X 139.43 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 4340 \times 246 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 0.9 \times 10^{-9}$

$\lambda = 0.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.11 @ 25C and 1.87 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (Latch-Up lot QVBZCQ001A, D/C 0940)

The HS40 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 8000V per JEDEC JESD22-A114	Lot QVBZDA008E, D/C 1136
ESD-CDM:	+/- 750V per JEDEC JESD22-C101	Lot QVBZDA007G, D/C 1134

Latch-Up testing has shown that this device withstands a current of+/- 250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX9259GTN+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	82	0	QVBZDQ003C, D/C 1104
	Biased	& functionality	87	0	QVBZDA005C, D/C 1123
	Time = 1000 hrs.		77	0	QVBZDQ002F, D/C 1036

Note 1: Life Test Data may represent plastic DIP qualification lots.