RELIABILITY REPORT

FOR

MAX9321ExA

PLASTIC ENCAPSULATED DEVICES

May 5, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Manager, Reliability Operations

Conclusion

The MAX9321 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX9321 is a low-skew differential receiver/drivers designed for clock and data distribution. The differential input can be adapted to accept a single-ended input by connecting the on-chip V_{BB} supply to an input as a reference voltage.

The MAX9321 features ultra-low propagation delay (172ps) and part-to-part skew (20ps) with 24mA maximum supply current, making these devices ideal for clock buffering or repeating. For interfacing to differential HSTL and LVPECL signals, these devices operate over a +2.25V to +3.8V supply range, allowing high-performance clock and data distribution in systems with a nominal +2.5V or +3.3V supply. For differential LVECL operation, these devices operate from a -2.25V to -3.8V supply. Multiple pinouts are provided to simplify routing across a backplane to either side of a double-sided board.

The device is offered in space-saving 8-pin SOT23, SO, and µMAX packages.

B. Absolute Maximum Ratings

Item	Rating
VCC to VEE	+4.1V
D or D	VEE - 0.3V to VCC + 0.3V
D to D	±3.0V
Continuous Output Current	50mA
Surge Output Current	100mA
Junction-to-Ambient Thermal Resistance in Still Air	
8-Pin SOT23	+112°C/W
8-Pin µMAX	+221°C/W
8-Pin SO	+170°C/W
Junction-to-Ambient Thermal Resistance with 500 LFPM Airflow	
8-Pin SOT23	+78°C/W
8-Pin µMAX	+155°C/W
8-Pin SO	+99°C/W
Junction-to-Case Thermal Resistance	
8-Pin SOT23	+80°C/W
8-Pin µMAX	+39°C/W
8-Pin SO	+40°C/W
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
ESD Protection	
Human Body Model (D, D, Q_, Q_,VBB)	>2kV
Soldering Temperature (10s)	+300°C

II. Manufacturing Information

A. Description/Function:	Differential LVPECL/LVECL/HSTL Receiver/Drivers
B. Process:	GST2 – High Speed Double Poly-Silicon Bipolar Process
C. Number of Device Transistors:	162
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Malaysia or Thailand
F. Date of Initial Production:	July, 2001

III. Packaging Information

	8-Pin uMAX	**8-Pin SO**	**8-Pin SOT**
A. Package Type:			
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin (all packages)		
D. Die Attach:	Silver-Filled Epoxy	Silver-Filled Epoxy	Silver-Filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-0010	# 05-3601-0047	# 05-3601-0011
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	46 x 30 mils
B. Passivation:	Si_3N_4 (Silicon nitride)
C. Interconnect:	Poly / Au
D. Backside Metallization:	None
E. Minimum Metal Width:	2 microns (as drawn)
F. Minimum Metal Spacing:	2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director**)**

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9706 \times 93 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 5.29 \times 10^{-9}$

λ = 5.29 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. The Burn-In Schematic (Spec.# 06-5812) shows the static circuit used for this test. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-B2A**). Current monitor data for the GST2 Process results in a FIT Rate of 0.09 @ 25C and 1.52 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The EC09-3 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX9321ExA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality		93	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	NSO SOT uMAX	77 77 77	0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

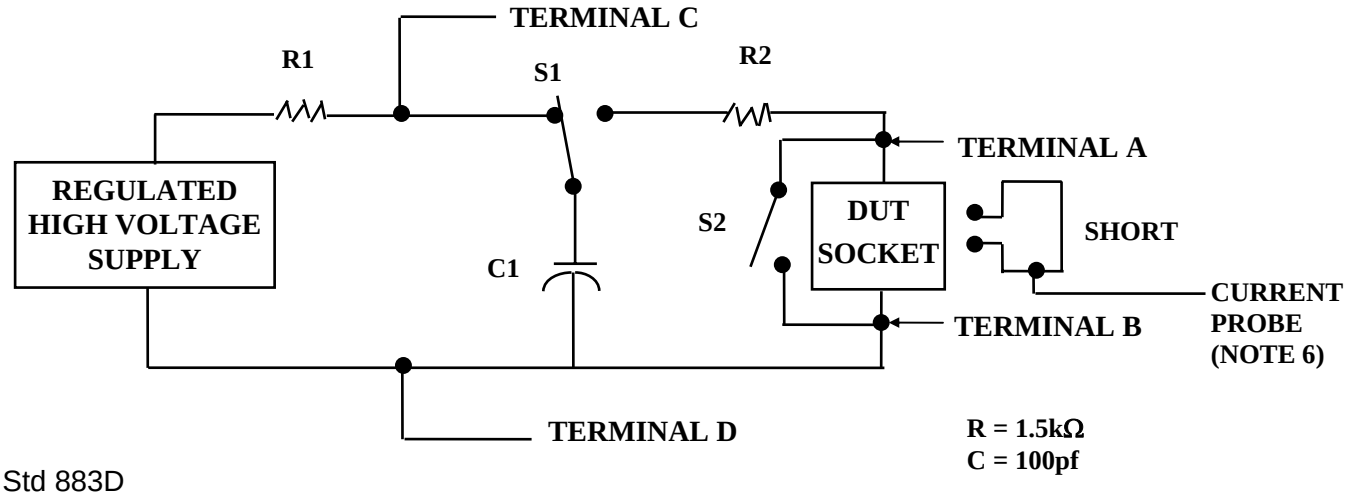
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

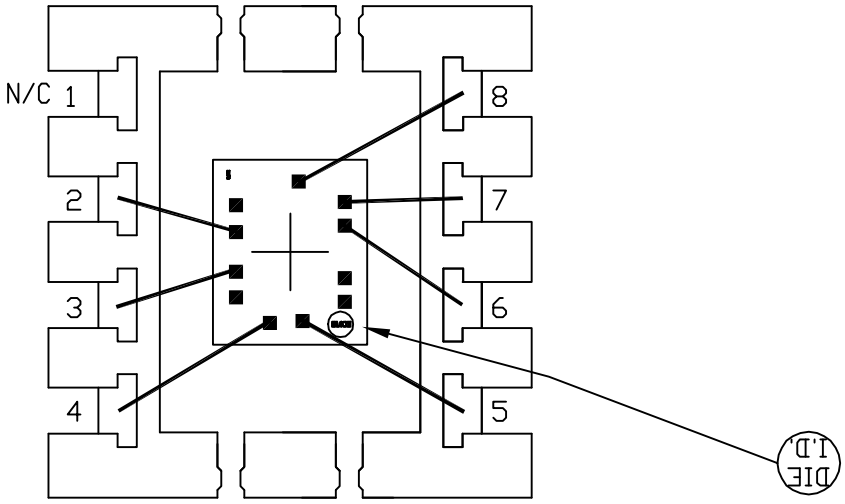
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

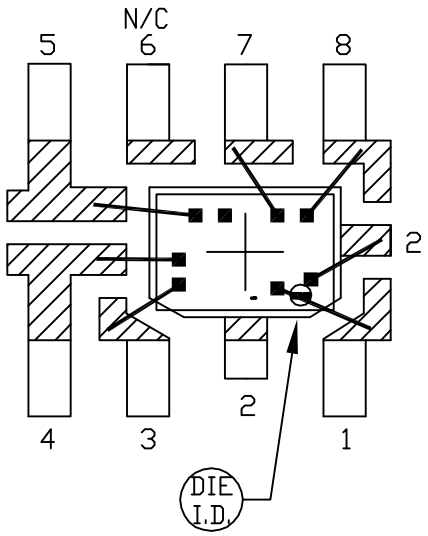
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG. CODE: U8-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 68x94	PKG.			BOND DIAGRAM #: 05-9000-0010	REV: A
	DESIGN				



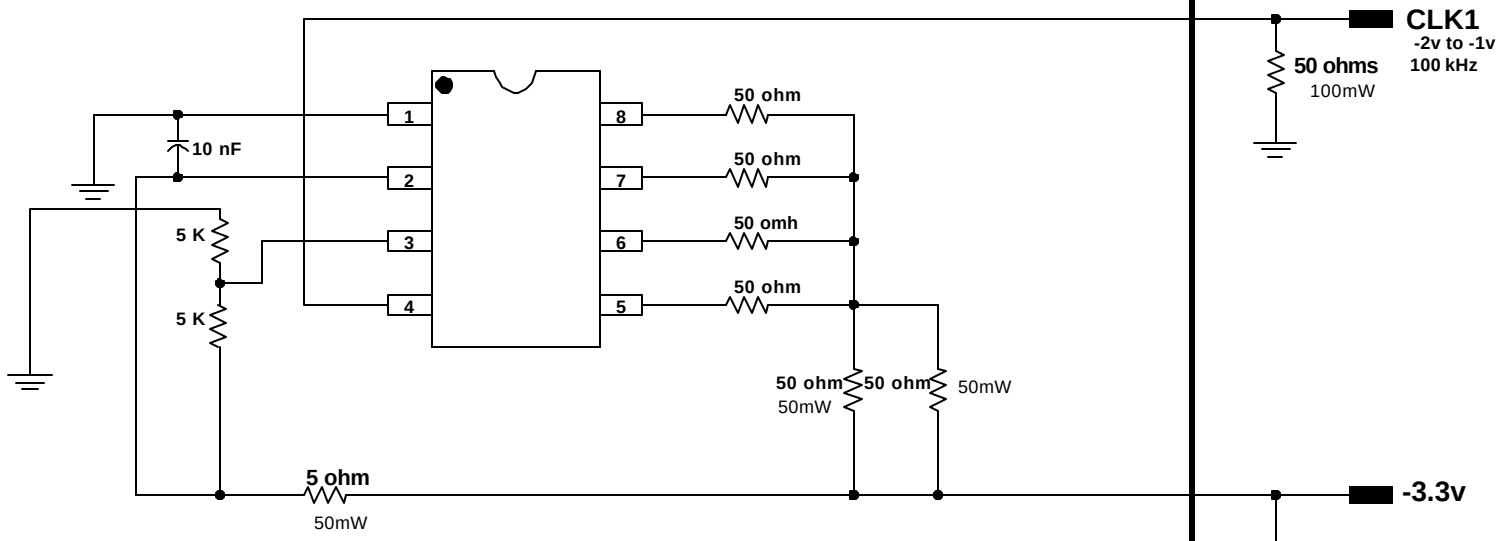
NOTE: CAVITY DOWN

BONDABLE AREA

PKG. CODE: K8-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 50x34	PKG.		3/20/01	BOND DIAGRAM #: 05-3601-0011	REV: A
	DESIGN		3/20/01		

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 9320
PACKAGE: 8-SOT23
MAX. EXPECTED CURRENT = 60mA

NOTES: Clk 1: 100kHz (-2 to -1V)