RELIABILITY REPORT

FOR

MAX9619AXT+T

PLASTIC ENCAPSULATED DEVICES

April 14, 2015

**MAXIM INTEGRATED**

160 RIO ROBLES

SAN JOSE, CA 95134

| Approved by |
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| Sokhom Chum |
| Quality Assurance |
| Reliability Engineer |

## Conclusion

The MAX9619AXT+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

## Table of Contents



## I. Device Description

A. General

The MAX9617-MAX9620 are low-power, zero-drift operational amplifiers available in space-saving SC70 packages. They are designed for use in portable consumer, medical, and industrial applications. The MAX9617-MAX9620 feature rail-to-rail CMOS inputs and outputs, a 1.5MHz GBW at just 59µA supply current and 10µV (max) zero-drift input offset voltage over time and temperature. The zero-drift feature reduces the high 1/f noise typically found in CMOS input operational amplifiers, making it useful for a wide variety of low-frequency measurement applications. The MAX9617 and MAX9619 are available in a space-saving, 2mm x 2mm, 6-pin SC70 package. The MAX9619 features a power-saving shutdown mode. The MAX9618 is available in a 2mm x 2mm, 8-pin SC70 package. The MAX9620 is available in a 2mm x 2mm, 5-pin SC70 package. All devices are specified over the -40°C to +125°C automotive operating temperature range.

## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | High-Efficiency, 1.5MHz Op Amps with RRIO |
| B. Process: | S18 |
| C. Number of Device Transistors: | 1452 |
| D. Fabrication Location: | California |
| E. Assembly Location: | Malaysia, Thailand |
| F. Date of Initial Production: | January 8, 2010 |

## III. Packaging Information

| | |
|---|---|
| A. Package Type: | 6-pin SC70 |
| B. Lead Frame: | Copper |
| C. Lead Finish: | 100% matte Tin |
| D. Die Attach: | Non-conductive |
| E. Bondwire: | Au (1 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | #05-9000-3789 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1 |
| J. Single Layer Theta Ja: | 326°C/W |
| K. Single Layer Theta Jc: | 115°C/W |
| L. Multi Layer Theta Ja: | 326.5°C/W |
| M. Multi Layer Theta Jc: | 115°C/W |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 27.559X27.9527 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Al with Ti/TiN Barrier |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 0.18um |
| F. Minimum Metal Spacing: | 0.18um |
| G. Bondpad Dimensions: | |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

| | |
|---|---|
| A. Quality Assurance Contacts: | Don Lipps (Manager, Reliability Engineering)<br>Bryan Preeshl (Vice President of QA) |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet.<br>0.1% for all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SXQYAQ003A, D/C 0944)

The OY40-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

**Table 1**
Reliability Evaluation Test Results

**MAX9619AXT+T**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES | COMMENTS |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters & functionality | 48 | 0 | SXQZBQ001C, D/C 0927 |

Note 1: Life Test Data may represent plastic DIP qualification lots.