MAX9704ETJ
Rev. A

RELIABILITY REPORT

FOR

**MAX9704ETJ**

PLASTIC ENCAPSULATED DEVICES

April 4, 2004

# MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086


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**Conclusion**

The MAX9704 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

**Table of Contents**



## I. Device Description

### A. General

The MAX9704 stereo class D audio power amplifiers provide class AB amplifier performance with class D efficiency, conserving board space and eliminating the need for a bulky heatsink. Using a class D architecture, this device delivers up to 15W while offering up to 78% efficiency. Proprietary and patent-protected modulation and switching schemes render the traditional class D output filter unnecessary.

The MAX9704 offers two modulation schemes: a fixed-frequency mode (FFM), and a spread-spectrum mode (SSM) that reduces EMI-radiated emissions due to the modulation frequency. The device utilizes a fully differential architecture, a full bridged output, and comprehensive click-and-pop suppression.

The MAX9704 features high 80dB PSRR, low 0.07% THD+N, and SNR in excess of 100dB. Short-circuit and thermal-overload protection prevents the device from being damaged during a fault condition. The MAX9704 is available in a 32-pin TQFN (7mm x 7mm x 0.8mm) package. Both devices are specified over the extended -40°C to +85°C temperature range.

### B. Absolute Maximum Ratings

| Item | Rating |
|---|---|
| (All voltages referenced to GND.) | |
| VDD to PGND, AGND | 30V |
| OUTR_, OUTL_, C1N | -0.3V to (VDD + 0.3V) |
| C1P | (VDD - 0.3V) to (CHOLD + 0.3V) |
| CHOLD | (VDD - 0.3V) to +40V |
| All Other Pins to GND | -0.3V to +12V |
| Duration of OUTR_/OUTL_ | |
| Short Circuit to GND, VDD | 10s |
| Continuous Input Current (VDD, PGND) | 1.6A |
| Continuous Input Current | 0.8A |
| Continuous Input Current (all other pins) | ±20mA |
| Continuous Power Dissipation (TA = +70°C) | |
| Junction Temperature | +150°C |
| Operating Temperature Range | -40°C to +85°C |
| Storage Temperature Range | -65°C to +150°C |
| Continuous Power Dissipation (TA = +70C) | |
| 32-PIN TQFN (7x7) | 2666.7mW |
| Derates above +70°C | |
| 32-PIN TQFN (7x7) | 33.3mW/°C |

## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | 15W, Filterless, Spread-Spectrum Stereo Class D Amplifiers |
| B. Process: | BCD80 |
| C. Number of Device Transistors: | 4630 |
| D. Fabrication Location: | Oregon, USA |
| E. Assembly Location: | Philippines, Malaysia or Thailans |
| F. Date of Initial Production: | March, 2004 |

## III. Packaging Information

| | |
|---|---|
| A. Package Type: | **32-Pin TQFN (7x7)** |
| B. Lead Frame: | Copper |
| C. Lead Finish: | Solder Plate |
| D. Die Attach: | Silver-filled Epoxy |
| E. Bondwire: | Gold (1.3 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | # 05-9000-0637 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-A: | Level 1 |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 183 X 183 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Aluminum/Si (Si = 1%) |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 3 microns (as drawn) |
| F. Minimum Metal Spacing: | 3 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 22.62 \times 10^{-9}$

$\lambda = 22.62$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6165) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The AU19-3 die type has been found to have all pins able to withstand a transient pulse of ±800V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

**Table 1**
Reliability Evaluation Test Results

**MAX9704ETJ**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | PACKAGE | SAMPLE SIZE | NUMBER OF FAILURES |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | | |
| | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | | 48 | 0 |
| **Moisture Testing** (Note 2) | | | | | |
| Pressure Pot | Ta = 121°C<br>P = 15 psi.<br>RH= 100%<br>Time = 168hrs. | DC Parameters<br>& functionality | QFN | 77 | 0 |
| 85/85 | Ta = 85°C<br>RH = 85%<br>Biased<br>Time = 1000hrs. | DC Parameters<br>& functionality | | 77 | 0 |
| **Mechanical Stress** (Note 2) | | | | | |
| Temperature Cycle | -65°C/150°C<br>1000 Cycles<br>Method 1010 | DC Parameters<br>& functionality | | 77 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

**Attachment #1**

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|---|---|---|
| 1. | All pins except $V_{PS1}$ 3/ | All $V_{PS1}$ pins |
| 2. | All input and output pins | All other input-output pins |

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

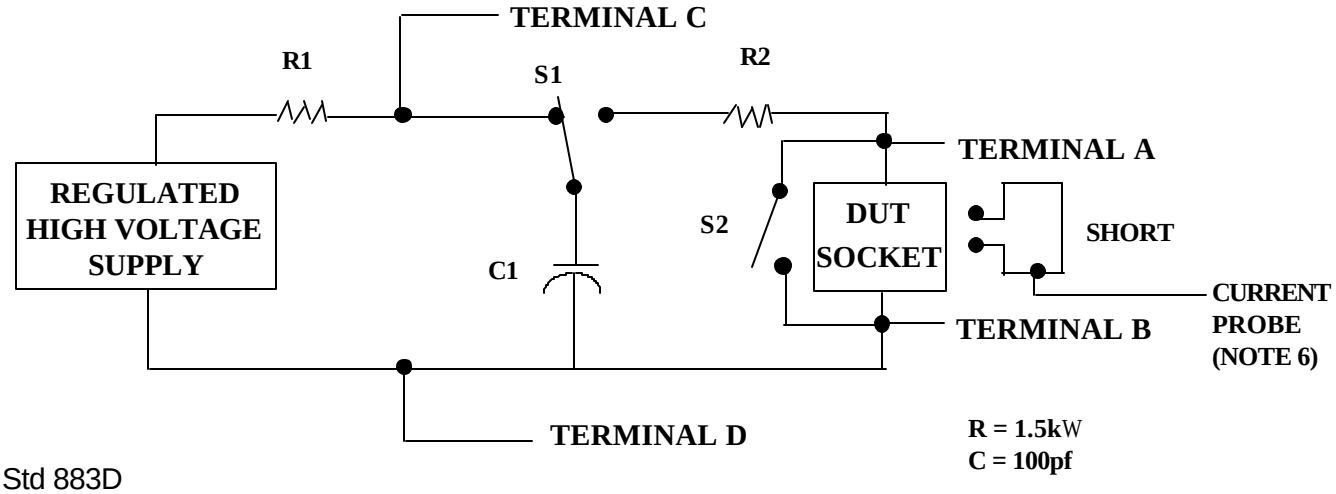
(e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

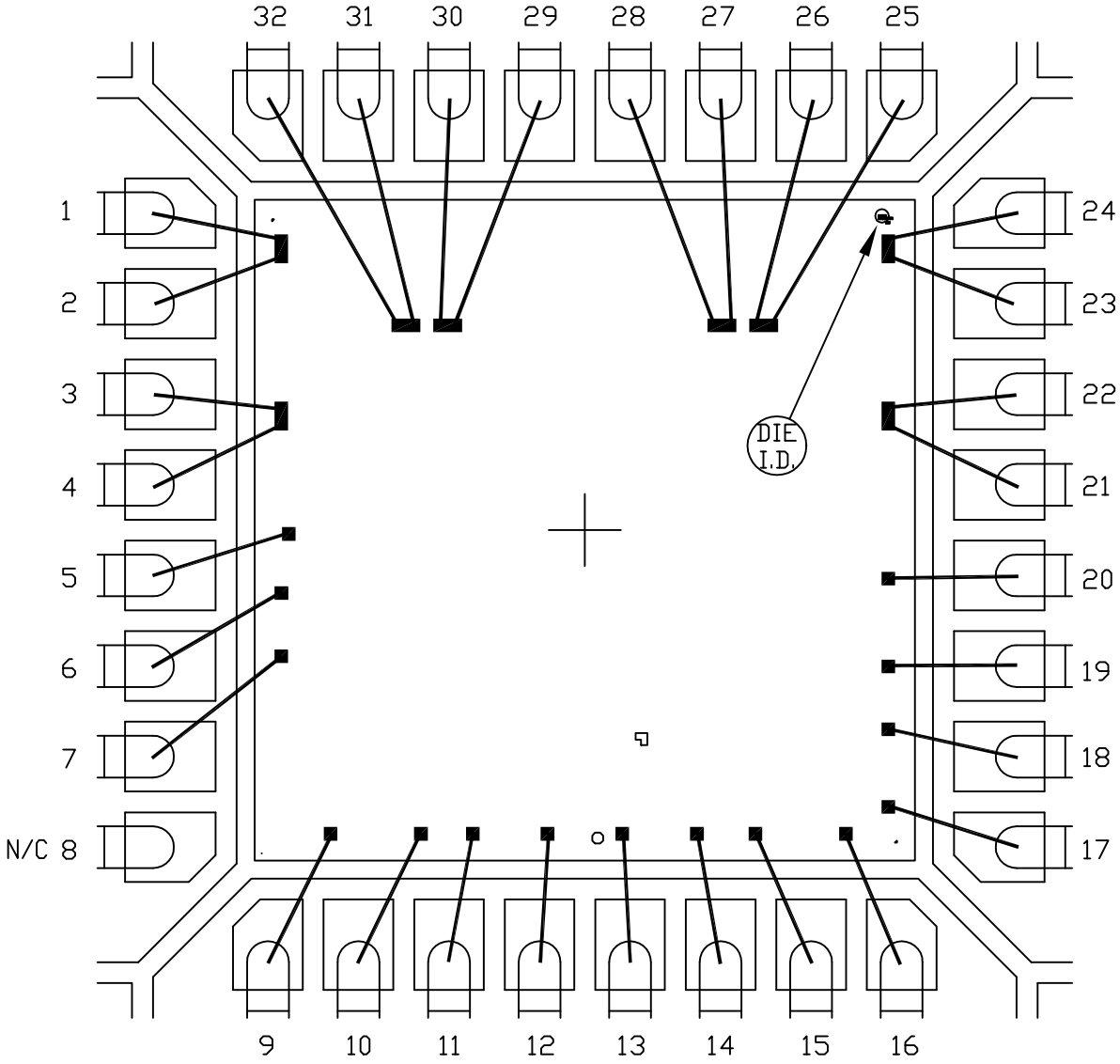
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

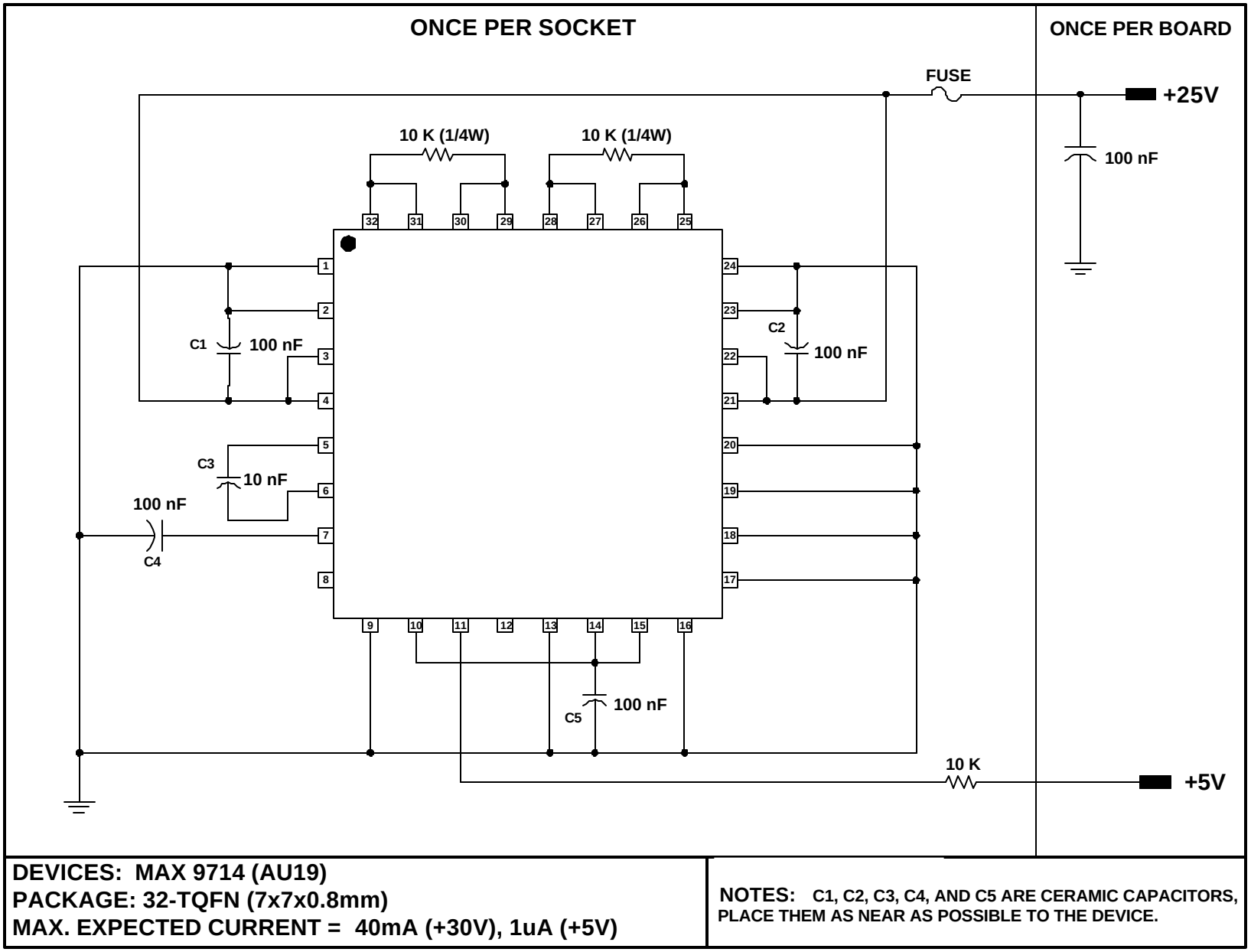



Mil Std 883D
Method 3015.7
Notice 8

7x7x0.8mm QFN THIN PKG. EXPOSED PAD PKG.




| PKG. CODE: T3277-1 | | SIGNATURES | DATE | MAXIM CONFIDENTIAL & PROPRIETARY | |
|---|---|---|---|---|---|
| CAV./PAD SIZE: 193x193 | PKG. | | | BOND DIAGRAM #: 05-9000-0637 | REV: A |
| | DESIGN | | | | |




**DEVICES: MAX 9714 (AU19)**
**PACKAGE: 32-TQFN (7x7x0.8mm)**
**MAX. EXPECTED CURRENT = 40mA (+30V), 1uA (+5V)**

**NOTES:** C1, C2, C3, C4, AND C5 ARE CERAMIC CAPACITORS, PLACE THEM AS NEAR AS POSSIBLE TO THE DEVICE.