RELIABILITY REPORT

FOR

MAXM17532AMB+T

PLASTIC ENCAPSULATED DEVICES

January 25, 2018

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAXM17532AMB+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAXM17532 is a step-down DC-DC power module built in a compact uSLIC™ package. The MAXM17532 integrates a controller, MOSFETs, an inductor, as well as the compensation components. The device operates from an input voltage of 4.0V to 42V, supports an adjustable output voltage from 0.9V to 5.5V, and supplies up to 100mA of load current. The high level of integration significantly reduces design complexity, manufacturing risks and offers a true "plug and play" power supply solution, hence reducing the time-to-market. The MAXM17532 uses peak-current-mode control and operates in pulse-width modulation (PWM) mode. The MAXM17532 is available in a thermally enhanced, compact 10-pin 2.6mm x 3mm x 1.5mm uSLIC package and is rated to operate over the full -40°C to +125°C industrial/automotive temperature range.

II. Manufacturing Information

A. Description/Function:	4V to 42V, 100mA, Compact Step-Down Power Module
B. Process:	S18
C. Fabrication Location:	USA
D. Assembly Location:	China
E. Date of Initial Production:	May 18, 2017

III. Packaging Information

A. Package Type:	10-pad eMGA
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Assembly Diagram:	#05-100290
G. Flammability Rating:	Class UL94-V0
H. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
I. Single Layer Theta Ja:	41.7°C/W
J. Single Layer Theta Jc:	15.8°C/W
K. Multi Layer Theta Ja:	N/A°C/W
L. Multi Layer Theta Jc:	N/A°C/W

IV. Die Information

A. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
B. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
C. Minimum Metal Width:	0.23 microns (as drawn)
D. Minimum Metal Spacing:	0.23 microns (as drawn)
E. Isolation Dielectric:	SiO_2
F. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 4340 \times 236 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 0.89 \times 10^{-9}$

$\lambda = 0.89$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05@ 25C and 0.93@ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The PI41-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAXM17532AMB+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 1000 hrs.	DC Parameters & functionality	236	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.