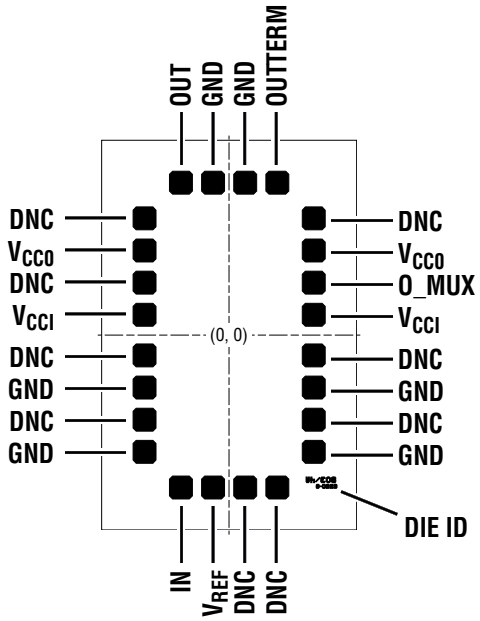
ANALOG DEVICES

DICE/DWF SPECIFICATION

LTC6560
Single Channel Transimpedance Amplifier with Output Multiplexing



DIE CROSS REFERENCE

Finished Part Number	Order Part Number
LTC®6560 LTC6560	LTC6560DICE LTC6560DWF*

Please refer to ADI standard product data sheet for other applicable product information.
***DWF = DICE in wafer form.**

Die Size: 36mils × 55mils (914.4µm × 1397µm)
Bond Pad Size: 102µm × 102µm (4mils × 4mils)
Bond Pad Opening: 82µm × 82µm (3.22mils × 3.22mils)
Bond Pad Metal Thickness: 7.4µm (0.29mils)
Wafer Saw Street Width: 2.4mils (61µm)
Wafer/Die Thickness: 8mils (204µm)
Backside Metal: None
Backside Potential: V^-

FEATURES

- **220MHz –3dB Bandwidth with 2pF Input Capacitance**
- **Single-Ended Output**
- **74kΩ Transimpedance Gain**
- **4.8pA/√Hz Input Current Noise Density at 200MHz (2pF)**
- **64nA$_{RMS}$ Integrated Input Current Noise Over 200MHz (2pF)**
- **Linear Input Range 0µA to 30µA**
- **Overload Current > ±400mA Peak**
- Fast Overload Recovery: 1mA in 12ns
- Fast Output MUXing: <50ns
- Single 5V Supply
- 90mW Power Dissipation
- 2V$_{P-P}$ Output Swing on 100Ω Load
- Output MUX Combines Multiple LTC6560 Devices

APPLICATIONS

- LIDAR Receiver
- Industrial Imaging

DESCRIPTION

The LTC6560 is a low-noise, transimpedance amplifier (TIA) with 220MHz bandwidth. The LTC6560's low noise, high transimpedance and low power dissipation are ideal for LIDAR receivers using avalanche photodiodes (APDs). The LTC6560 features 74kΩ transimpedance gain and 30µA linear input current range. Using an APD with a total input capacitance of 2pF, the input current noise density is 4.8pA/√Hz at 200MHz. With lower capacitance, noise and bandwidth improve further. The LTC6560 operates from a single 5V supply and consumes only 90mW. Utilizing the LTC6560's output MUX, multiple LTC6560 devices can be combined to a single output. The LTC6560's fast overload recovery and fast output MUXing make it well suited for LIDAR receivers with multiple APDs. The LTC6560's single-ended output can swing 2V$_{P-P}$ on a 100Ω load. Its low impedance op amp style output has been designed to drive back-terminated 50Ω cables.

PAD COORDINATES

PAD NAME	X-COORDINATE (µm)	Y-COORDINATE (µm)
DNC	417.9	303.24
V_{CCO}	302.9	303.24
DNC	187.9	303.24
V_{CCI}	72.9	303.24
DNC	–72.9	303.24
GND	–187.9	303.24
DNC	–302.9	303.24
GND	–417.9	303.24
IN	–546.21	172.5
V_{REF}	–546.21	57.5
DNC	–546.21	–57.5
DNC	–546.21	–172.5

PAD NAME	X-COORDINATE (µm)	Y-COORDINATE (µm)
GND	–417.9	–303.24
DNC	–302.9	–303.24
GND	–187.9	–303.24
DNC	–72.9	–303.24
V_{CCI}	72.9	–303.24
O_MUX	187.9	–303.24
V_{CCO}	302.9	–303.24
DNC	417.9	–303.24
OUTTERM	546.21	–172.5
GND	546.21	–57.5
GND	546.21	57.5
OUT	546.21	172.5

Note: (0,0) at center of die

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V_{CCI}, V_{CCO} to GND) 5.5V
Voltage (O_MUX) ..... –0.3V to 5.5V
Amplifier Reference Current (V_{REF}) .....±10mA
Amplifier Input
Current (IN) .....±400mA$_{RMS}$ ±2A Transient (10ns)
Amplifier Output Current (OUT, OUTTERM) .....+80mA
Operating Temperature Range
LTC6560 ..... –40°C to 125°C
Storage Temperature Range..... –65°C to 150°C
Junction Temperature ..... 150°C

DICE/DWF AC ELECTRICAL TEST LIMITS

T_A = 25°C, V_{CCI} = V_{CCO} = 5V, O_MUX = 0V, GND = 0V, R_{LOAD} = 100Ω. Output taken from OUT pin.

SYMBOL	PARAMETER	CONDITIONS	MIN		MAX	UNITS
BW	–3dB Bandwidth	200mV$_{P-P,OUT}$ and $C_{IN,TOT}$ = 2pF		220		MHz
R_T	Small Signal Transimpedance	I_{IN} < 2µA$_{P-P}$	63	74	85	kΩ
R_{IN}	Input Resistance	f = 100kHz		236		Ω
R_{OUT}	Output Resistance	f = 100kHz		3		Ω
I_N	Input Current Noise Density	f = 100MHz, $C_{IN,TOT}$ = 2pF		4.3		pA/√Hz
		f = 200MHz, $C_{IN,TOT}$ = 2pF		4.8		pA/√Hz
	Integrated Input Current Noise	f = 0.1MHz to 100MHz, $C_{IN,TOT}$ = 2pF		43		nA$_{RMS}$
		f = 0.1MHz to 200MHz, $C_{IN,TOT}$ = 2pF		64		nA$_{RMS}$
	Channel Isolation	f = 100MHz (O_MUX = High)		–65		dB
$t_{RECOVER}$	Overload Recovery Time	Input Pulse = 1mA		12		ns
t_{OMUX_SWITCH}	O_MUX Switchover Time			50		ns

DICE/DWF DC ELECTRICAL TEST LIMITS

T_A = 25°C, V_{CCI} = V_{CCO} = 5V, O_MUX = 0V, GND = 0V, R_{LOAD} = 100Ω. Output taken from OUT pin.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Pin and V_{REF} Pin						
V_{IN}	Input Bias Voltage	Active Channel Inactive Channel	1.43 0.78	1.55 0.93	1.64 1.38	V V
V_{REF}	Input Reference Voltage	Active Channel Inactive Channel	1.43 1.34	1.55 1.50	1.63 1.67	V V
Offset	$V_{IN} – V_{REF}$	Active Channel	–12		12	mV
OUT Pin						
V_{OUT}	Output Default Voltage	O_MUX = 0V (Output Enabled) O_MUX = 3.3V, Standalone Device	0.83 0.32	1.10 0.60	1.47 0.88	V V
OVR	Output Voltage Range	I_{IN} Current Range = 0µA to –50µA	1.22	1.90	2.58	V_{P-P}
$R_{OUTTERM}$	Internal Series Resistor	Measured at OUTTERM	44	56	70.8	Ω
O_MUX Pin with Internal Pull-Down Resistors						
V_{IL}					0.7	V
V_{IL}			1.5			V
I_{IL}	Pin Voltage = 0.7V		16.9	20.7	26.0	µA
I_{IH}	Pin Voltage = 1.5V		37	47	57	µA
C_{IN}	Input Capacitance			1.5		pF
R_{IN}	Input Resistance		22	29	35	kΩ
Power Supply						
V_S	Operating Supply Range	V_{CCI}, V_{CCO}	4.75	5	5.25	V
$I_{S(VCCI)}$	Input Supply Current	V_{CCI} = 5V	12	16	20	mA
$I_{S(VCCO)}$	Output Supply Current	V_{CCO} = 5V	1.8	2.3	2.8	mA
I_S	Total Supply Current ($I_{S(VCCI)}$ + $I_{S(VCCO)}$)		13.8	18.3	22.8	mA
PSRR(V_{CCI})	Input Power Supply Rejection Ratio	V_{CCI} = 4.75V to 5.25V, V_{CCO} = 5V	21	25		dB
PSRR(V_{CCO})	Output Power Supply Rejection Ratio	V_{CCO} = 4.75V to 5.25V, V_{CCI} = 5V	34	40		dB

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All measurements were conducted in the dark.

PAD FUNCTION

V_{CCO}: Positive Power Supply for the Output Stage. Typically 5V. V_{CCO} can be tied to V_{CCI} for single supply operation. Bypass capacitors of 1000pF and 0.1µF should be placed as close as possible between V_{CCO} and ground. Both V_{CCO} pads are connected within the die.

DNC: Do not connect these pads. Allow them to float.

IN: Input Pad for Transimpedance Amplifier. This pad is internally biased to 1.55V when the channel is active. See the applications section for specific recommendations.

V_{REF}: Reference Voltage Pad for TIA. This pad sets the input DC voltage for the TIA. The V_{REF} pad should be bypassed with a high quality ceramic bypass capacitor of at least 0.1µF. The bypass cap should be located close to the V_{REF} pad. The V_{REF} pad has a Thevenin equivalent resistance of approximately 1.4k and can be overdriven by an external voltage. If no voltage is applied to V_{REF}, it will float to a default voltage of approximately 1.55V on a 5V supply when active.

V_{CCI}: Positive Power Supply for the Input Stage. Typically 5V. Bypass capacitors of 1000pF and 0.1µF should be placed as close as possible between V_{CCI} and ground. Both V_{CCI} pads are connected within the die.

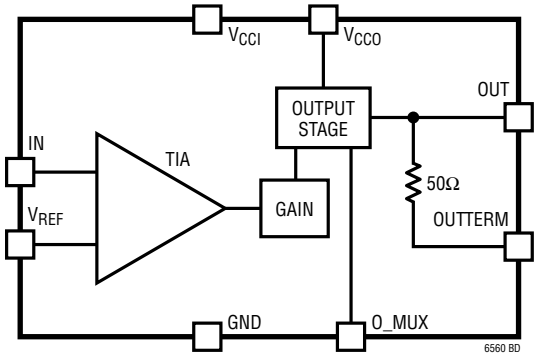
O_MUX: Output MUX is a digital input controlling the output multiplexing function. The pad is functional when multiple LTC6560s are combined at the output. When O_MUX is low, the output is enabled. When O_MUX is high, the input is decoupled from the output. Its default value is 0V. This MUX pad is ineffective unless a second LTC6560 is DC-coupled at the output. See Applications section on how to use O_MUX to expand the channel count with multiple LTC6560's. The O_MUX pad has a 29kΩ internal pull-down resistor.

OUTTERM: TIA Output with an Internal Series 50Ω Resistor.

OUT: TIA Output without an Internal Series 50Ω Resistor.

GND: Negative Power Supply. Normally tied to ground. All GND pads should be down-bonded to a ground plane with minimum length down-bonds.

BLOCK DIAGRAM



Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

I.D.No. 66-13-6560