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APPLICATION NOTE 2039

50W Voltage-Mode Forward Converter Design with the MAX8541

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Abstract: This application note details the design of a 50W, isolated forward converter using the MAX8541 synchronizable, high-frequency, voltage-mode PWM controller. Design procedures for both the power stage and controller are presented, along with actual performance measurements.

The converter delivers 20 amps of load current at an output voltage of 2.5V, and employs synchronous rectifiers for secondary rectification. The input voltage range for the converter is 36VDC–75VDC.

This design is available as an evaluation board. The evaluation board demonstrates how easy it is to implement the features network and telecom applications require. The design methods can easily be adapted to the design of high performance, full featured off-line power supplies.

Key features of the application are:

- *300kHz switching frequency*
- *Programmable input UV/OV Protection*
- *Programmable hiccup mode and latch type current limit protection*
- *Programmable maximum duty cycle clamp with feedforward*
- *Adjustable ramp magnitude of MAX8541 voltage mode controller*
- *Synchronization to external clock*
- *Adjustable current limit threshold*
- *Active low-enable feature for easy turn on and turn off*
- *Internal leading edge blanking on the current sense pin*
- *Output overvoltage protection*
- *Space saving 16-pin QSOP*

Description of Application Circuit Operation

Figure 1 shows the circuit diagram of a 2.5V, 20A, isolated forward converter that uses the MAX8541 voltage-mode controller (U1). At start-up, the total capacitance at the V_{CC} pin is charged through MOSFET Q7 and the parallel combination of resistors R30 and R22 from the DC input voltage V_{IN}. When V_{CC} exceeds the undervoltage lockout threshold of the MAX8541, it goes through the soft-start mode and pulses of gradually increasing duty cycle are applied to the gate drive IC, U8. The MOSFET

Q1 starts to switch the input dc voltage across the power transformer T1, used to provide isolation and to step the input dc voltage down to the required level. (Selection of the power transformer turns ratio is dealt with in the following section.)

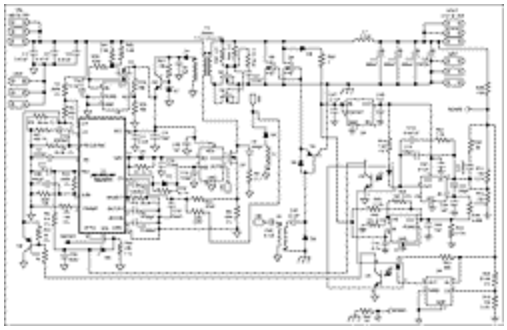


Figure 1. Circuit diagram of 2.5V, 20A, isolated voltage-mode forward converter using the MAX8541.

Since the energy for driving Q1 comes from the capacitance at V_{CC}, the V_{CC} voltage falls. The hysteresis of the MAX8541 undervoltage lockout feature allows this to happen. Pulses on the bias winding of transformer T1 are rectified by D1, regulated and applied to the V_{CC} pin. The rectified and regulated bias circuit voltage builds up and prevents the V_{CC} pin from falling below the undervoltage lockout threshold, and the primary side control continues to operate from the bias winding. The MAX8515 IC U2, is configured to sense the V_{CC} pin and turn off Q7 at a voltage slightly higher than the worst-case startup voltage for U1. This avoids unnecessary power dissipation in Q7, R30and R22.

For power transformer T1, the volt-seconds applied to the primary winding during the "ON" time of Q1 should be balanced by the volt-seconds applied during the "OFF" time, in order to maintain the operating point for the flux in the core. This is achieved by employing D2 and a "demagnetizing winding" whose number of turns equally the primary turns, and is connected with polarity as shown in the schematic. When Q1 turns off, D2 conducts the magnetizing current and the polarity of the applied voltage to the demagnetizing winding causes the magnetizing current to decay to zero. Since the magnitude of voltage applied during the ON and OFF times is identical, the ON time equals the time taken for the magnetizing current to decay to zero and "reset" the core. This limits the duty cycle to a maximum value of 50%, beyond which proper reset of the core will not occur, leading to saturation of the core.

The high frequency switching waveform appearing across the primary of T1 is stepped down by T1 and rectified by synchronous rectifiers Q2, Q8, Q3 and Q9. The forward synchronous rectifiers Q2, Q8 are self-driven from the secondary winding of T1. The freewheeling rectifiers Q3, Q9 are driven with an inverted, suitably delayed version of the gate drive pulses to Q1, using transformer T2. Q5 provides for fast turn off of Q3, Q9. The rectified pulse train is applied to the output L-C filter L1, C11, C12, C13 and C26. The output voltage of the L-C filter is the Average value of the rectified pulse train. For a fixed frequency switching scheme as implemented in the MAX8541, the output voltage is proportional to the "ON" time of the rectified pulse train. The feedback circuit consisting of U4 (LMX321), U5 (LP2980), and U7 (MAX8515) perform the function of regulating the output voltage for load and dc input voltage variations. U4 is a low dropout linear regulator that provides a fixed bias for the secondary side feedback circuit. The output voltage is sensed by resistor divider R12, R11 and is applied to the inverting input of op-amp U4. U7 provides the reference voltage to the non-inverting pin of U4. At start-up the reference is applied through an R-C delay (R36, C29) so as to produce a smooth output voltage start-up waveform. The error between the reference and the output voltage drives the (pins 1, 2) LED portion of optocoupler U3, which couples the error signal across the isolation boundary. The phototransistor (pins 8, 7 of U3) produces a current that depends on the current transfer ratio of U3 and adjusts the voltage at the OPTO pin of U1 to program the duty ratio required to produce the desired output voltage. The primary current is

sensed by means of resistor R8. U6 (MAX8515) provides the output overvoltage protection feature for the converter. When the output voltage exceeds 2.87V, the OUT pin of U6 goes low and drives the (pins 3, 4) LED portion of U3 to turn on Q4 and shutdown the converter. This initiates a fresh start-up cycle for the converter.

Design of Power Stage Components

Transformer Design

Once the required core size for the given power output, switching frequency, flux density, and temperature rise has been established, the primary to secondary turns ratio is estimated. In the typical application circuit the maximum allowed duty ratio is 50% due to the transformer core reset scheme employed. Therefore the primary-secondary turns-ratio $\frac{n_S}{n_P}$ should be based on the lowest operational input voltage, as follows,

$$\frac{n_S}{n_P} \geq \frac{V_{OUT} + (V_{DS} \bullet D_{MAX})}{D_{MAX} \bullet V_{IN\_MIN}}$$

where V_{OUT} is the output voltage, V_{DS} is the voltage drop across the synchronous rectifier, D_{MAX} is the maximum allowable duty ratio (use 0.45 for some safe margin), and $V_{IN\ MIN}$ is the minimum operational input voltage. The design for the actual number of primary turns for low voltage, high current "bricks" for the telecom input voltage range is done by assuming 1 turn for the secondary. This approach is especially true of the "core-on-board" transformers designed for these applications. The turns-ratio from primary winding to primary bias winding is given by,

$$\frac{n_{BIAS}}{n_P} \geq \frac{(9 + V_D)}{V_{INMIN}},$$

where V_D is the voltage drop across the bias winding diode. At the minimum operational input voltage the bias voltage should be at least 9V to power up the MAX8541 and it is a good trade-off between the driving voltage and efficiency.

The reset winding should have the same number of turns of the primary winding, however small gauge wire can be used because the RMS current through the reset winding is very small.

To construct the transformer, one needs to know the RMS currents for both primary and secondary windings. These are given as follows.

$$I_{P\_RMS} = I_{OUT} \bullet \frac{n_S}{n_P} \bullet \sqrt{\frac{n_P}{n_S} \bullet \frac{V_{OUT}}{V_{IN\_MIN}}} \text{ for primary winding rms current, and}$$

$$I_{S\_RMS} = I_{OUT} \bullet \sqrt{\frac{V_{OUT}}{V_{IN\_MIN}}} \text{ for secondary winding rms current,}$$

where I_{OUT} is the maximum output current. Once the above parameters are known, the transformer can be designed. Tightly wound the primary and the reset windings together help to minimize the switching loss due to the leakage inductance at each time when the transformer is reset. Interleaving primary and secondary windings help to increase the coupling and reduce the leakage inductance. However, it may increase the cost if the transformer needs to meet safety requirement. In the typical application circuit

however, a standard off-the-shelf transformer is used. The primary to secondary turns ratio for the selected transformer, ns/np is 0.188.

Output Inductor Selection

There are several parameters that must be examined when determining an optimum inductor value. Input voltage, output voltage, load current, switching frequency and LIR. LIR is the ratio of inductor current ripple to DC load current. A higher LIR value allows for a smaller inductor, but results in higher losses and higher output ripple current. A good compromise between size, efficiency and cost is a LIR of 30%. Once all of the parameters are chosen, the inductor value is determined as follows:

$$L = \frac{V_{OUT} \bullet (V_{SEC} - V_{OUT})}{V_{SEC} \bullet f_S \bullet I_{LOAD(MAX)} \bullet LIR}$$

Where V_{SEC} is the voltage on the secondary side of the transformer at which the maximum ripple voltage is specified and f_S is the switching frequency. Choose a standard value close to the calculated value. For the application circuit, plugging in the values for the above equation, and selecting the nearest standard inductor results in a value of 2.2µH. Lower inductor values minimize size and cost, but they also increase the output ripple and reduce the efficiency due to higher peak currents. On the other hand, higher inductor values increase efficiency, but eventually resistive losses due to extra turns of wire will exceed the benefit gained from lower AC current levels. For any area-restricted applications, find a low-core-loss inductor having the lowest possible DC resistance. Ferrite cores are often the best choice. The chosen inductor's saturation current rating must exceed the expected peak inductor current (I_{PEAK}). Consult the inductor manufacturer for saturation current ratings. Determine I_{PEAK} as:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{V_{OUT} \bullet (V_{SEC} - V_{OUT})}{2 \bullet V_{SEC} \bullet f_S \bullet L}$$

where V_{SEC} is the maximum secondary side voltage.

Output Capacitor Selection

As in any high-frequency power supply, the output filter capacitors must meet very low ESR and ESL requirements. At the 300kHz frequency, the most favorable technologies are ceramic capacitors and polymer tantalum capacitors (POSCAPs). The key selection parameters for the output capacitor are capacitance, ESR, ESL and the voltage rating requirements. It may be noted that capacitance, ESR and voltage rating are also temperature dependent. These parameters affect the overall stability, output ripple voltage and transient response of the DC-DC converter. The output ripple occurs due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL. Calculate the output voltage ripple due to the output capacitance, ESR and ESL as:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)}$$

Where the output ripple due to output capacitance, ESR, and ESL are:

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \bullet C_{OUT} \bullet f_{SW}}$$

$$V_{RIPPLE(ESR)} = I_{P-P} \bullet ESR$$

$$V_{RIPPLE(ESL)} = \frac{I_{P-P}}{t_{ON}} \bullet ESL \quad \text{or}$$

$$\frac{I_{P-P}}{t_{OFF}} \bullet ESL \quad \text{whichever is greater.}$$

And I_{P-P} the peak-to-peak inductor current is:

$$I_{P-P} = \frac{(V_{IN} - V_{OUT})}{f_{SW} \bullet L} \bullet \frac{V_{OUT}}{V_{IN}}$$

The peak values estimated by the above equations for the three components of ripple voltage are not in phase, and therefore cannot be added algebraically. Usually, one of the ripple components dominates the others and can be used for initial capacitor selection. As a rule, a smaller ripple current results in less output voltage ripple. Since the inductor ripple current is a factor of the inductor value, the output voltage ripple decreases with larger inductance. Load transient response depends on the selected output capacitors. During a load transient, the output instantly changes by ESR × I_{LOAD}. Before the controller can respond, the output deviates further, depending on the inductor and output capacitor values. After a short time, the controller responds by regulating the output voltage back to its nominal state. The controller response time depends on the closed-loop bandwidth. A higher bandwidth yields a faster response time, thus preventing the output from deviating further from its regulating value. For the application circuit, 3 x 680µF, POSCAPs are used, each with an ESR of 0.035Ω.

Input Capacitor Selection

The input capacitor (C_{IN}) reduces the current peaks drawn from the battery or input power source. The impedance of the input capacitor at the switching frequency should be less than that of the input source so that high-frequency switching currents are supplied by the input capacitor rather than from the source. The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Non-tantalum chemistries (ceramic, aluminum, or organic) are preferred due to their resistance to power-up surge currents. I_{RMS} is calculated as follows:

$$I_{RMS} = \frac{I_{LOAD}}{N} \bullet \sqrt{\frac{V_{OUT} \bullet N}{V_{IN}} \bullet \left(1 - \frac{V_{OUT} \bullet N}{V_{IN}}\right)},$$

where N is the primary to secondary turns ratio. For the forward converter, V_{IN} is the minimum input voltage for designs where the maximum duty ratio is less than 0.5, and the value of input voltage at which the duty ratio equals 0.5 for designs with maximum duty ratio greater than 0.5. Choose input capacitors that have a higher ripple current rating than the calculated value. For the application circuit, 3 × 0.47µF/100V ceramic caps are used.

Primary MOSFET Selection

The MAX8541 typically drive an n-channel MOSFET power switch. The maximum drain voltage, maximum $R_{DS(ON)}$ and total gate switching charge are the parameters involved in choosing the FET. The maximum gate switching charge is an important factor defining the power consumption, since the product of the switching frequency and the total gate charge is the current consumption of the MAX8541 controller. $R_{DS(ON)}$ is the parameter that determines the total conduction power losses in the switch and

the choice depends on the expected efficiency and the cooling and mounting method. The maximum drain voltage requirements can be different depending on the transformer reset scheme used. For the forward converter show in the application circuit, a simple demagnetizing winding based reset scheme is used, wherein the maximum voltage stress on the MOSFET switch is 2 times the highest input voltage. A 200V MOSFET should be used. The MOSFET should also handle the RMS current associated with the forward topology. The current through the MOSFET is determined as:

$$I_{RMS} = \frac{I_{OUT}}{N} \bullet \sqrt{\frac{V_{OUT} \bullet N}{V_{IN}}}$$

A MOSFET with the lowest total gate charge and the lowest $R_{DS(ON)}$ for the maximum drain voltage expected (plus some safety factor) is the best choice. The choice of package depends on the application, the total power and the cooling methods available. For the Application circuit, based on the above considerations, IRF640 MOSFET: 200V, 18Amps, $R_{DS(ON)}$ = 0.18Ω is chosen.

Secondary Synchronous Rectifier Selection

The typical application circuit uses synchronous rectifier for both the forward and the freewheeling rectifiers on the secondary side. The forward synchronous rectifier is self-driven from the secondary winding, and freewheeling rectifier is driven from a gate drive transformer with signals generated by the controller IC. The voltage rating for the synchronous rectifiers is equal to the maximum secondary voltage plus a margin for spike due to leakage inductance. Switching losses in this topology are not an issue due to the lower drain-source voltages. For synchronous rectifiers, the power dissipation is mainly due to conduction losses. The power dissipation is calculated as:

$$P_D = \left(1 - \frac{V_{OUT} \bullet N}{V_{IN(MAX)}}\right) \bullet I_{LOAD}^2 \bullet R_{DS(ON)}$$

,

for the freewheeling rectifier, and

$$P_D = \left(\frac{V_{OUT} \bullet N}{V_{IN(MAX)}}\right) \bullet I_{LOAD}^2 \bullet R_{DS(ON)}$$

,

for the forward synchronous rectifier. Choose MOSFETs with $R_{DS(ON)}$ such that an acceptable junction temperature is achieved for the estimated power dissipation. Note the synchronous rectifiers' maximum junction temperature depends on the thermal resistance that will be realistically achieved with the device packaging, layout and cooling methods used. IN the application circuit, 2 × IRF7832 (30V, 20A, $R_{DS(ON)}$ = 4mΩ at Vgs = 10V) MOSFETs are used for both forward and freewheeling synchronous rectifiers.

Design of Component Values for the MAX8541 Controller

OV Threshold

The MAX8541 include an over-voltage protection feature that turns off the external MOSFET when the input voltage exceeds the user-set threshold. Connect a resistor divider from the system input to GND with OV connected to the center to set the over-voltage protection trip point. The threshold voltage for OV is 3.021V (typ).

$$V_{IN(MAX)} = \left(\frac{R1 + R2}{R2}\right) \bullet V_{OV}$$

,

where V_{OV} is the OV threshold, $V_{IN(MAX)}$ is the over-voltage trip-point, R1 is the resistor from the system input to OV and R2 is the resistor from OV to GND.

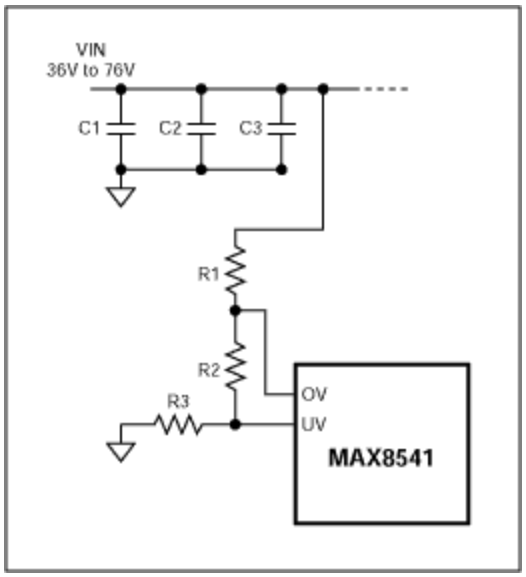
UV Threshold

The MAX8541 also include an under-voltage sensing input. The IC holds the external MOSFET low until UV reaches its threshold (1.25V typ). Once the threshold has been reached, the circuit enters soft-start and brings the output into regulation. Connect a resistor divider from the system input to GND with UV at the center to set the under-voltage protection trip point.

$$V_{IN(MiIN)} = \left(\frac{R1 + R2}{R2}\right) \bullet V_{UV}$$

,

where V_{UV} is the UV threshold, $V_{IN(MIN)}$ is the under-voltage trip-point, R1 is the resistor from the system input to UV and R2 is the resistor from UV to GND.



An alternate method used in the application circuits for setting the over-voltage and under-voltage trip points is demonstrated in **Figure 2**. Use 36.5kΩ for the bottom resistor (R3). R2 and R1 are calculated as follows:

$$R2 = R3 \bullet \left(\frac{V_{OV} \bullet V_{IN(MIN)}}{V_{UV} \bullet V_{IN(MAX)}} - 1\right)$$

$$R1 = \frac{R3 \bullet V_{IN(MIN)}}{V_{UV}} - R2 - R3$$

Where $V_{IN(MIN)}$ is the under-voltage trip point, $V_{IN(MAX)}$ is the over-voltage trip point, V_{UV} is the UV threshold (1.25V typ) and V_{OV} is the OV threshold (3.021V typ). R1 should consist of two equal value resistors in series to protect against single point failure.

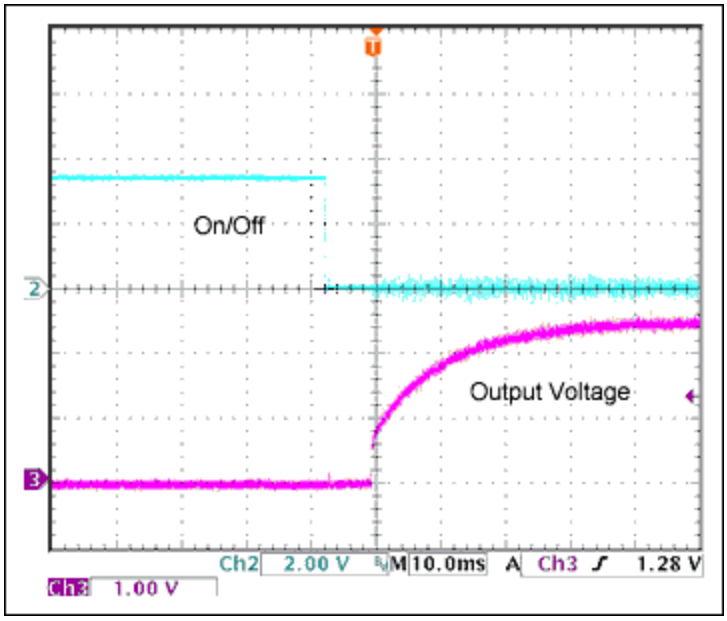


Figure 2. Output voltage at startup using the ON/OFF feature of 8541.

Table 1. Typical specifications of UV/OV and the actual on/off hysteresis of input voltage

UV voltage specs		V_{IN} Off Window (LTP)	V_{IN} On Window (UTP)
MIN	1.083	29.76V	
TYP	1.128	31.00V	
MAX	1.173	32.24V	
MIN	1.200		32.97V
TYP	1.250		34.34V
MAX	1.300		35.70V
OV voltage specs		**V_{IN} Off Window (UTP)**	**V_{IN} On Window (LTP)**
MIN	2.901	79.70V	
TYP	3.021	83.00V	
MAX	3.142	86.32V	
MIN	2.778		76.32V
TYP	2.894		79.50V
MAX	3.010		82.68V

Assume that 1.250V at UV/OV is scaled to 34.34V for 48V bus and 17.17V for 24V bus.

For achieving the input OVP and input UVP trip points as shown in Table 1, the above equations results in R1 = 965kΩ, R2 = 402Ω, and R3 = 36.5kΩ.

Switching Frequency and Synchronization

The MAX8541 oscillator operates in two modes: stand-alone or synchronized (sync). A single input, FREQ/SYNC, doubles as the attachment point for the frequency programming resistor and as the synchronization input. The mode recognition is automatic, based on the signal applied to FREQ/SYNC. In stand-alone mode, an external resistor connected from FREQ/SYNC to GND sets the operating

frequency. A 1.25V source is internally applied to FREQ/SYNC and the oscillator frequency is proportional to the current out of FREQ/SYNC through the programming resistor. The operating frequency is determined as:

$$f_S = (1.25V/R_{FREQ/SYNC}) \bullet (8 \bullet 10^9)$$

The MAX8541 also synchronizes with an external oscillator. Drive FREQ/SYNC with a square wave with a positive pulse width of at least 200ns and a minimum pulse amplitude of 3V plus the V_F of the external diode. The maximum duty cycle of the external signal allowed is 55%. The MAX8541 synchronizes to frequencies between 200kHz and 1MHz, however, the signal must be within ±30% of the frequency set by the external resistor at FREQ/SYNC. Frequency set resistor R4 from the above is calculated to be 32.4kΩ. An R-C filter as specified in the application circuit should be connected across R4 for nose filtering.

Maximum Duty Cycle

Set the maximum duty cycle at the minimum system input voltage ($V_{IN(MIN)}$) connecting a resistor from MAXDTY to GND. The maximum duty cycle is inversely proportional to the voltage at UV. As the voltage on UV increases the duty cycle decreases. The maximum duty cycle is internally limited to 80% at all switching frequencies. The MAXDTY resistor is determined as:

$$R_{MAXDTY} = \frac{D \times (97.6 \times 10^3)}{60}$$

Where D is determined as:

$$D = \frac{V_{OUT}}{V_{IN(MIN)}}$$

The range of valid resistor values for R_{MAXDTY} is from 24.3kΩ to 130kΩ. For the application circuit, a value of 80.6kΩ is chosen to limit the duty ratio to within 50%.

N-Channel MOSFET Driver

The DRV output drives an N-channel MOSFET in low power applications. In high power applications, the gate driver internal to the MAX8541 may not be capable of driving the external MOSFET efficiently and an external gate driver may be required. In this situation, connect DRV to the input of the external gate driver.

Voltage Ramp Setup

The MAX8541 is a voltage-mode device and requires a voltage ramp for duty cycle control. Connect a resistor from PRAMP to GND (R_{PRAMP}) to set the ramp amplitude V_M. The value of R_{PRAMP} is determined by the following equation:

$$R_{PRAMP} = 1.25V \frac{25k\Omega}{V_M},$$

where R_{PRAMP} is in kΩ. The ramp voltage magnitude is independent of frequency. The range of values for R_{PRAMP} is from 14kΩ to 42kΩ. A 14kΩ resistor is chosen for the application circuit to set the

maximum possible ramp amplitude of 2.2V.

Soft-Start

The soft-start feature allows converters built using the MAX8541 to apply power to the load in a controllable soft ramp, thus reducing start-up surges and stresses. It also determines power-up sequencing when several converters are used. Upon power turn-on, SS acts as a current sink to discharge any capacitance connected to it. Once the voltage at V_{CC} has exceeded its lockout value, SS then charges the external capacitor (C_{SS}) allowing the converter output voltage to ramp up. Full output voltage is reached in approximately 440ms/µF. Since the application circuit has a secondary soft start circuit which is used to control the output voltage at start-up, the SS delay is set to be minimal. A delay of 660µs is set using a 1500pf capacitor.

Current-Limit

Two types of current limit schemes can be implemented with the MAX8541. They are the "Hiccup mode" and the Latch mode. The CS signal provides feedback on the current ramp through the main external MOSFET. The voltage on CS is monitored by the MAX8541. The cycle-by-cycle current-limit feature abbreviates the on-time of the external MOSFET in the event that the voltage at CS is greater than the threshold voltage set by ILIM. Set the current-limit threshold using a resistor divider from REF to GND with ILIM connected to the center. The current-limit threshold is determined as:

$$V_{ILIM} = \frac{R26}{R26 + R10} \bullet V_{REF}$$

Where V_{REF} is the 5V reference and R26 and R10 are the external resistors. Use 10kΩ for R16 and vary R26 to change the threshold. For the Application circuit, R26 was adjusted to 205kΩ to set the current limit at 125% of the full load current. To select Hiccup mode, connect capacitors to SKTON and SKTOFF to program the hiccup mode on- and off-time. When a cycle-by-cycle event is detected, the IC charges the capacitor at SKTON. The capacitor continues to charge as long as the CS voltage is greater than the ILIM threshold voltage. Once the voltage on SKTON reaches its threshold voltage, the MAX8541 begins skipping switching cycles for a time determined by the capacitance connect to SKTOFF. Once this time period has elapsed, the IC begins to switch for the time period set by the capacitance connected to SKTON. This process continues until the output short or overload condition is removed. To select latched mode, connect SKTOFF to REF. In this mode, if the hard short or overload exceeds the time period set by the capacitance at SKTON, the output is latched off. To unlatch the output, toggle active-low EN or cycle the input power to V_{CC}.The hiccup mode is chosen for the Application circuit. See the *SKTON and SKTOFF* section below for details on setting the hiccup mode periods.

SKTON and SKTOFF

The capacitance, C_{SKTON}, determine the time period allowed before the short-circuit current-limit initiates. Once the CS voltage exceeds the ILIM threshold, the capacitor at SKTON begins to charge. The capacitor continues to charge until the SKTON threshold voltage is reached or the over-current event is removed. This feature allows for the higher currents required during start-up to bring the IC online. Set C_{SKTON} in order to allow sufficient time for start-up. The required capacitance at SKTON is determined as:

$C_{SKTON} = t_{ON}/10^3$

Where t_{ON} is in ms and C_{SKTON} is in µF. The allowable range for C_{SKTON} is 100pF to 0.01µF.

The capacitance at SKTOFF determines the time period that the external MOSFET is turned off during an over-current event. Once the SKTON time period is exceeded, the SKTOFF capacitor charges. Once V_{SKTOFF} reaches its threshold, the IC begins to switch again. C_{SKTOFF} is determined as:

$C_{SKTOFF} = t_{OFF}/10^3$
Where t_{OFF} is in ms and C_{SKTOFF} is in µF. The allowable range for C_{SKTOFF} is 1000pF to 1µF. For the Application circuit, C_{SKTON} = 0.0047µF and C_{SKTOFF} = 0.068µF are used.

Pull V_{SKTOFF} to V_{REF} through a 10kΩ pull-up resistor to enable the latch-off feature. In this mode, once the SKTON time has elapsed, the IC is latched off. The circuit will remain off until active-low EN is toggled, or the input power is toggled.

Compensation

Since Voltage mode control is employed using the MAX8541 voltage mode controller, the power stage of the forward converter exhibits a double L-C filter pole, along with a zero due to the ESR of the output capacitor. The goal of the compensator design is to achieve a single slope of -20dB/decade with a phase margin greater than 45 degrees at the crossover frequency. To achieve a good dc regulation, a high low- frequency gain is another requirement for the compensator. To achieve this, the compensator should have two zeros, one pole and an integrator. The type 3 compensator scheme readily achieves this. For the Forward converter in the Application circuit, the open loop gain is given by the expression,

$$T(s) = \frac{V_G}{V_M} \frac{(s \bullet C_{OUT} \bullet R_{ESR} + 1)}{\left(1 + s \bullet \left(R_{ESR} \bullet C_{OUT} + \frac{L \bullet I_{OUT}}{V_{OUT}}\right) + \frac{s^2}{\omega_o}\right)} \frac{(s \bullet C14 \bullet R27 + 1)}{(s \bullet C24 \bullet R28 + 1)}$$
$$\bullet \frac{((s \bullet C24 \bullet (R11 + R28)) + 1)}{(s \bullet C15 \bullet R27 + 1)} \frac{G_{OPTO}}{(s \bullet C14 \bullet R11)} \frac{R6}{R14}$$

Where C14 >> C15, G_{OPTO} is the optocoupler gain. $V_G = V_{IN} \bullet n_S/n_P$, $V_M = 2V$ and $\omega_o = \frac{1}{\sqrt{L \bullet C_{OUT}}}$

The frequency that the output poles and zero occur at is determined as:

$$f_{outputpoles} = \frac{1}{2\pi \bullet \sqrt{L \bullet C_{OUT}}} = 2376Hz$$

$$f_{ESRzero} = \frac{1}{2\pi \bullet R_{ESR} \bullet C_{OUT}} = 6690Hz$$

,

where C14, C15, C24, R27, R28 and R11 are the reference designators are used in the MAX8541 Typical Application Circuits. C_{OUT} is the total output capacitance and R_{ESR} is the output capacitors' ESR. Calculate the compensation components using the following method:

First, determine the desired bandwidth (f_{BW}) of the system. The bandwidth (crossover frequency) will determine the speed that the MAX8541 will respond to changes in the output caused by load transients. A bandwidth of 5kHz is chosen for the Application circuit. Unity gain is desired at f_{BW}. Therefore, T(s) at f_{BW} must be equal to 1. Choose C14 = 0.047µF, s = $2\pi \times f_{BW}$ and set the loop gain to unity in equation for loop gain T(s) to determine R11. For a single active pole at the crossover frequency,

$$R11 = \frac{n_s}{n_p} \bullet \frac{V_{IN}}{V_M} \bullet G_{OPTO} \bullet \frac{1}{2\pi \bullet f_{BW} \bullet C14} \bullet \frac{R6}{R14}$$

,

where n_P is the number of primary turns, n_S is the number of secondary turns, and G_{OPTO} is the gain of

the optoisolator used. The value for R11 is obtained as 6.85kΩ from the above equation. Use 6.81kΩ, the nearest standard value.

Place the R27 zero to cancel one of the two output poles. R27 is found to be 1.5kΩ using the following equation:

$$R27 = \frac{1}{2\pi \bullet C14 \bullet f_{outputpoles}}$$

Solve equations (1) and (2) and calculate R28 to be 3.75kΩ. Choose R28 = 3.9kΩ.

$$f_{outputpoles} = \frac{1}{2\pi \bullet (R11 + R28) \bullet C24} \qquad \text{Eq. 01}$$

$$f_{ESRzero} = \frac{1}{2\pi \bullet C24 \bullet R28} \qquad \text{Eq. 02}$$

Either equation (1) or (2) may be used to solve for the value of C24 which is found to be 4000pf. Use the nearest higher standard value of 4700pf.

Design the value of C15 so as to place a pole in the compensator at half the switching frequency to roll off the gain to a small value at the switching frequency.

$$C15 = \frac{1}{\pi \bullet R27 \bullet fs}$$

A value of 680 pf was used for C15. The above method though simple, predicts a lower crossover frequency, since it assumes perfect cancellation of the system poles and zeros by the controller. In practice, it is desirable to place at least one of the controller zeros at a lower frequency than the output L-C filter double pole to soften the abrupt 180 degree phase transition of the L-C filter. When this is done, the actual crossover frequency measured may be higher than desired. When the actual frequency response was measured using a network analyzer, the value of R11 was changed to 15K to reduce the crossover frequency to the desired value. Again, R28 was changed to 3k during testing in order to allow the ESR zero to boost the phase to account for optocoupler phase lag not considered in the foregoing calculations. The final values for the compensator are R11 = 15kΩ, R27 = 1.5kΩ, R28 = 3kΩ, C14 = 0.047µF, C15 = 680pf and C24 = 4700pf.

Output Overvoltage Protection

Output overvoltage protection is implemented by sensing the overvoltage condition using the MAX8515 (U6) as a comparator, coupling the fault signal through an optocoupler (U3), and pulling down the UV input of the MAX8541. The MAX8541 turns off the drive pulses and goes through a fresh startup cycle repeatedly till the overvoltage condition is removed.

Layout Guidelines

All connections carrying pulsed currents must be very short, be as wide as possible and have a ground lane behind them whenever possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents in high frequency switching power converters. In the development of prototyping process, multipurpose boards, wire wrap and similar constructive practices are not suitable for these types of circuits; attempts to use them will fail. Instead, used milled PC boards with a ground plane or equivalent techniques.

Current loops must be analyzed in any layout proposed and the internal area kept to a minimum to reduce radiated EMI. The use of automatic routers is discouraged for PC board layout generation in the board area where the high-frequency switching converters are located. Designers should carefully review the layout. In particular, pay attention to the ground connections. Ground planes must be kept as intact as possible. The ground planes for the power section of the converter should be kept separate from the logic ground planes except for a connection at the least noisy section of the power ground plane. The power-line filter capacitor and the ground return of the power switch or current sensing resistor must be close together. All ground connections must resemble a star system as much as practical.

Thermal management is another important issue to be considered in the design of converters such as that described above. The temperature rise of the components is a strong function of the cooling methods and packaging techniques used. Forced cooling is definitely required for the Application circuit to deliver full power reliably.

Measurements on the MAX8541 EVKIT

Some important measurements taken on the MAX8541 evaluation kit are presented here.

They are:
1. Converter Efficiency (**Figure 3**)
2. Transient Response (**Figure 4**), and
3. Output voltage at startup (Figure 2) employing the ON/OFF feature of the MAX8541.

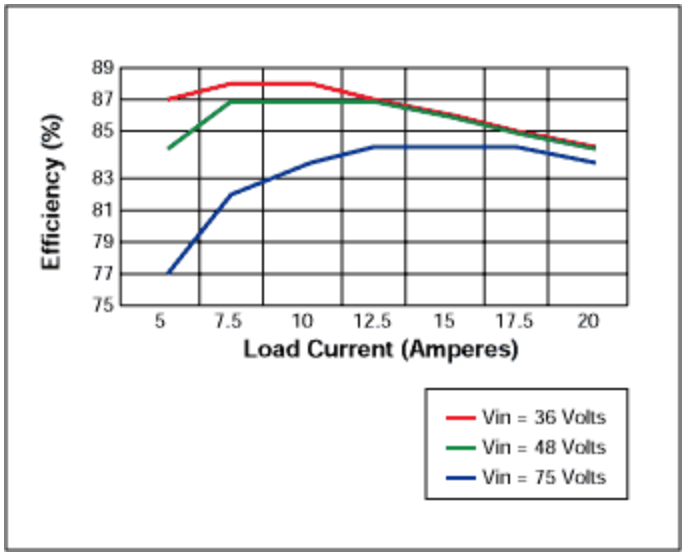


Figure 3. Converter efficiency vs load current.

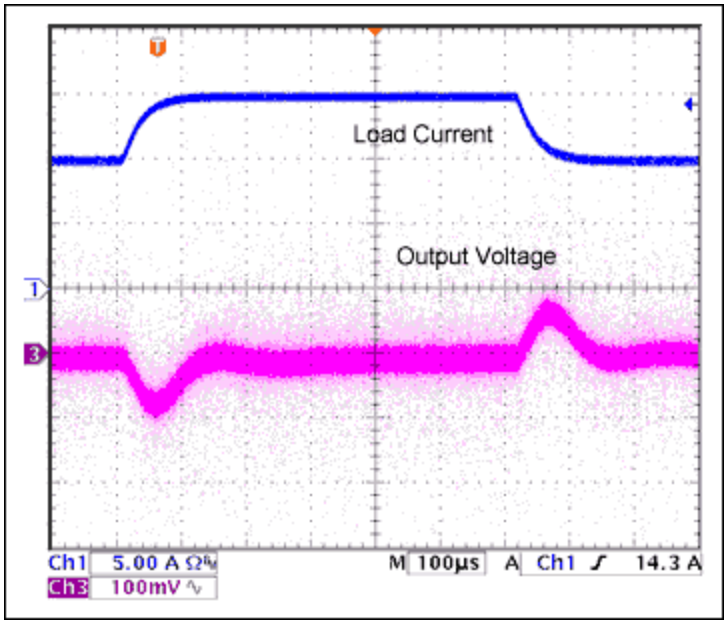


Figure 4. Output voltage deviation for step load increase and decrease. Load current slew rate is approximately 0.1/µS.

Summary

The design of a 2.5V, 20A converter using the MAX8541 voltage mode controller has been discussed, and a typical application circuit along with the Bill of materials for the same has been presented. Features particularly desirable for the network and telecom industry incorporated in the MAX8541 have been demonstrated in the Application circuit.

Bill of Material:

Components	Functions	Part Number
C1, C2, C3	Input filtering capacitor	0.47µF 100V X7R cer cap (1812), TDK, C4532X7R2A474M
C4	V_{CC} filtering capacitor	10µF/16V X5R cer cap (1210), Taiyo Yuden EMK325BJ106MN
C5	Soft start capacitor	1500pF/50V X7R cer, (0603), Murata, GRM188R71H152KA01B
C6	Decoupling for U2	0.1µF/25V, cer, X7R, (0603), GRM188R71E104KA01B
C7	V_{CC} bypass capacitor	0.1µF/50V X7R cer cap (0805), Taiyo Yuden UMK212BJ104KG
C8	Bias filtering capacitor	1µF/25V, X7R, Taiyo Yuden, TMK316BJ105ML
C9	Snubber capacitor	100pF/630V, Murata, GHM1030R101K630
C10	Filter for MAXDTY pin	2200pF/50V X7R cer, (0603), Murata, GRM188R71H222KA01B
C11, C12, C13	Output filtering capacitor	680µF/4V/35mΩ, 4TPB680M, POSCAP, Sanyo
C14	Loop compensation capacitor	.047µF/25V, cer, X7R, (0603), GRM188R71E473KA01B
	Loop compensation	

C15	capacitor	680pF, ceramic, X7R, (0603), GRM1885C1H681JA01B
C16	Decoupling capacitor	0.1µF/25V, cer, X7R, (0603), GRM188R71E104KA01B
C17	REF bypass capacitor	1µF/10V, Taiyo Yuden, LMK107BJ105MA
C18	Time delay capacitor	120pF/50V, COG, ceramic, (0603), GRM1885C1H121JA01B
C19	Time delay capacitor	220pF/50V, COG, ceramic, (0603), GRM1885C1H221JA01B
C20	Gate drive Xfmr Cap	0.1µF/50V X7R cer cap (0805), Taiyo Yuden UMK212BJ104KG
C21	Snubber capacitor	1500pF/50V, X7R, cer, (0603), GRM188R71H152KA01B
C22	ON time capacitor at hiccup mode	4.7nF/50V, X7R ceramic, (0603), GRM188R71H472KA01B
C23	OFF time capacitor at hiccup mode	0.068µF/25V, cer, (0603), GRM188R71E683KA01B
C24	Compensator cap	4.7nF/50V, X7R, ceramic, (0603), GRM188R71H472KA01B
C25	Gate drive Xfmr Cap	0.1µF/ X7R ceramic (0805), Taiyo Yuden UMK212BJ104KG
C26	Output filter Capacitor	open
C27	Bypass Cap for sec bias	0.1µF/25V, X7R, cer, (0603), GRM188R71E104KA01B
C28	Bypass Cap for sec bias	1µF/10V, Taiyo Yuden, LMK107BJ105MA
C29	Delay cap for sec Ref	1µF/10V, Taiyo Yuden, LMK107BJ105MA
C30	Stabilizing cap for U7	1µF/10V, Taiyo Yuden, LMK107BJ105MA
C31	capacitor	150pF/ 50V, X7R ceramic, (0603), GRM1885C1H151JA01B
C32	capacitor	Open (0603)
C33	Decoupling Cap for Driver	1µF/16V, X7R, (0805), TDK, C2012X7R1C105M
C34	capacitor	2200pF/50V X7R cer, (0603), Murata, GRM188R71H222KA01B
C35	Filter for current lim Ref	120pF/50V, COG, ceramic, (0603), GRM1885C1H101JA01B
C36	Filter for feedback signal	Open (0603)
C37	Decoupling capacitor	0.1µF/25V, cer, X7R, (0603), GRM188R71E104KA01B
D1	Rectifying diode	80V/100mA Schottky diode, Panasonic MA111CT, Digikey MA111CT-ND, (S-Mini)
D2	Ultrafast rectifier diode	200V/ 1 A, On semiconductor MURA120T3, SMA
D3	Zener diode	BZX399-1V8, 1.8 volt zener, Phillips semiconductor, (SOD-323)
D4	Diode	IN4148WS, General Semiconductor, (SOD-323)
D5	Diode	IN4148WS, General Semiconductor, (SOD-323)
D6	Diode	IN4148WS, General Semiconductor, (SOD-323)
D7	Zener diode	12V Zener diode, Panasonic MA3120CT
D8	Diode	IN4148WS, General Semiconductor, (SOD-323)

D9	Diode	IN4148WS, General Semiconductor, (SOD-323)
U1	PWM Control IC	MAX8541, Voltage mode, 16 PIN QSOP, MAXIM
U2	OVP comparator	MAX8515, SC-70, MAXIM
U3	Dual Opto-coupler	Dual 70V CTR Photo-transistor (SO-8), Fairchild MOCD217
U4	Secondary control IC	LMX321, SOT223-5, MAXIM
U6, U7	Shunt regulator	MAX8515, SC-70, MAXIM
U8	Gate driver	Dual 2A driver, Texas Instruments #UCC27324D, SO-8
U5	Sec bias LDO	LP2980, 5 volts LDO, National semiconductor.
L1	Output inductor	2.2µH/32A, HC2 2R2, Coiltronics
Q1	Primary switch	200V/18A N-MOSFET, IR, IRF640NS, (D2PAK)
Q2	Forward sync rectifier	30V/20A, N-MOSFET, IR, 2xIRF7832, (SO-8)
Q3, Q9	Freewheeling sync rect	30V/20A, N-MOSFET, IR, 2xIRF7832W, (SO-8)
Q4	PNP transistor	40V 200mA PNP (S0T-23), Fairchild MMBT3906
Q5	PNP transistor	40V 200mA PNP (S0T-23), Fairchild MMBT3906
Q6	NPN transistor	40V/200mA NPN (SOT89), Central Semi, CXT3904
Q7	N-MOSFET	IRLM110A, SOT223, 100V
Q8		open
R1	Voltage divider resistor	965kΩ 1%, (0805)
R2	Voltage divider resistor	402Ω 1%, (0603)
R3	Voltage divider resistor	36.5kΩ, 1%, (0603)
R4	Frequency set resistor	32.4kΩ, 1%, (0603)
R5	SCOMP resistor	30.9kΩ, 1%, (0603)
R6	Feedback resistor	3kΩ, 1%, (0603)
R7	Time delay resistor	1kΩ, 1%, (0603)
R8	Current sense resistor	40mΩ, 1%, WSL-2010 .04 1% B43, VISHAY DALE
R9	Snubber resistor	51.1Ω, 5%, (1206)
R10	Current limit resistor	205kΩ, 1%, (0603)
R11	Feedback resister divider	15kΩ, 0.5%, (0603)
R12	Feedback resister divider	15kΩ, 0.5%, (0603)
R13	Feedback resister divider	10kΩ, 0.5%, (0603)
R14	Opto current limit resistor	1.2kΩ, 1%, (0603)
R15	Base resistor for OVP Xstr.	1kΩ, 5%, (0805)
R16	Snubber resistor	51.1Ω, 5%, (1206)
R17	Pull up for OVP xstr	1kΩ, 5%, (0603)
R18	Time delay resistor	1kΩ, 1% (0603)
R19	Maximum duty resistor	80.6kΩ, 1%, (0603)

R20	Resistor	100kΩ, 5%, 0603
R21	Resistor	10kΩ, 5%, 0603
R22, R30	Resistor	2.3kΩ, 5%, (2010), 0.5W
R23	OVP Opto current limit resistor	330Ω, 5%, (0603)
R24	Resistor	28kΩ, 5%, (0603)
R25	Resistor	10kΩ, 5%, (0603)
R26	Current limit divider resistor	10kΩ, 1%, (0603)
R27	Compensator resistor	1.5kΩ, 1%, (0603)
R28	Compensator resistor	3kΩ, 1%, (0603)
R29	Resistor	37.9kΩ, 1%, (0603)
R30	Resistor	20kΩ, 1%, (0603)
R31	Resistor	10kΩ, 5%, (0603)
R32	Secbias resistor	1Ω, 5%, (0603)
R33	Resistor	5.11kΩ, 5%, (0603)
R34	Resistor	12kΩ, 0.5%, (0603)
R35	Resistor	11kΩ, 0.5%, (0603)
R36	Resistor	9.09kΩ, 5%, (0603)
R37	Resistor	5.11kΩ, 5%, (0603)
R38	Resistor	open
R39	Resistor	100Ω, 5%, (0603)
R40	Resistor	10Ω, 5%, (0603)
R41	Resistor	2.2Ω, 5%, (1206)
R42	Resistor	2.2Ω, 5%, (1206)
T1	Transformer	200µH 1:1:0.313:0.188 turn Transformer (12pin Gull Wing) Copper Electronics, CTX03-16222
T2	Isolation Transformer	MIDCOM 31264R

Related Parts	
MAX8541	Synchronizable, High-Frequency Current- and Voltage-Mode PWM Controllers for Isolated Supplies

More Information
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