Flexible Bandwidth 4 mA to 20 mA Current Input with Easy HART Compatibility

by Michal Brychta and Derrick Hartmann, Analog Devices, Inc.

4 mA to 20 mA analog current loops are commonly found in both process plants and factory environments. While the basic signaling is the same in both environments, the bandwidth requirements differ significantly. Factory control systems may require loop bandwidths of 100 Hz from position and displacement sensor. On the other hand, typical process control systems only require updated rates of a few hertz, and are often HART enabled. The HART (highway addressable remote transducer) protocol allows for bidirectional 1.2 kHz/2.2 kHz FSK (frequency shift keying) modulated digital communication, over traditional analog 4 mA to 20 mA current loops. Designing a 4 mA to 20 mA input that caters to both scenarios can be challenging. This article outlines a method to greatly simplify such a design.

The circuit diagram in Figure 1 shows a traditional approach to implementing a HART enabled analog input.

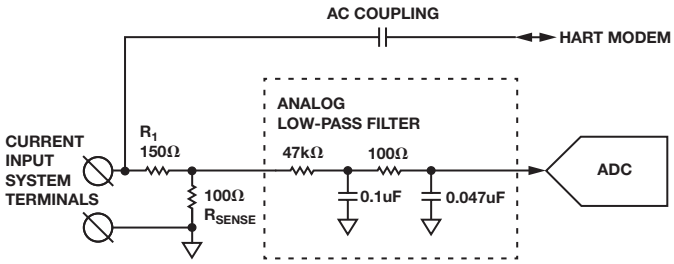

Figure 1. HART enabled input with passive filter.

R_1 and R_{SENSE} provide a 250 Ω system terminal impedance. The HART FSK signal is ac-coupled from there to a HART modem. The 4 mA to 20 mA analog signal is converted by a precision 100 Ω R_{SENSE} resistor to a 0.4 V to 2 V voltage signal. The analog low-pass filter then attenuates the HART FSK component from the analog signal before passing it to an ADC. The second order low-pass analog filter has a bandwidth of 25 Hz and –40 dB/decade roll-off.

This circuit is compliant with HART specifications, and provides attenuation of a HART FSK signal to level over –60 dB below the 4 mA to 20 mA full scale, ensuring less than 0.1% disturbance of the 4 mA to 20 mA analog input by the HART FSK communication.

On the other hand, this analog low-pass filter takes almost 70 ms to settle within 0.1% after a full-scale step on the system input. The long settling time and low bandwidth would not be suitable in the systems where fast operation is required and HART communication is not needed. The analog filter could indeed be bypassed, but that would require additional analog circuitry, such as switches or multiplexers.

Figure 2 shows an alternative approach to the HART enabled analog input.

Similarly to the previous circuit, the HART FSK signal is ac-coupled from a 250 Ω input impedance, and the 4 mA to 20 mA analog signal is converted by a precision 100 Ω R_{SENSE} resistor to a 0.4 V to 2 V voltage signal. In this circuit, however, a considerably lighter low-pass filter limits the bandwidth of the signal to about 27 kHz, just to provide system immunity and electro-magnetic compatibility (EMC). The filter settles to 0.1% in 40 μs after a full-scale step on the system input.

This signal is passed to a Σ-Δ ADC with a built-in digital filter—for example, the AD7173 from ADI. The digital filter can be programmed for either slower operation and optimum HART FSK signal rejection, or fast operation when fast analog input functionality is required.

The AD7173 digital filter has many modes of operation. One of the modes suitable for rejecting HART FSK signal is a sinc3 filter with notch set to 400 Hz, or submultiples, which provides a deep filter notch at the lower HART FSK frequency of 1.2 kHz, and significant attenuation at the higher frequency of 2.2 kHz. The graph in Figure 3 shows the frequency response of this digital filter and its comparison with the analog filter from Figure 1.

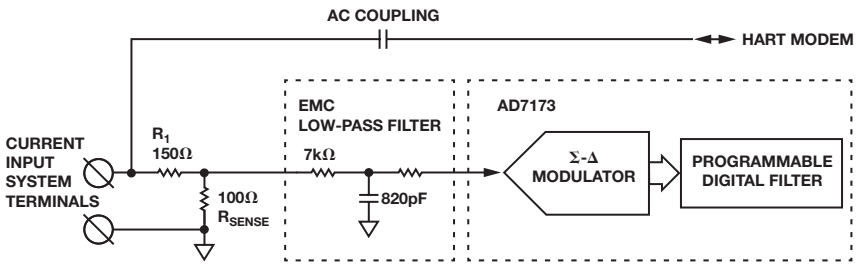

Figure 2. HART enabled, flexible bandwidth input.

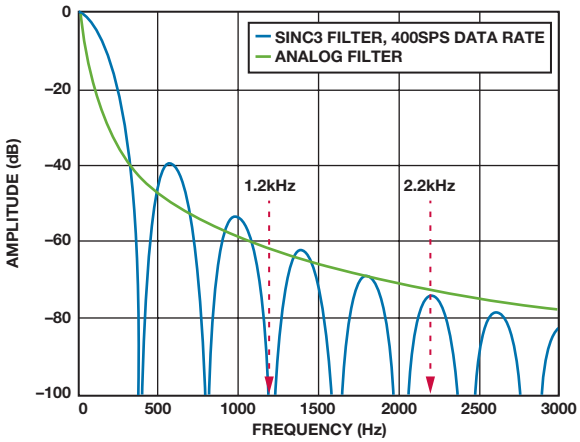

Figure 3. HART enabled input with passive filter.

Unfortunately, the real world is not that simple. When a complete message is sent via HART, the HART FSK modulated signal spectrum does not only contain energy at the base modulation frequencies, but will also contain components between, below, and above the 1.2 kHz and 2.2 kHz carrier.

Figure 4 shows a typical spectrum of the HART FSK message on the ADC input, as well as the spectrum when attenuated by the sinc3 filter with a 400 Hz notch. In this case the master is sending HART command 3 and a slave is responding to that command.

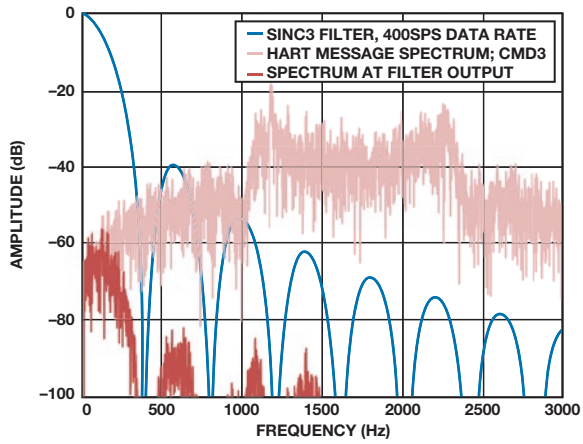

Figure 4. HART message spectrum.

From this figure it is apparent that a portion of the HART message, especially at the lower frequencies, can still be present in the analog-to-digital output data. That said, the digital filter settings can easily be altered to set the right balance between the 4 mA to 20 mA input speed and rejection of the HART FSK signaling.

Figure 5 shows the system performance, measured as a percentage error with respect to the 4 mA to 20 mA full scale, vs. the system speed for the analog filter (shown in Figure 1) and the sinc3 digital filter (shown in Figure 2).

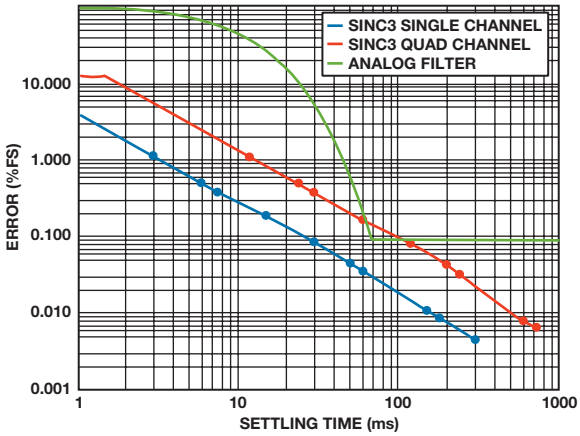

Figure 5. Sinc3 filter vs. analog filter.

The analog filter is fixed in hardware and has a fixed settling time. For fast changing analog signals on the system input, the analog filter output error is dominated by its slow settling. For example, if the system input was changing full scale every 40 ms, the filter output would not settle closer than 1% of the correct value. For the slow input signals, the analog filter output error is dominated by its ability to reject the low frequency components of the HART FSK signaling. This error was measured as approximately 0.09% of the 4 mA to 20 mA full scale for a typical HART command 3 message.

On the other hand, the digital sinc3 filter's settling time is a parameter set by the user, and the error on the filter output caused by the HART FSK signaling corresponds to the filter setup. For example, the sinc3 filter with the 400 Hz notch discussed previously corresponds to a settling time of 7.5 ms, and when communicating with the HART command 3, the measured disturbance in the analog-to-digital result was less than 0.4% of the 4 mA to 20 mA full scale. In a system with four analog inputs, the sinc3 filter is sequentially switched between the channels. The same sinc3 filter with 400 Hz notch now needs $4 \times 7.5 = 30$ ms to scan all four channels. That is why the plot shows the same ~0.4% error at 30 ms for the 4-channel system.

For a more accurate 4 mA to 20 mA input, the sinc3 filter can be set to 30 ms settling, which corresponds to 100 Hz notch and it rejects the HART signal to less than 0.1% of the full scale. If speed is more valued in the system, the sinc3 filter with 6 ms settling (~500 Hz notch) still rejects the HART communication signal below 0.5% of the 4 mA to 20 mA full scale. And if the speed is the only requirement and HART communication is not needed, the AD7173 used in our example can sample over 31 kSPS with a settling time of 161 μs per channel.

In conclusion, the traditional analog low-pass filter is easier to understand, and, for the price of a few more components per channel on the board, in some cases may give a better analog input performance when implemented in a multichannel system. On the other hand, the digital sinc3 filter integrated on a Σ-Δ ADC enables significant flexibility, which can be offered all the way down to the end system user. The digital solution requires less hardware, and if setup properly, its performance in filtering HART FSK signaling is considerably better than the analog solution in single channel systems and comparable or better in up to 4-channel systems.

About the Author

Michal Brychta is a senior staff system applications engineer, with focus on industrial automation. He works for the Industrial Automation Group, Analog Devices, and is based in Limerick, Ireland. Prior to his current role, Michal was a product applications engineer supporting Analog Devices Σ-Δ converters, and before that he worked for 10 years as an instrumentation and industrial system design engineer. Michal holds his master's degree in electronic engineering from the Brno University of Technology in Czech Republic. He can be reached at *michal.brychta@analog.com*

Derrick Hartmann is a system applications engineer in the Industrial Automation Group, Analog Devices. He is based in Wilmington, MA. Prior to his current role, Derrick was a product applications engineer supporting the Analog Devices industrial DAC portfolio. Derrick holds a degree in electronic engineering from the University of Limerick, Ireland. He can be reached at *derrick.hartmann@analog.com*.

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Analog Devices, Inc.
Worldwide Headquarters
Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA 02062-9106
U.S.A.
Tel: 781.329.4700
(800.262.5643,
U.S.A. only)
Fax: 781.461.3113

Analog Devices, Inc.
Europe Headquarters
Analog Devices, Inc.
Wilhelm-Wagenfeld-Str. 6
80807 Munich
Germany
Tel: 49.89.76903.0
Fax: 49.89.76903.157

Analog Devices, Inc.
Japan Headquarters
Analog Devices, KK
New Pier Takeshiba
South Tower Building
1-16-1 Kaigan, Minato-ku,
Tokyo, 105-6891
Japan
Tel: 813.5402.8200
Fax: 813.5402.1064

Analog Devices, Inc.
Asia Pacific Headquarters
Analog Devices
5F, Sandhill Plaza
2290 Zuchongzhi Road
Zhangjiang Hi-Tech Park
Pudong New District
Shanghai, China 201203
Tel: 86.21.2320.8000
Fax: 86.21.2320.8222

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