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FUNDAMENTAL PRINCIPLES BEHIND THE SIGMA-DELTA ADC TOPOLOGY: PART 2



The AD717x page on *analog.com* provides details of the complete family, which includes information on the AD7172-2, AD7175-2, AD7172-4, AD7173-8, and the AD7175-8. These precision ADCs comes with a fully integrated analog signal chain with true rail-to-rail analog input and reference input buffers. The family offers multiple input channel counts with pin-to-pin upgrades for either speed of conversion or for lower noise or lower power alternatives. AD7175-2 and AD7175-8 provide the fastest outputs and lowest noise. AD7177-2 offers a 32-bit resolution output. AD7172 and AD7173 provide the lowest power options.

The AD7175-2 includes an extremely useful software tool to help with its evaluation. Eval+ is a single piece of software downloadable from the ADI website, which can be used to configure, analyze, and select the ADC with



Figure 2. Configuration tab of the AD7175-2 Eval+ software in functional model evaluation mode.

or without hardware. The software, running with hardware, will operate as per the standard evaluation board. Without hardware, a functional model of the ADC runs in the background, allowing the user to establish the best operating configuration for their end application.



Figure 1. AD7175x Σ - Δ ADC family; AD7175-2 block diagram and noise performance.

Table 1. AD717x Family Overview, Showing the Channel Count Options Available and the Pin-for-Pin Alignment of Family Members

		AD717x F	24-lead TSSOP	5 × 5 32-lead LFCSP	6 × 6 40-lead LFCSP	
	Noise-Free Bits (Full Speed)	Modulator (mA)		-2	-4	-8
AD7175 250 kSPS	17.2	8.4	Fast, low noise, true rail-to-rail buffers, 5 V supply	•		•
AD7172 32 kSPS	17.2	1.5	Low power, true rail-to-rail buffers, 5 V or 3 V supply	•	•	
AD7176 250 kSPS	17.3	8	Fast, low noise, unbuffered, 5 V supply	•		
AD7173 32 kSPS	17.5	1.5	Low power, buffered input, 5 V or 3 V supply			•
AD7177 10 kSPS	19.1	8.4	Fast, low noise, 32-bit true rail-to-rail buffers, 5 V supply	•		

Eliminating the Σ - Δ ADC Quantization Noise: Noise and BW Considerations

The AD7175 ADC will be used to illustrate how the quantization noise of Σ - Δ ADCs can be eliminated using digital filtering. Trade-offs in noise/ input bandwidth and settling time come into focus.

Figure 4 shows where the raw modulator noise is plotted from vs. the log of frequency for the AD7175 device from dc to FMOD/2 (or 4 MHz). The AD7175 modulator samples at an effective rate of 8 MHz (FMOD). The modulator is a MASH style that is designed to give an 80 dB/decade slope to the modulator noise. The thermal noise of the circuit sets the in-band noise floor before getting to the point of the frequency axis where the modulator noise begins to ramp. The plot illustrating the low noise floor gives an insight into the high dynamic range capability of the ADC for low bandwidth signals. This dynamic range and the ability of the AD7175 to push this noise floor down translates into improved sensitivity for the user, which is particularly useful when acquiring low amplitude signals in the application.

The minimum oversampling ratio of the ADC, the digital filter order, and the corner frequency all contribute to ensuring that the quantization noise is not the limiting factor for the ADC noise. To filter the noise, the envelope of the filter needs to be able to attenuate, with sufficient roll-off to deal with the rate of increase of the magnitude quantization noise.

The minimum oversampling ratio of the AD7175 is \times 32, so given the 8 MHz FMOD, the maximum output data rate offered is 250 kHz.

The AD7175 offers a number of different filter types selectable by the user. The theory behind the operation of a digital filter operation is described by comparing the sinc5 + sinc1 and sinc3 filters in different scenarios.



Figure 3. AD7175 modulator output spectrum dc to FMOD/2 with the sinc5 + sinc1 and decimate by 32 (effectively a sinc5 dc response) overlaid.

At a 250 kHz ODR, the AD7175 sinc5 + sinc1 is configured directly as a sinc5 path with a -3 dB frequency of \sim 0.2 × ODR (50 kHz). The sinc5 filter has an attenuating envelope of -100 dB per decade. This means the sinc5 filter attenuation and roll-off is more than sufficient to eliminate the modulator noise, as shown in Figure 3.

In contrast, changing to sinc3 at 250 kHz ODR, the attenuation and roll-off are not sufficient to eliminate the modulator noise. The data sheet noise numbers at 250 kHz and 125 kHz ODR show this fact. Only when the data rate is set to 62.5 kHz and below does the sinc3 response fully filter the quantization noise from the ADC result.

Beyond filtering quantization noise, the digital filter can be used to trade off input bandwidth for lower noise. This is done by increasing the decimation rate. In the case of the sinc5 + sinc1 filter, increasing the oversampling ratio means that the initial fifth-order sinc filter becomes averaged. The averaging of the initial result enables the user to choose from a range of different output data rates, speed, and bandwidth improving noise performance (shown in Figure 5) by the sinc5 and subsequent sinc5 + sinc1 averages to improve the noise performance. Averaging the sinc5 result introduces first-order notches at the output data rate and multiples of that rate, which are compound with the overall sinc5 envelope. The notches in the sinc style filter have traditionally been used to reject interferers at known freque cies by strategically setting the data rate to coincide with the interferer frequency. A classic example of this is in the 50 Hz and 60 Hz rejection of the line frequency.



Figure 4. AD7175-2 sinc5 + sinc1 filter: adjusting the input bandwidth by changing the decimation rate of the ADC.



Figure 5. AD7175-2 sinc5 + sinc1 filter - noise vs. ODR plot.

The sinc style filter is a moving average filter with a sin(x)/x profile, so it is commonly referred to as a sinc filter. The filter is made up of a series of integrators and a switch that operates as the decimator, followed by a series of differentiators. This is a finite impulse response (FIR) type of filter. It exhibits a known and finite linear phase response to a step change at the input. As the output data rate and integer multiples of this rate, deep notches occur with attenuating signals within the notch.



Figure 6. Frequency domain comparison of the different orders of sinc filters: sinc5 vs. sinc3.

Figure 6 shows the comparison of the third-order and fifth-order sinc filters, both running with a decimation rate of 32 for the AD7175. In this case, both filters will provide conversion data at an output rate of 250 kHz. The order of the filter determines both the roll-off and the -3 dB frequency. A sincP filter will sit under a frequency response envelope of $-P \times 20$ dB/decade. The steeper roll-off gives a lower -3 dB frequency. The major trade-off between different orders of filters is in the settling time of the filter, which has different effects on the end measurement application depending on the scenario.

Filter Settling Time

As the digital filter processes a moving average of the data stream from the Σ - Δ modulator, there is an associated settling time. The delay is fixed for any FIR filter, but differs for each sinc filter order. The delay is typically described by two terms: group delay and settling time. The group delay describes the delay between the analog signal being present at the input to when it is seen at the digital output. For a single tone sine wave, for instance, it is the time between the voltage peak of the sine wave existing at the analog input and the same peak appearing at the digital output.

The settling time is the full averaging time of the digital filter. If there were a step at the analog input, it takes the full settling time of the filter until the data output from the ADC has no correlation with that previous step at the input. Other delays can exist, such as the computation time of the filter. For AD7175 family, the first conversion will have a longer settling time or settling after coming out of standby can also incur a delay due to an initial computation cycle of 1/ODR. Any delays in addition to the settling time of the filter can vary depending on the converter selected, so be mindful when reading ADC data sheets.



Figure 8. Multiplexed ADC, sinc3 filter, and three conversion cycles-fully settled data.

The filter settling time effect is best shown by comparing a single Σ - Δ ADC scenario with that of a multiplexed Σ - Δ ADC. The settling time of the digital filter heavily impacts the rate at which the user can cycle the multiple input channels while keeping each channel result independent.



Figure 7. Single ADC input, sinc5, and five conversion output cycles.

Why do you need to wait the full settling time to give an independent result? Let's look at the digital filtering for a single ADC with a single input source. The data from the modulator Σ - Δ ADC is passed at a rate of FMOD to the digital filter (as described in Figure 5) with each sample passed through the moving average filter. Depending on the order and style, the filter weighs each sample differently over the conversion time period (set by the filter decimation rate) as shown in Figure 7. Input Sample 0 and subsequent samples are discrete modulator output results separated by a single period of the modulator clock. The y-axis scales the weighing attributed by the digital filter to each sample. The shape of this weighing is the time domain representation of the low-pass digital filter. The output data rate of this situation is 250 kHz (8 MHz/32 = FMOD/decimation rate). The time between the data ready signals (vertical dashed lines in each of the different colors) is 4 μ s. The ADC is set up to run with the sinc5 + sinc1 filter with a decimation rate of 32. All five conversion outputs have some overlap in the modulator inputs that define the filter output, thus, none

are independent from each other. For a single ADC input, each conversion result shares inputs from the modulator but the filter weighs each of these modulator outputs differently.

For the multiplexed input case, the modulator data provided to create each conversion output must be independent for each channel. The full settling time of the filter must elapse before the multiplexer switches from one analog input channel to the next. Taking an example of the sinc3 style filter and using a decimation rate of 32, the filter settling time is illustrated for one conversion in Figure 8 (a). The data output, once the filter is fully settled, is a weighted average of the previous 96 outputs from the modulator. This equates to 12 µs or three cycles of the output data rate of the ADC.

Figure 8 (b) shows the first three samples of the multiplexed situation where each of the samples output by the ADC is fully settled. The modulator output does not overlap between any of the samples. The multiplexed rate indicated by the time between the DRDY (vertical lines) is decided by the settling time of the filter. This rate is often described in data sheets and parametric plots as a fully settled data rate.

For the sincP filter, the settling time of the filter is the filter order P, multiplied by 1/0DR. For a sinc3 filter running at 250 kHz ODR it means that the settling time of the filter is $3 \times 1/250$ kHz = 12 µs. By comparison, if using a sinc5 filter at the same ODR of 250 kHz, the settling time of the filter is $5 \times (1/2 50$ kHz) = 20 µs.

An approximate rate for switching between channels is the ODR divided by the order of the filter, so ODR/3 for sinc3, or ODR/5 for sinc5 filter. It is straight forward for direct sinc filters. An added step is required for cases such as the sinc5 + sinc1 style. The AD7175 family of ADCs offers the ability to choose between different styles of filters. The next section demonstrates the differences between the filter types and also provides an example of calculating the settling time for each of the cases.

Let's work out the settling time for a multiplexed scenario. A typical analog input module in process control and factory automation will have a front-end stage to scale a ± 10 V input to the input range of an AD7175-8. The AD7175-8 will then multiplex through each of the channels converting each input or input pair in sequence. The time to convert all channels depends on the filter used and also on the number of channels.

The following example compares the use of a sinc3 filter and a sinc5 + sinc1 filter, with both configured to the same output data rate we will see the contrast and method to calculate the settling time. Both filters options, which could be selected by the user of an AD7175-8.

a. Using sinc3 filter, 62.5 kHz ODR Calculating the settling time.

AD7175 sinc3: ODR = 62.5 kHz Settling time = $3 \times (1/62.5 \text{ kHz}) = 48 \ \mu\text{s}$, Channel switch rate = $1/48 \ \mu\text{s} = 20.833 \ \text{kHz}$

b. Using sinc5 + sinc1 filter, 62.5 kHz ODR Calculating the settling time.

AD7175 sinc5 + sinc1: ODR = 62.5 kHz

Note, there are two components. The sinc5 filter averages over a 4 μ s window (FMOD = 8 MHz) so it passes data to the averaging block at a rate of 250 kHz.

- 1. Settling time of the sinc5 = $5 \times 1/250$ kHz = 20 µs. This provides the first sample for the averaging.
- 2. Settling for the sinc1, averaging filter. For ODR = 62.5 kHz, 250 kHz data stream is averaged four times. Settling time for the remaining three samples for averaging is $3 \times 1/250$ kHz = 12 µs. Total settling time = 20 µs + 12 µs = 32 µs, channel switch rate = 1/32 µs = 31.25 kHz.

Note that for the sinc5 + sinc1 filter, data rates of 10 kSPS and below the ADC have a single cycle settling. This means that the settling time of the ADC = 1/0DR.

Table 2 shows the comparison of a 4-channel multiplexed measurement with setup (a) and (b). Using the sinc5 + sinc1 filter enables a faster per channel sampling rate, showing the advantages of shorter settling time. Note that this rule of thumb is relevant to the converter alone, if there are analog preconditioning circuits prior to each input, which have longer time constants than that of the ADC, it will be the worst-case settling time which will dominate.

This comparison is shown in Table 2:

Table 2. Per Channel Data Rate Comparisons of Sinc5 + Sinc1 vs. Sinc3 Filter for a 4-Channel Multiplexed System (for Instance, Using the AD7175-8)

Filter Type	ODR (kHz)	Per Channel Settling Time (µs)	Time to Convert Four Channels (µs)	Per Channel Data Rate (kHz)
Sinc5 + sinc1	62.5	32	128	7.8125
Sinc3	62.5	48	192	5.208

That completes the overview of Σ - Δ ADCs—the theory surrounding the modulator and concept followed by the examples of the digital filtering, and their effects on noise, settling time, and some of the knock on effects of both within your measurement system.

References

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