Need More Bandwidth for the Ka-Band? Here Are Three Options

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Introduction

As the demand for global connectedness increases, many satellite communications (satcom) systems are pushing toward higher data rates with an increased presence in the Ka-band spectrum. With high performance signal chains now able to support multiple GHz of instantaneous bandwidth and with potentially hundreds of transceivers in a system, the potential for very high throughput data rates is now a reality.

In addition, there is a trend in many systems to move away from static mechanically steered parabolic antennas toward active phased array antennas. This is driven by the enhanced technology and increased integration available to drive element spacing down to what is required at the Ka-band. Phased array technology also allows for improved interference mitigation by creating nulls in the antenna pattern in the direction of interfering signals.

The following overview describes some of the trade-offs that exist within the transceiver architectures available, and what types of architectures may be appropriate for different types of systems. Included in this analysis is a breakdown of some of the key specifications for a satellite system and how these system-level specifications translate to transceiver signal chain level components.

Specification Flow-Down from System-Level Analysis

Satcom systems at a high level are concerned with maintaining a certain carrier-to-noise ratio (CNR), which is a result of the link budget calculation. Maintaining this CNR ensures a certain bit error rate (BER). The CNR required depends on many things, such as error correction, information coding, bandwidth, and modulation type. Once a required CNR is established, the individual receiver and transmitter specifications can flow down from the high level system requirements. Typically, they will first flow down in the form of a required gain-to-system-noise-temperature (G/T) figure of merit for receivers, and effective isotropic radiated power (EIRP) for transmitters.

For the receiver, translating from G/T to a lower level receiver signal chain specification, the system designer needs to know the antenna gain and system noise temperature, which is a function of where the antenna is pointing and the receiver's noise temperature, as shown in Equation 1. From here, the receiver temperature can be found in Equation 2.

$$\frac{G}{T}(\text{dB}) = G_{ant}(\text{dB}) - 10log(T_{sys}) \quad (1)$$

$$T_{sys} = T_{ant} + T_{RX} \quad (2)$$

The noise figure required of the receiver signal chain can then be found from Equation 3:

$$NF_{RX}(\text{dB}) = 10log\left(\frac{T_{RX}(\text{K})}{290\text{K}} + 1\right) \quad (3)$$

Once the receiver noise figure is known, a cascade analysis can be computed to determine if the signal chain is meeting these required specifications and if adjustments can be made as necessary.

For the transmitter, the EIRP needed is first determined based on how far away the receiver is (either ground-to-satellite or satellite-to-ground) and how sensitive the receiver is. Once the EIRP requirement is known, there exists a trade-off between the output power of the transmit signal chain and the gain of the antenna. With a higher gain antenna, the power consumption and size of the transmitter can go down but at the expense of a larger antenna. The EIRP is given by Equation 4.

$$EIRP\ (\text{dBW}) = P_{TX}(\text{dBW}) + G_{ant}(\text{dB}) \quad (4)$$

With careful component selection in the signal chain, the output power required can be maintained without causing degradation to other important parameters, such as the output noise spectral density and out-of-band RF energy that can cause interference in other systems.

Other critical specifications for both the transmitter and receiver include:

- Instantaneous bandwidth: How much spectrum the signal chain can digitize at any point in time
- Power handling: How large of a signal can a signal chain handle without degrading performance
- Phase coherency among channels: For emerging beamforming systems, ensuring predictable phase between channels to allow for simplified beamforming signal processing and calibration
- Spurious performance: Ensuring the receiver and transmitter do not produce RF energy at undesired frequencies that can impact the system or other system's performance

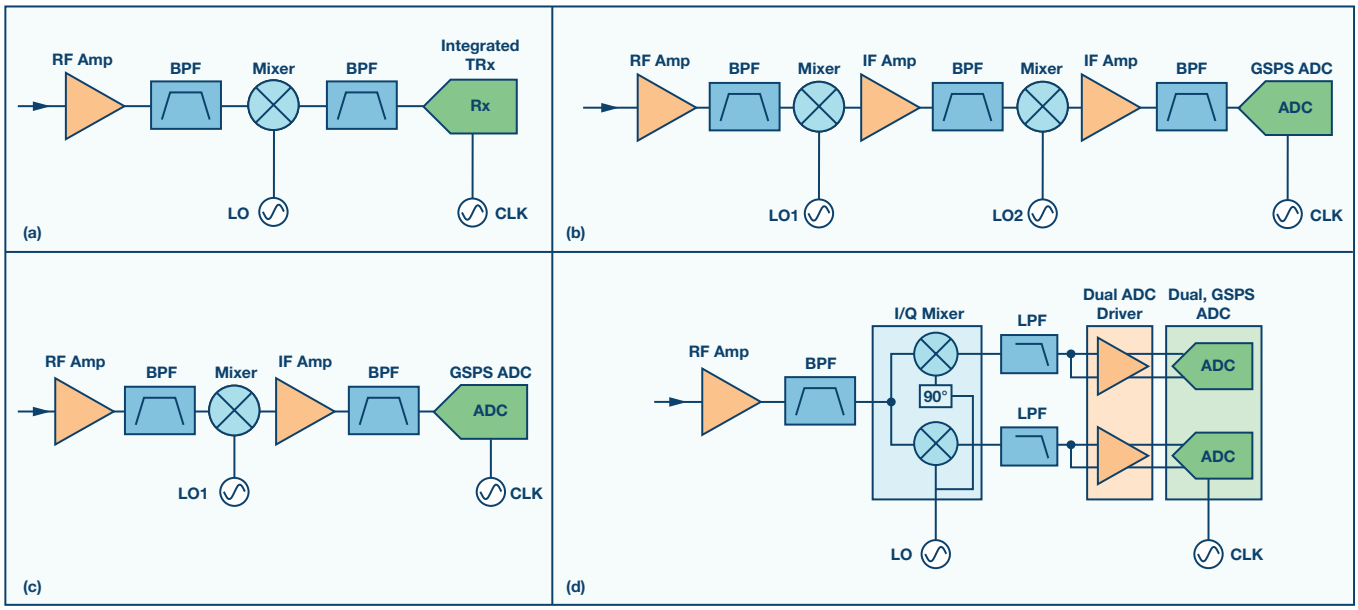

Figure 1. Architecture comparison, (a) high IF with integrated TRx, (b) dual-conversion super-heterodyne with GSPS ADC, (c) single-conversion super-heterodyne with GSPS ADC, (d) direct conversion with I/Q mixer.

Keeping these, and other specifications, in mind during the signal chain design is critical to guarantee a high performance system to meet any given application, whether it be a wideband multicarrier aggregation hub or an individual narrow-band handheld satcom terminal.

General Architecture Comparison

Once the high level specifications are determined, the signal chain architecture can be decided upon. One of the critical specifications previously listed that can have a big impact on the architecture is instantaneous bandwidth. This impacts the analog-to-digital converter (ADC) for the receiver and digital-to-analog converter (DAC) for the transmitter. To reach higher instantaneous bandwidth, the digitizers must be sampled at a higher rate, which can generally drive up power consumption of the signal chain as a whole, but decrease power consumption if judged on a W/GHz basis.

For systems with less than 100 MHz bandwidth, a base architecture, similar to that shown in Figure 1a, is optimal in many cases. This architecture uses a hybrid of a standard downconversion stage paired with an integrated direct conversion transceiver chip. The integrated transceiver provides a high level of integration, drastically reducing size and power.

To reach up to 1.5 GHz of bandwidth, a classic dual-conversion super-heterodyne architecture, in conjunction with the latest ADC technology, can be utilized; this is shown in Figure 1b. This is a well-established, high performance architecture with conversion stages used to filter out unwanted spurious signals. Depending on the received frequency band, there is a downconversion stage to an intermediate frequency (IF), and then an additional downconversion stage to bring the final IF to a low frequency that the ADC can digitize. The lower this final IF, the higher the ADC performance will be but at the expense of increased filtering requirements. Generally, due to the increased component count, this architecture is the largest and highest power of the four options presented.

A similar option is shown in Figure 1c, which is a single-conversion stage to a higher IF that is sampled by a GSPS ADC. This architecture takes advantage of the increasing RF bandwidth that ADCs are able to digitize with very little performance degradation. The latest GSPS ADCs on the market allow direct sampling of RF frequencies up to 9 GHz. In this option, the IF is centered somewhere in the range of 4 GHz to 5 GHz to strike the best balance between filtering requirements for the signal chain and ADC requirements.

The final option is shown in Figure 1d. This architecture provides an even larger increase in instantaneous bandwidth, but at the expense of complexity and potentially decreased performance. This is a direct conversion architecture using a passive I/Q mixer that can put out two IFs at baseband that are 90° offset from one another. Each I and Q leg is then digitized using a dual-channel, GSPS ADC. In this case, up to 3 GHz of instantaneous bandwidth can be obtained. The major challenge with this option is maintaining the quadrature balance between the I and Q path, as the errors propagate through the mixer, low-pass filter, and ADC driver. Depending on CNR requirements, this may be an acceptable trade-off.

A general overview has been given here that describes, at a high level, the operation of these receiver architectures. The list shown is not all inclusive by any means, and hybrids that use elements of each option are also possible. Although transmit signal chains were not covered in the comparison, each option from Figure 1 has a corresponding transmit signal chain with similar trade-offs.

Ka-Band Satcom Receiver Examples

With the previous discussion on the pros and cons for each architecture, we can now apply these understandings to real signal chain examples. Many satcom systems are now operating in the Ka-band in order to decrease antenna size and increase data rates. This is especially relevant in high throughput satellite systems. The following are examples using different architectures along with a more detailed comparison.

For systems that require instantaneous bandwidth below 100 MHz, such as with very small aperture terminals (VSATs), the high IF architecture with an integrated transceiver chip (AD9371) can be used, as shown in Figure 2. This design can achieve low noise figure and because it has such a high level of integration, it offers the smallest design footprint. A summary of its performance can be seen in Table 1.

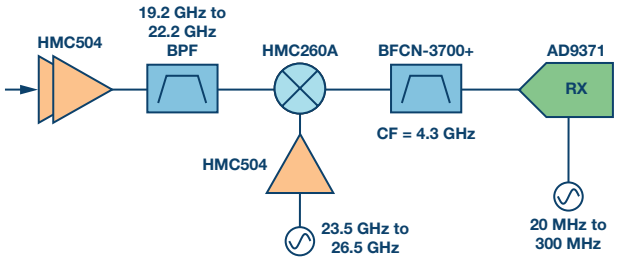

Figure 2. High IF with integrated TRx, up to 100 MHz bandwidth.

Some systems may be dealing with many carrier signals at a time if they are acting as a hub for multiple users in a satcom system. In this case, bandwidth per receiver or bandwidth/power become important factors. The signal chain shown in Figure 3 uses a high speed ADC, the AD9208, a recently released high sample rate ADC, which can digitize up to 1.5 GHz of instantaneous bandwidth. In this example, the IF is placed at 4.5 GHz to achieve 1 GHz of instantaneous bandwidth. The achievable bandwidth here will depend on filtering requirements for the antialias filter before the ADC but is generally limited to ~75% of a Nyquist zone (half of the sample rate).

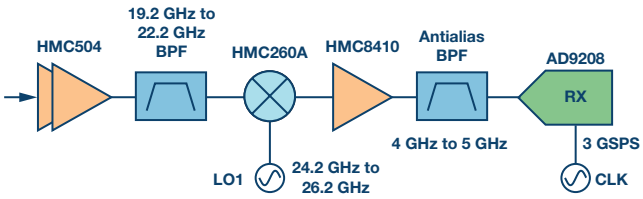

Figure 3. Single downconversion to high IF with GSPS ADC.

In systems that demand the highest instantaneous bandwidth and can give up performance in the form of CNR, the signal chain shown in Figure 4 may be desirable. This signal chain utilizes an I/Q mixer, the HMC8191, which has an image rejection performance of ~25 dBc. In this case, the image rejection is limited by the amplitude and phase balance between the I and Q output channels. This is the limiting factor for this signal chain without more advanced quadrature-error-correction techniques (QEC). A summary of the signal chain performance is shown in Table 1. Notably, the NF and IP3 performance is similar to the other options, but the power/GHz metric is the lowest of the three and size is similarly optimal for the amount of bandwidth that can be utilized at any instant.

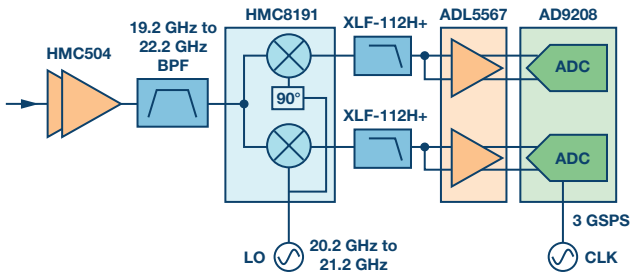

Figure 4. Direct conversion with I/Q mixer and GSPS ADC.

The three receive options given here are shown in the table below but it should be noted that this list is not meant as a comprehensive breakdown of all possible options. This summary overview is given in order to show differentiation among the various signal chain options. In any given system, the final optimal signal chain may be one of the three shown or a hybrid approach of any of these.

Table 1. Detailed Comparison of Ka-Band Receivers

	High IF with Int. TRx	High IF with GSPS ADC	Direct Conversion
Digitizer	AD9371	AD9208	AD9208 (dual-channel)
Instantaneous Bandwidth	100 MHz	1 GHz	2 GHz
NF (dB)	2.5	2.3	2.3
IIP3 (dBm)	–19	–20	–20
Max Pin (dBm)	–38	–40	–41
Other Spurious (HD2, HD3, MxN)	65 dB	73 dB	45 dB
Image Rejection (dBc)	75	80	25
Filtering Difficulty	Low	Medium	Low
Power (W)	2.9	4.1	6.1
Power/GHz (W/GHz)	29	4.1	3.05
Package Size (mm^2)	300	510	580

Additionally, even though only the breakdown for the receiver side is shown, many similar trade-offs exist for transmitter signal chains as well. Generally, there is a trade-off between the bandwidth and performance as systems move from a super-heterodyne style architecture to a direct-conversion style architecture.

Data Interface

Once the data has been digitized by the ADC or transceiver, it must be passed along through a digital interface to be processed by the system. All of the digitizers mentioned utilize the high speed JESD204b standard, which takes the bits from the data converter and packages them into frames to be transmitted on a small number of traces. The data rate coming out of the chips will vary based on system requirements, but all of the mentioned parts have digital functionality to decimate and frequency shift to accommodate various data rates to suit different system requirements. This specification allows for up to 12.5 GSPS speeds on the JESD204b lanes, which is fully taken advantage of for high bandwidth systems passing large amounts of data. Detailed descriptions of these interfaces can be found in the data sheets for the AD9208 and AD9371. Furthermore, selection of the FPGA must take into account this interface. Many FPGAs from vendors, such as Xilinx® and Altera®, and others now incorporate this standard into their part for easy integration with these data converters.

Conclusion

The analysis shown has broken down the various trade-offs and given specific examples of signal chains appropriate for satcom systems operating in the Ka-band. Several architecture options have been given including a single-conversion to high IF utilizing the integrated transceiver AD9371, a similar architecture using a GSPS ADC in place of the integrated transceiver to increase instantaneous bandwidth, and a direct conversion architecture that increases bandwidth, but at the trade-off of decreasing image rejection performance. The signal chains presented can be used directly but are meant as starting points in the design process. Depending on the system level application, different requirements will emerge, and a clear path will likely be evident that will favor one signal chain over the other.

References

Bosworth, Duncan and Wyatt Taylor. "Bandwidth Demands Place New Strains on Satellite Communications Design." Analog Devices, Inc., 2016.

Delos, Peter. "A Review of Wideband Receiver Architectures." Analog Devices, Inc., 2017.

Hall, Brad and Wyatt Taylor. "Small Form Factor SATCOM Solutions." Analog Devices, Inc., 2017.

Bousquet, Michel and Gerard Maral. *Satellite Communications Systems*—5th Edition. West Sussex: John Wiley & Sons, Inc., 2009.

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