Phase Alignment and Control on the ADF4356/ADF5356 Devices

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Introduction

As their name suggests, phase-locked loops (PLLs) use a phase detector to compare a feedback signal with a reference signal, locking the phases of both signals together. While this property still has many applications, PLLs today are most commonly used in frequency synthesis, generally as local oscillators (LOs) in frequency up/downconverters, or clocks for high speed analog-to-digital converters (ADCs) or digital-to-analog converters (DACs).

Until comparatively recently, little attention was paid to the behavior of phase in these circuits. However, with growing demand for efficiency, bandwidth, and performance, RF engineers have to devise new techniques to improve spectral and power efficiency. Repeatability, predictability, and adjustability of the phase of a signal all play an increasingly important role in modern communication and instrumentation applications.

All Is Relative

It is meaningless to refer to a phase measurement unless it is relative to another signal or to the original phase. For example, the phase measurements of a vector network analyzer (VNA) of a two port network—like an amplifier—refers the output phase to the input phase ANG(S21). The phase of a single input refers the reflected phase to the incident phase ANG(S11). On PLL synthesizers, phase measurements are referred to the input reference phase or from one signal to another. The holy grail or ideal state for any phase measurement is to be at a precisely desired value compared to the original phase, but nonlinearities, nonidealities, temperature differences, and board trace, as well as other manufacturing variances, means that phase is among the more variable of properties in signal generation. For the purposes of this article, the term in-phase refers to signals that have precisely the same amplitude and timing properties; deterministic phase means the phase offset between them is known and predictable.

Oscilloscopes Measuring Phase

To compare phases of two different frequencies, a high speed oscilloscope is a relatively intuitive means of comparing the output phase to a reference phase. In order to be visible, the input and output phases generally have to be integer multiples of each other. This is relatively common in many clocking circuits. For integer-N PLLs, the relationship between the input frequency (REF_{IN}) and the output frequency (RF_{OUT}) is generally deterministic and repeatable. Simply place a scope probe on both the REF_{IN} and RF_{OUT}, but take care to only capture the signal when you are certain that the phase has settled. Sophisticated oscilloscopes, like RTO1044, allow the event trigger to activate only when certain conditions have been met: like when a specific digital pattern has been written to the PLL device and a rising edge from the known signal is present. Given that there may be some delay between the writing of the digital pattern and when the final signal has settled, it is vital to insert some delay between the two events, and this is possible with this particular model of instrument.

The goal of the measurement in Figure 1 is to verify that the phase delay of the ADF4356 PLL relative to a known reference signal (in this case, another ADF4356 programmed to the same output frequency) is constant and repeatable on power up. To set up the instrument correctly, two low speed probes were connected to the CLK and DATA lines of the ADF4356 SPI interface. Once the digital pattern to write the particular frequency was noted, a wait time of 1 sec was followed before the instrument captured the time domain plot showing the output of both PLLs.

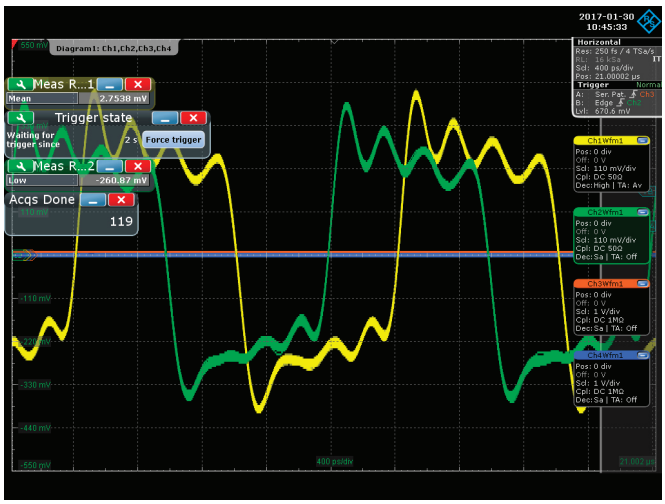


Figure 1. Integer-N setup.

For this measurement, two ADF4356 PLLs were locked at a VCO frequency of 4 GHz and divided by 8 MHz to 500 MHz, and one was repeatedly powered off and on using the software power down feature. 119 acquisitions were followed with the oscilloscope in infinite persistence mode and the phase difference between the two is constant and repeatable. A number of precautions were followed to ensure the phase difference was repeatable. Low R divider values introduce less uncertainty than higher ones and it is vital that the divided feedback from the VCO output is fed to the N counter input. Given that the ADF4356 PLL and VCO contain 1024 differing VCO bands, it is important that this uncertainty is eliminated by using the manual calibration override procedure.

Phase Resync Definition

Phase resync is defined as the ability of fractional-N PLLs to return to the same phase offset at each given frequency. That is, observing Frequency A with Phase P1 when changing channels to Frequency B, the same original phase P1 is observed when the frequency is reprogrammed back to F1. This definition ignores changes due to VCO drift, leakage currents, temperature changes, etc.

Resync sends a reset pulse to the fractional-N, Σ-Δ modulator, which places it in a known repeatable state. This reset pulse needs to be applied after the frequency settling mechanisms like VCO band select and loop filter settling time have completed. Its value is controlled by a timeout counter in Register 12. On recent PLLs, the ability to adjust the timing of this reset pulse has enabled a degree of adjustability on the output signal, with the ability to vary the timing of this in steps of $360°/2^{25}$, which is more than can easily be measured by most instruments.

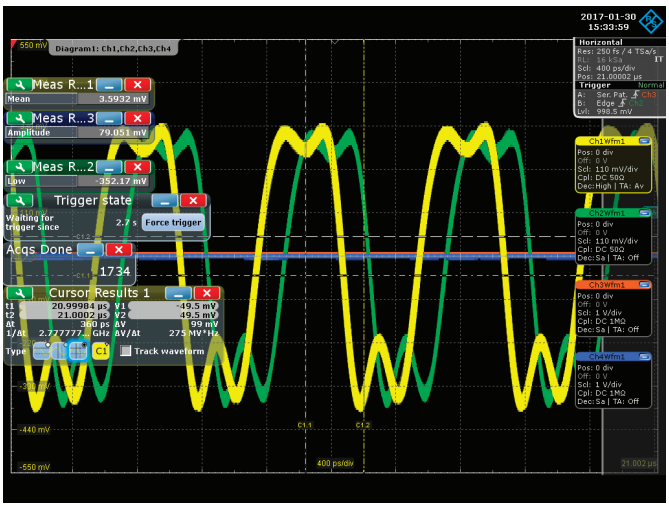


Figure 2. Fractional-N resync in operation, programming from 4694 MHz to 4002.5 MHz.

For this experiment, both ADF4356 VCOs were programmed to 4002.5 MHz and divided by 8. The second PLL was programmed to a VCO frequency of 4694 MHz and then programmed back to 4002.5 MHz. Using an oscilloscope to examine the behavior of the PLL, it can be seen that after 1700 frequency changes, the PLL settles to the same phase each time.

In order to characterize the different phase offset feature, the phase word was programmed to $4194304/2^{25}$, which equates to 90°. Similar values for 90°, 180°, 270°, and 0° were programmed, and the scope plot examined again (Figure 3).

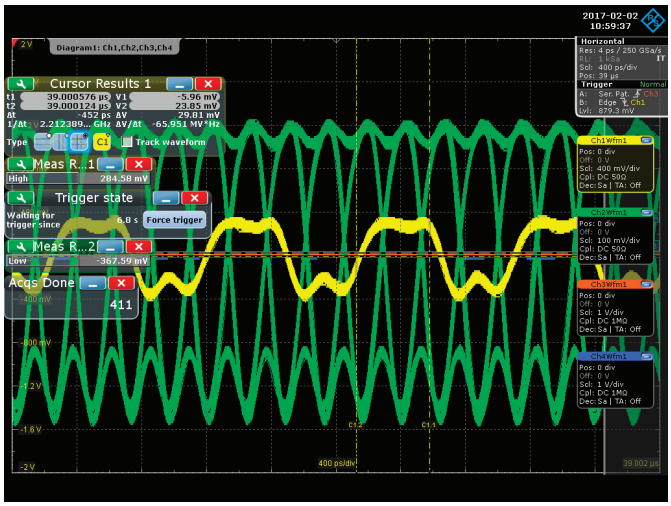


Figure 3. Phase resync with variable offsets.

Relative to the original signal on Channel 1, four equally spaced signals are observed, confirming the accuracy of the phase resync with programmable offset.

This feature is highly useful and means that a look-up table of phase values can be created for each user frequency, with the phase value dialed in on each use. In an application that combines four LO frequencies in phase, the phase resync and offset features are used to adjust the output phases so that they combine to give 6 dB lower phase noise. If used as a tunable LO (likely on the first stage of a signal analyser), the resync and phase offset features allow the user to run a one-time calibration on power-up to determine the precise phase value for each LO. In use as the LO, the phase values can be programmed to each LO as necessary, eliminating the procedure of calibrating at each frequency.

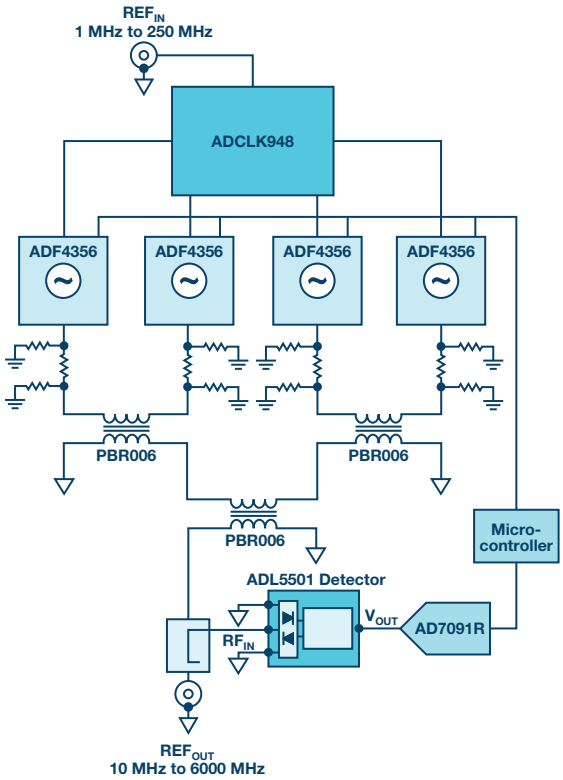


Figure 4. A phase critical application requiring precise control of PLL output phase.

For a phase critical application like a network analyzer, the circuit can measure the phase values at each frequency on power-up and then program them in as necessary, as the LO is swept across the range of interest.

Measuring Phase, Vector Signal, and Network Analyzers

Vector signal and network analyzers are also useful for characterizing phase behavior, although their use is limited to comparing the phase of the device to its initial value. Sophisticated analyzers, like the FSWP, can be placed in FM demodulation mode and the phase output selected.

This can be very useful for evaluating the phase resynchronization function that exists on the ADF4356 PLL. The trace below (Figure 5) shows the ADF4356 phase varied by 180° at an output frequency of 5025 MHz.

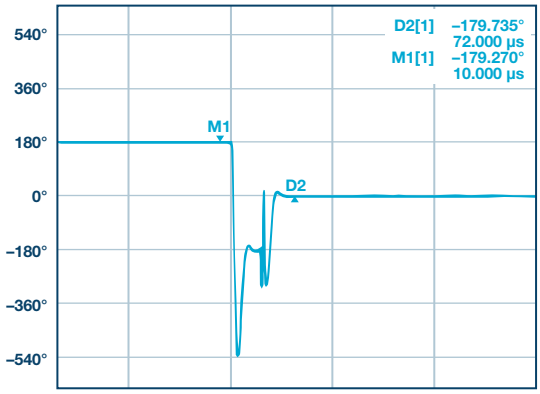


Figure 5. FSUP FM demodulator output for 180° phase offsets.

Phase Adjust

The phase adjust feature avoids resetting the Σ-Δ modulator and simply adds a phase word between 0° to 360° to the existing phase. This is useful in applications in which a reset of the phase is not desired. It can be used to dynamically adjust the phase word to compensate for known differences in phase due to effects like temperature.

Phase adjust adds phase to the existing signal on each update of R0 (with the value programmed to Register 3). It doesn't contain a reset pulse like phase resync. Measurements below from an FSWP show the addition of 90° (Figure 6) and 270° (Figure 7) to the original signal. In both cases the output frequency of the ADF4356 was set to 5025 MHz before changing the phase.

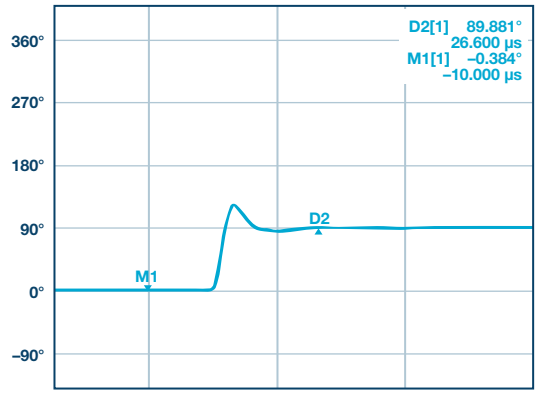


Figure 6. 90° change.

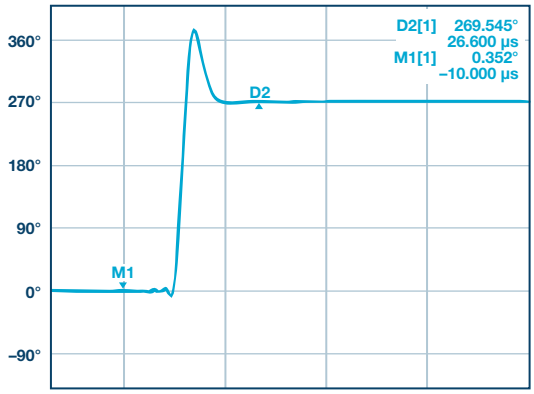


Figure 7. 270° change.

Behavior Over Temperature

Because the physical parameters of inductors change over temperature, so do the electrical characteristics, which manifest as a change in phase. To mitigate this phase change, the user can program in the required phase offset to maintain the same phase. Two ADF4356 PLLs programmed to 4 GHz output frequency placed in the same oven chamber at the same phase track each other's phase closely (Figure 2), so this proves that a user can adjust the phase depending on temperature.

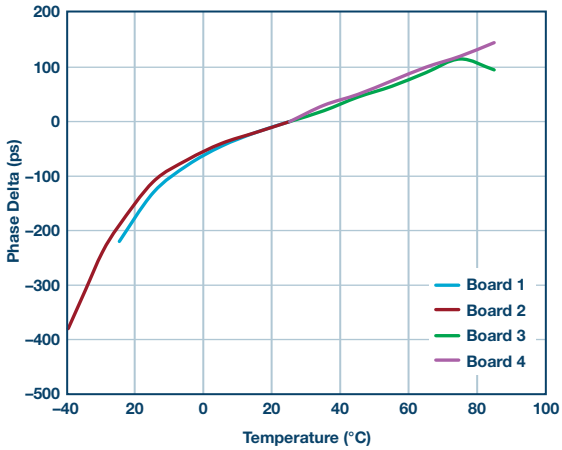
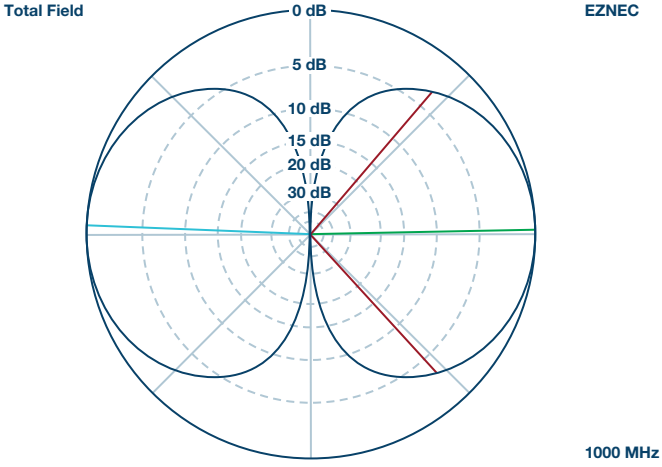


Figure 8. ADF4356 phase drift over temperature, measured at 4 GHz VCO frequency.

5G

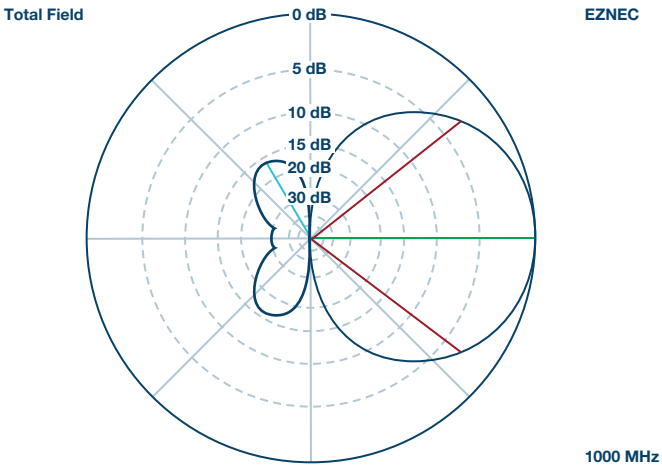
Beamforming is a technique that is key to the architecture of 5G networks. In these networks multiple antenna array elements are used with varying phase and amplitude at each element to direct antennae energy directly to the end user. For this application, phase repeatability is critical. The LO phase needs to be repeatable for beamforming and if the phase is uncertain, then additional calibration by the beamforming circuitry will be required.

Figure 9 shows two half element wavelengths spaced a quarter wavelength apart and driven in phase. The antenna radiation pattern is almost omnidirectional and no beamforming is observed. Figure 10 shows two elements driven by signals 90° out of phase and the resulting radiation pattern shows how the radiation pattern is more focused. As the number of element arrays is increased, this permits greater accuracy of the radiation pattern toward the end user, which results in greater spectral efficiency.



Azimuth Plot		Cursor Az	1.0°
Elevation Angle	0.0°	Gain	0.23 dBi
Outer Ring	0.23 dBi		0.0 dB max
Slice Max Grain	0.23 dBi @ Az Angle = 1.0°		
Front/Side	34.19 dB		
Beamwidth	96.8°; –3 dB @ 312.3, 49.1°		
Sidelobe Gain	0.23 dBi @ Az Angle = 178.0°		
Front/Sidelobe	0.0 dB		

Figure 9. No beamforming.



Azimuth Plot		Cursor Az	0.0°
Elevation Angle	0.0°	Gain	5.26 dBi
Outer Ring	5.25 dBi		0.0 dB max
Slice Max Grain	5.26 dBi @ Az Angle = 0.0°		
Front/Side	29.26 dB		
Beamwidth	75.5°; –3 dB @ 322.6, 38.1°		
Sidelobe Gain	–10.88 dBi @ Az Angle = 122.0°		
Front/Sidelobe	16.14 dB		

Figure 10. Beamforming.

The phase resync feature ensures that the uncertainties in the phase characteristic of the LO are eliminated. Additionally, the ability to adjust this phase provides the user with an additional lever to overcome any other phase delays in the circuit that are difficult to adjust by the beamformer or the baseband circuitry.

Conclusion

Phase resynchronization places the ADF4356 and similar PLL parts into a known phase, which enables many applications and greatly simplifies calibration routines.

About the Author

Ian Collins graduated from University College Cork with a degree in electrical and electronic engineering, and has worked in the RF and Microwave Group of Analog Devices since 2000. He is currently applications manager of the Microwave Frequency Generation Group, which focuses mainly on phase-locked loop (PLL) and voltage control oscillator (VCO) products. When not spending time at work or with his young family, Ian enjoys photography and the theater (both on and off-stage), reading, and listening to music.

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