



# Ultralow Power Opening Applications to High Speed Isolation

# by Mark Cantrell, applications engineer, Analog Devices, Inc.

Isolation has long been considered a necessary burden by designers. It is necessary because it makes electronics safe for anyone to use. It is a burden because it limits communication speed and consumes a lot of power and board space. Old technology optocouplers and even many newer digital isolators consume so much power that certain types of applications have not been practical. In this article, we will examine the latest developments in ultralow power isolation, how it relates to the available technologies, and how it has been achieved. We will also explore several applications that can benefit from this new class of devices.

The advent of the modern optocoupler about 45 years ago was a great step forward for designers. They allowed feedback in power supply control circuits, signal isolation in communications to break ground loops, and communications to high side power transistors or current monitors. In the 1970s there was a proliferation of optoelectronic devices. These shaped the development of communications standards such as RS-232, RS-485 and industrial busses like 4 to 20 mA current loops and DeviceNet and PROFIBUS®. The capabilities of optical isolation shaped many of the properties for these communications buses due to the limits of the isolation devices. During the next 20 years, the changes in isolation technology were largely incremental until 2000, when the first of the new chip scale digital isolators were introduced. These new devices were based on inductive coupling through chip scale transformers, GMR materials, and, later, through differential capacitive coupling. The new technologies were capable of vastly higher speeds and substantially lower power levels than the older optocouplers, but the standards were in place and many of the capabilities of the new devices such as high speeds have not been fully utilized since the existing standard interfaces did not require

Digital isolators' use of standard packaging and IC processes to build their encoding and decoding electronics makes

adding digital functionality straightforward. Low power consumption, support for low supply voltages, and high levels of integration have become the primary design advantages of the nonoptical isolators. Innovation that moves isolation into much higher speeds or much lower power will allow support of the most demanding new interface standards. Currently the power consumption in digital isolators, while significantly lower than the optocoupler, needs to be two to three orders of magnitude lower to allow entry into new application spaces. High performance isolation has not been able to achieve this goal until now.

### **COMPARING TECHNOLOGIES**

The driver of performance in isolation devices is a combination of the data encoding scheme and the efficiency of the medium used to transfer the data. For this discussion we will focus on the aspects that determine power consumption. The encoding and decoding schemes can broadly be divided into edge encoding pulse-based systems and level encoded systems. At its simplest, a level-based system must constantly push energy across the isolation barrier to hold a dominant output state, while sending no energy across the barrier to represent the recessive output state.

In an optocoupler, light mediates the energy transfer, which has poor efficiency when compared to creating electric or magnetic fields directly, and poor detection efficiency at the receiving element. So simple transistor or PIN diode-based optocouplers have to expend a lot of energy creating light to hold the output in the on state, but the receiver expends little energy to receive the signal. This can be seen in Table 1 with the power consumption of the PIN diode receiver optocoupler. On average, high input current and low output current characterize this type of optocoupler. Higher speed digital optocouplers have reduced the amount of light required to maintain a state by adding active amplification to the receiver. This reduced the average current required for the LED, but the receivers have relatively large quiescent current, so the power consumption has not really diminished—it has been pushed to the receiver. Lowering the required power would require raising the efficiency of the LED and receiver element, or changing the encoding scheme. This is why advances in optocoupler technology have been incremental for so long.

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In many capacitively coupled digital isolators, the system is actually similar to the optocoupler. This type of device uses a high frequency oscillator to send a signal across a pair of differential capacitors. The oscillator, much like the LED of an optocoupler, consumes power to send the active state and turns off to send the recessive state. The receiver has active amplifiers that consume bias current for either state. As shown in Table 1, due to the high coupling efficiency of the capacitors, the overall current consumption is significantly better than the optocoupler options. It should be noted that the power level in the digital isolator would be about the same if it used inductive coupling instead of capacitive. In this case, it is primarily the encoding scheme that sets the minimum power level, especially at low data rates.

A second encoding scheme shown in Figure 1 is utilized by the iCoupler®-based digital isolators from Analog Devices, such as the ADuM140x series. In this scheme, edges are detected at the input and encoded as pulses. In the case of the ADuM140x, one pulse represents a falling edge, and two pulses represent a rising edge. These pulses are coupled to the secondary through small, on-chip pulse transformers. The receiver counts pulses and reconstructs the data stream. The pulses themselves are robust to get good signal to noise ratio, but only 1 ns wide so the energy per pulse is low. This has the very nice property that when no data is changing, the state is held at the output in a latch and almost no power is consumed. This means that the power consumption is simply the integrated energy delivered in the pulse stream plus some bias currents. As the data rate goes down, the power goes down linearly all the way to dc. Again, it is the encoding scheme that delivers the reduction in power consumption rather than the specific medium of data transfer, this scheme could be implemented in capacitive or even optical systems.

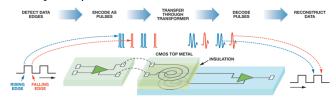


Figure 1. Pulse-Based Encoding

The pulse encoding scheme is not a low power panacea. Its drawback is that if there are no logic changes at the input, then no data is sent to the output. This means that if there is a dc level difference due to the start-up sequence, the input and output would not match. The ADuM140x addresses this condition by implementing a refresh watchdog timer on the input channel that resends the dc state if no activity has been

detected for more than 1  $\mu$ s. The result of this design is that this encoding scheme no longer continues to reduce power consumption once the data rate is below 1 Mbps. The part is effectively always running at least 1 Mbps, so the power consumption does not continue to fall for low data rates. Even so, the pulse encoding scheme provides lower average power when compared to the level sensitive schemes as shown in Table 1.

Technology	Input (mA)	Output (mA)
High Speed Digital Opto	2.5	8.5
High Speed PIN/Transistor Opto	8	1.2
Capacitive Digital Isolator	1.25	1
Inductive Digital Isolator	0.5	0.23
Ultralow Power Inductive Digital		
Isolator	0.01	0.01

Table 1. Comparison of Isolator Power Consumption/Channel at V<sub>DD</sub> = 3.3 V and 100 kbps

# **PUSHING THE LOW POWER ENVELOPE**

The ADuM140x pulse encoding scheme was originally optimized for high data rates, not absolute lowest power consumption. This encoding scheme has considerable potential for further power reduction especially in the dc to 1 Mbps frequency range. This data range is where the bulk of the isolation applications are found, especially the ones that require low power. The following innovations were implemented in the 4-channel ADuM144x and 2-channel ADuM124x *i*Coupler technology-based families.

- 1. The design was implemented in a lower voltage CMOS process
- 2. All bias circuits were reviewed and, where possible, biases were minimized or eliminated
- 3. The frequency of the refresh circuit was reduced from 1 MHz to 17 kHz
- 4. The refresh circuit can be disabled completely for lowest possible power consumption

The current consumption as a function of frequency is shown in Figure 2 compared to the ADuM140x. The knee in the curves due to refresh can easily be seen at 1 Mbps for the ADuM140x and at 17 kbps for the ADuM144x when refresh is enabled. The ADuM144x has a typical current consumption per channel 65 times lower at 1 kbps, and about 1000 times lower if refresh is completely disabled.

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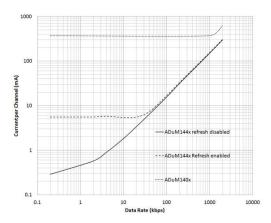


Figure 2. Total Current Consumption per Channel for ADuM144x and ADuM140x Parts at VDDX = 3.3 V

Why is this much reduction in power useful? Below are three applications where traditional optocouplers and digital isolators are either marginal or completely unusable.

# 4 mA TO 20 mA ISOLATED LOOP-POWERED FIELD INSTRUMENT

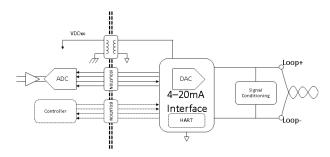


Figure 3. Isolated, Loop-Powered Smart Sensor Front End with HART® Modem Support

Loop-powered field instruments have a very limited power budget since all power is derived from the 4 mA loop current. Luckily, the loop usually provides enough voltage, typically 24 V, to pull about 100 mW from the system. The entire application will use about 12 V of the loop voltage at 4 mA. Within that budget, a simple dc-to-dc converter supplies the isolated sensor, analog-to-digital converter (ADC), and controller. Even assuming a fairly high efficiency for the dc-to-dc converter, and a 2:1 step down in voltage, a typical sensor front end will have < 4 mA at 3.3 V to work with. The loop side has about the same power budget. The primary interface is the SPI bus to the ADC. Each side of the isolated interface is powered from the loop, along with all of the controller's ADCs, and signal conditioning elements. Table 2 shows the current consumption for a 4-wire SPI bus for each of the isolation technologies. SPI 1 is the loop side current of the isolation, and SPI 2 is the sensor side current required. The

optocouplers would consume many times the power budget on each side of the isolation interface. The capacitive digital isolator would consume the entire power budget for the field instrument. The ADuM1401 is a possibility, but the power budget for the rest of the system is marginal even when supporting only the single SPI interface to the ADC. The new ultralow power ADuM1441 *i*Coupler-based digital isolator has such low power that it becomes a minor part of the power budget. This technology not only allows the application to work within its power budget, it allows the addition of a second 4-channel isolator to support a HART modem interface and a smart front-end controller, shown in the dotted blocks of the diagram. The ultralow power *i*Coupler technology enables new functionality that was previously not possible to achieve in an isolated application.

Technology	SPI 1 (mA)	SPI 2 (mA)
High Speed Digital Opto	16	28
High Speed PIN/Transistor Opto	25.2	11.6
Capacitive Digital Isolator	4.75	4.25
Inductive Digital Isolator	1.73	1.19
Ultralow Power Inductive Digital		
Isolator	0.04	0.04

Table 2. Total Power Consumption of Each Side of a 100 kbps Isolated SPI Interface

# POWER OVER ETHERNET I<sup>2</sup>C COMMUNICATIONS BUS

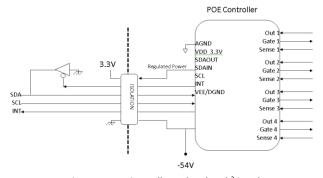


Figure 4. POE, Four Port Controller with Isolated PC and Interrupt

Telecom type applications like power over Ethernet (POE) get power from a relatively high voltage rail that supplies the Ethernet power. The control communications interfaces must get their power from an isolated dc-to-dc converter or through a regulator from the –54 V bus voltage. In the example in Figure 4, the 3.3 V communications interface for an I<sup>2</sup>C control bus is generated by a regulator internal to the

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POE controller. Table 3 shows the current required to run the I<sup>2</sup>C bus interface on the POE controller side along with the power dissipated inside the POE controller to support each technology. An optocoupler solution would dissipate half a watt of heat inside a chip that is likely running close to its thermal limit already. Each interface is a bit better going down the table until we get to the ultralow power ADuM1441, where the power dissipation is about 1 mW. This makes the interface a trivial thermal load for this chip. Even if the power was not regulated internal to the POE chip, this power is so low that a simple Zener diode and resistor could be used to give a suitable supply saving component cost and cooling load. This technology simplifies power architectures.

Technology	UART@ 100 kbps (mA)	Power Dissipation (mW)
High Speed Digital Opto	11.00	557.7
High Speed PIN/Transistor Opto	9.20	466.4
Capacitive Digital Isolator	2.25	114.1
Inductive Digital Isolator	0.73	37.0
Ultralow Power Inductive Digital		
Isolator	0.02	1.0

Table 3. Total Power Dissipation for Isolation Technologies in a POE Application

# **BATTERY-POWERED DEVICES**

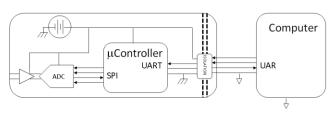


Figure 5. Battery-Powered Medical Sensor

The third example of the use of ultralow power is to support long duration battery applications. Medical appliances such as glucose meters and pulse oximeters for home health monitoring must be constructed to allow contact with the patient and connection to a nonmedical grade computer simultaneously. The serial interface has to be powered and ready to wake up the device when the computer is connected, so an active isolator should be part of the standby circuit. In this case, using the refresh disable feature of the

ADuM1441 will allow the part to draw less than  $4\,\mu\text{A}$  from the battery. This level is low enough that even a coin cell could maintain that standby current for years.

The ultralow power of the ADuM1441 also allows convenient powering of the computer facing side of the isolation. With only a few  $\mu A$  of current to operate the interface, a status line in the serial interface can be dedicated to providing power to the isolator, so no dedicated power supplies are required.

Table 4 illustrates some of the properties of optocouplers, as well as the varieties of digital isolation when operated in standby mode. Note that if the proper idle state is chosen, the PIN/transistor isolator can actually have a standby current as low as the ultralow power *i*Coupler-based product. This property of optocouplers has been used to generate low power standby in many applications. However, once communication starts, the power consumption jumps to relatively high levels, which is not the case with the ADuM1441 solution.

UART 10 kbps (mA)	UART idle (mA)
11.000	7.000
5.330	0.001
2.250	1.350
0.730	0.730
0.002	0.001
	(mA) 11.000 5.330 2.250

Table 4. Total Low Speed and Idle Power Consumption of Isolators

# CONCLUSION

ADI has developed a new version of the pulse encoded *i*Coupler-based digital isolators optimized for extremely low power. The modifications to this device have not compromised the isolation capabilities of the device, since the insulation is identical to what is used in our high isolation reinforced insulation devices. The signal integrity is similar to the standard *i*Couplers that have been on the market for the past 13 years. These devices are intended to give very low power operation in the dc to 1 Mbps range, with decreasing power consumption as the data rate gets lower. This represents a technology that enables isolation of interfaces not previously possible due to the dramatically lower operating power. For more information on the 4-channel ADuM144x series of ultralow power digital

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isolators, please visit www.analog.com/ADuM144x. For more information on the 2-channel ADuM124x series of ultralow power digital isolators, please visit www.analog.com/ADuM124x.



Mark Cantrell has been an applications engineer with the *i*Coupler Digital Isolator Technology Group at Analog Devices since 2006. Prior to that, he was the applications engineer at California Eastern Laboratories, where he was responsible for the NEC optocoupler and solid-state relay products.

# **RESOURCES**

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