

# Advancement in High Speed Converter Technology Enables Next-Generation Wireless Communications Systems Designs

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## INTRODUCTION

Wireless communications networks are evolving rapidly, as consumers express increasing demands for enhanced data services and greater use of bandwidth. New generation wireless communications systems demand higher data throughput, lower power consumption, and higher reliability. These requirements are often in conflict with each other. Meeting these demands requires a high sample rate, high signal bandwidth, and a power efficient digital-to-analog converter (DAC) solution. New generation high speed DAC products feature GSPS sample rates and input data rates, and offer multicarrier GSM compliant performance for the multiband, multistandard radio base station while lowering the total power consumption and the density of heat dissipation in the system. This article discusses how high speed converters can help system designers advance the innovation frontier in wireless communication systems design by providing a higher sample rate, larger data bandwidth, and lower power consumption.

## SYSTEM CHALLENGES IN HIGH BANDWIDTH

It is not uncommon that the transmit bandwidth of a modern mobile base station exceeds 300 MHz. The requirements of supporting wider data bandwidth and digital predistortion techniques are raising the bar for usable signal bandwidth and dynamic performance of high speed DAC products. The challenges in achieving higher system bandwidth are threefold.

First, higher signal bandwidth requires a faster DAC sample rate. The Nyquist-Shannon sampling theorem mandates that the converter sample rate be at least twice as fast as the signal to be synthesized. Hence, without taking account of other design constraints, the DAC sample rate needs to increase at  $2\times$  the rate of the signal bandwidth. Analog reconstruction filtering is another major factor in the system design that

pushes for a faster DAC sample rate. A brick wall analog filter is neither feasible nor efficient to build in a wireless transmitter. In practice, the system requires a certain oversampling ratio of the DAC sample rate over the synthesized signal bandwidth so that a filter transition band can be built between the desired signal and the high frequency DAC sampling images that need to be rejected. For example, if a signal to be synthesized spreads  $\pm 50$  MHz around the center frequency of 150 MHz, the higher end of the DAC output signal is 200 MHz, compared to 450 MHz when the signal is centered at 300 MHz with  $\pm 150$  MHz bandwidth. It can be seen that the second case requires a DAC with a much higher sample rate.

Second, higher signal bandwidth requires a faster and more reliable converter data interface. The required signal bandwidth increases proportionately with the transmitting data throughput. To achieve a 300 MHz system bandwidth using I/Q modulation, the combined input data rate of a dual DAC (I and Q) is 750 MSPS, considering a filter roll-off factor of 0.2. This translates to an input data period of 1.33 ns, which puts a large pressure on the system designers to minimize interbit timing misalignment on the data bus in order to meet the setup and hold timing requirements. With traditional parallel data interface schemes, such as LVDS and CMOS, this is very challenging. The new JESD204B high speed serial interface provides a reliable and scalable solution for migrating to higher data rates.

Third, integrated circuit (IC) devices are not ideal components. A DAC is no exception. A higher output bandwidth demands better dynamic performance from a DAC device for two reasons. The dynamic range generally decreases with the increase of the DAC output frequency. In addition, more spurious content tends to fall in band when the bandwidth is larger. However, the system spurious requirements do not scale or relax with the signal bandwidth. A mobile base station still needs to meet a regulated emission mask requirement regardless of the supported signal bandwidth. A DAC with superior dynamic performance eases frequency planning and filtering in the system.

Figure 1 and Figure 2 show the measured spectrum performance of an [AD9144](#) DAC synthesizing an 80 MHz signal (16 carrier W-CDMA) at a DAC sample rate of 2800 MSPS.

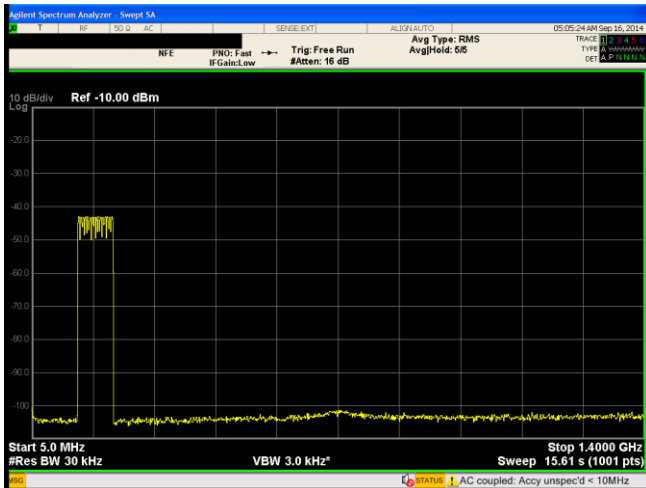


Figure 1. Measured Wideband Performance (Up to Nyquist Frequency) of an AD9144 DAC Synthesizing a 16 carrier W-CDMA Signal,  $f_{DAC} = 2800$  MSPS

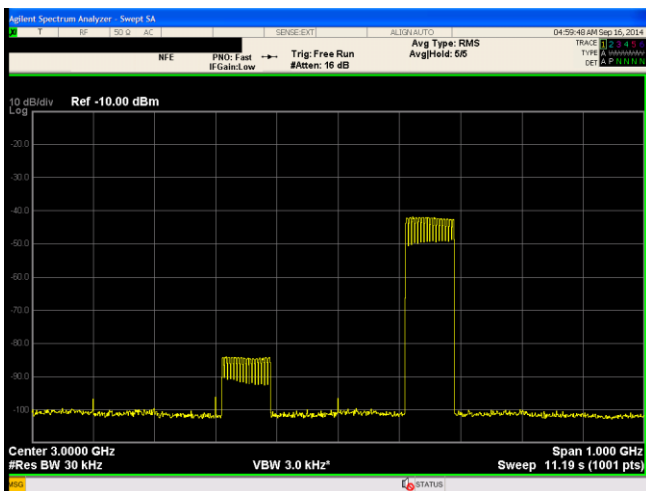


Figure 2. Measured Wideband Performance at an ADRF6720<sup>1</sup> QMOD Output at 3 GHz RF Frequency with the Same AD9144 DAC Output (as in Figure 1) Driving the QMOD

## SYSTEM CHALLENGES IN LOW POWER AND HIGH RELIABILITY

System designers are facing other challenges in increasing the transmit bandwidth and data capacity. These challenges include power consumption, heat dissipation, and system reliability. These dimensions are often orthogonal to, and sometimes in conflict with, the goal of higher system bandwidth. Therefore, system designers demand a new DAC product that can provide a higher level of feature integration, lower power consumption, lower operating heat density, and wider bandwidth in the same package.

High speed DAC products have been evolving rapidly in recent years and more digital and analog features have been integrated in the DAC product. Two clear examples are the DAC on-chip clock multiplier PLL and communication

specific signal processing features. These features used to be implemented somewhere else in the system, such as a high speed clock synthesizer and a baseband ASIC/FPGA. A DAC featuring these functions not only reduces the overall BOM cost but also provides a path for an easier and more reliable design. With a clock multiplier in the DAC, the system only needs to provide a low frequency reference clock to the device. The clock multiplier locks to the external reference clock and generates a high speed sample clock internally for the DAC. That means less worry about high speed clock coupling and trace impedance matching on the PCB. New digital features such as power detection and protection provide an extra layer of protection to the RF chain from being damaged by overrange signals or abnormal system behaviors. Despite this higher level of feature integration, the power consumption of DAC devices remains largely constant or even decreases compared to the last generation of products. The advancement of high speed DAC technology on finer silicon process nodes plays an important role in addressing system challenges.

Besides consuming less power and having a smaller carbon emission footprint, another important benefit from lower component power consumption is lower heat density. A wireless communications system is typically confined within a watertight metal chassis. The size and weight limits normally do not allow active cooling. The heat generated by the IC components is dissipated through the chassis. The cavity and PCB temperature inside of the chassis can be so high that it starts to have an impact on the system's long-term reliability. The accumulated heat can potentially affect the PCB mechanical characteristics, the solder joints between the components and board, and accelerate aging—long-term shifts of the electrical specifications of IC components. The heat distribution/dissipation in a system is not even. The contributions are mainly from several sources that are signal processing rich. The high speed DAC is one of them. Therefore, a DAC that is both feature rich and low power is very attractive to system designers.

Figure 3 and Figure 4 show measured performance of an AD9144 synthesizing a 4 carrier W-CDMA signal at a DAC sample rate of 1966 MSPS with on-chip DAC clock multiplier on and off respectively.

<sup>1</sup> [www.analog.com](http://www.analog.com)

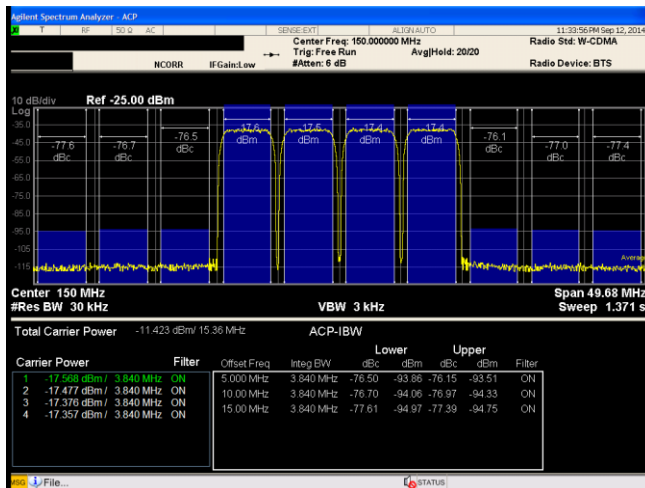


Figure 3. Measured 4 carrier W-CDMA ACLR Performance of an AD9144 at 150 MHz Output Frequency with On-Chip Clock Multiplier Enabled,  $f_{REF} = 245.76$  MHz,  $f_{DAC} = 1966$  MSPS

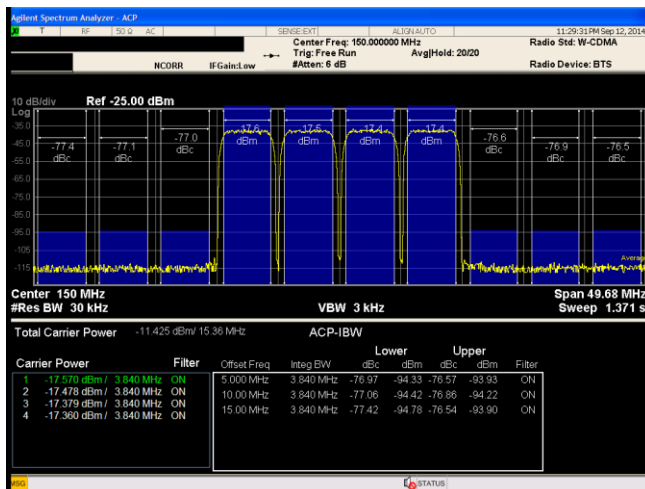


Figure 4. Measured 4 carrier W-CDMA ACLR Performance of an AD9144 at 150 MHz Output Frequency with On-Chip Clock Multiplier Disabled,  $f_{DAC} = 1966$  MSPS

## SYSTEM CHALLENGES IN COMMON PLATFORM DESIGN

While demanding wider coverage and ever more bandwidth, fast expansion of consumer demand for data services is also calling for multistandard radio (MSR) base stations. Different radio technologies and increasing frequency allocations make it more complex to control networks and reduce costs. Meeting these demands requires an efficient and comparatively inexpensive solution to the problem of building MSR base stations, a common platform design. DAC technological advances support this evolution of the base station design. Multicarrier GSM (MC-GSM) is generally considered the air standard that has the most stringent dynamic range requirements. The MC-GSM test is often used to judge whether a DAC product supports a common platform design.

Figure 5 and Figure 6 show the measured performance of an AD9144 synthesizing a 6 C-GSM signal at a DAC sample rate of 1966 MSPS.

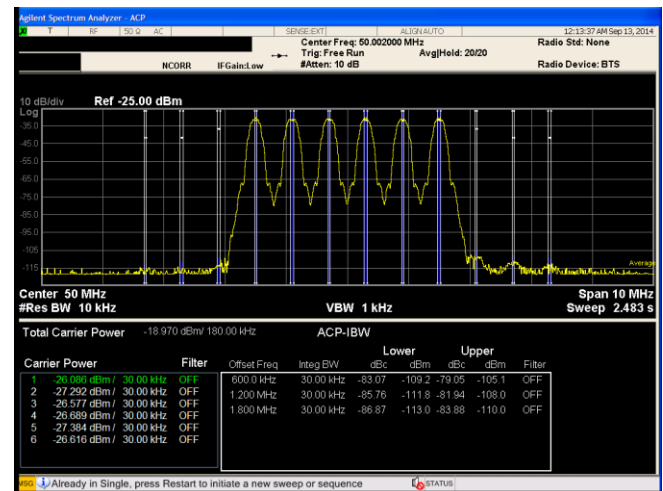


Figure 5. Measured 6 C-GSM IMD Performance of an AD9144 at 50 MHz DAC Output Frequency,  $f_{DAC} = 1966$  MSPS

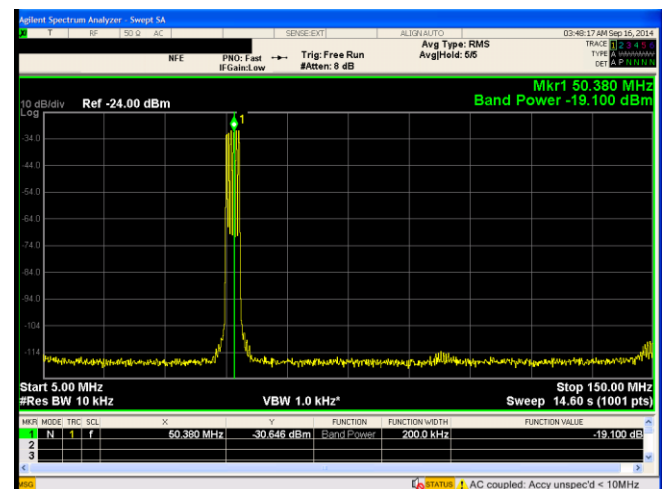


Figure 6. Measured 6 C-GSM Wideband Performance of an AD9144 at 50 MHz DAC Output Frequency,  $f_{DAC} = 1966$  MSPS

## SUMMARY

Modern wireless communications networks are evolving for more data services and greater use of bandwidth. In order to support this trend, new generation wireless communications systems need to have higher data throughput, lower power consumption, and higher reliability. The advancement of high speed DAC technology, such as the AD9144 from Analog Devices, has enabled next-generation multistandard radio design and has helped system designers achieve breakthrough innovations on multiple critical technological dimensions.

## ABOUT THE AUTHOR

Yi Zhang is an applications engineer for the High Speed Converter Group at Analog Devices. He has worked for ADI since 2007. Yi has over eight years of experience in high speed converter products and high speed mixed-signal applications. He is the author of the data sheets, application notes, and technical articles for several generations of high speed DAC products. Yi holds a master's degree in electrical engineering from Cornell University.

Michele Viani, applications engineer, has worked in the High Speed Converter Group at Analog Devices for five years.

Michele has worked as both a product engineer and applications engineer, responsible for evaluating high speed DAC products and providing technical support to customers in solving implementation issues. Michele holds a bachelor's degree in electrical engineering from Rensselaer Polytechnic Institute.

## RESOURCES

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