Keywords: programming SLC-96, SLC96, D4, signaling, framing, SLC-96

APPLICATION NOTE 2731

DS2155, DS21Q55, DS2156 Programming SLC-96

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Abstract: This application note provides a detailed description for using the SLC-96 multiframe in the DS2155, DS21Q55, and DS2156. Register values and an example flowchart for software routines allow the user to quickly implement SLC-96 into the application.

Introduction

This application note applies to the following products.

T1/E1 SCTs
DS2155
DS21Q55
DS2156

In a SLC-96-based transmission scheme, the standard Fs-bit pattern is robbed to make room for a set of message fields. The SLC-96 multiframe is made up of six D4 superframes, so it is 72 frames long. In the 72-frame SLC-96 multiframe, 36 of the framing bits are the normal Ft pattern and the other 36 bits are divided into alarm, maintenance, spoiler, and concentrator bits, as well as 12 bits of the normal Fs pattern. Please see the Bellcore document TR-TSY-000008 for more details about SLC-96.

Receive-Side SLC-96 Applications

To enable the DS2155 or DS21Q55 to synchronize onto a SLC-96 pattern, the following configuration should be used:

 - Set to D4 framing mode   T1RCR2.6 = 0
 - Set to cross-couple Ft and Fs bits T1RCR1.3 = 1
 - Set to minimum sync time   T1RCR1.2 = 0

The user has the option to either extract the SLC-96 message fields from the on-board RFDL register or via the external RLINK pin. The information is always available at both locations. If the user wishes to extract the message bits via the RLINK pin, then some hardware must be added to decode the bits. The SLC-96 message bits can be extracted via the RFDL register without any additional hardware, and it is this method that this application note addresses.

Figure 1 describes the method used to extract the SLC-96 message bits. The DS2155, DS21Q55, and DS2156 contain an on-board SLC-96 synchronizer that is enabled when the T1RCR2.4 bit is set to one. In this mode, the match flag (SR8.1) takes on a new meaning; it will indicate when the framer has received the 12-bit Fs pattern that exists in SLC-96 multiframe. In each SLC-96 multiframe, the user will read the RFDL register three times. The external controller will wait for the match flag to be set. Once set, the controller will then wait for the RFDL to fill.
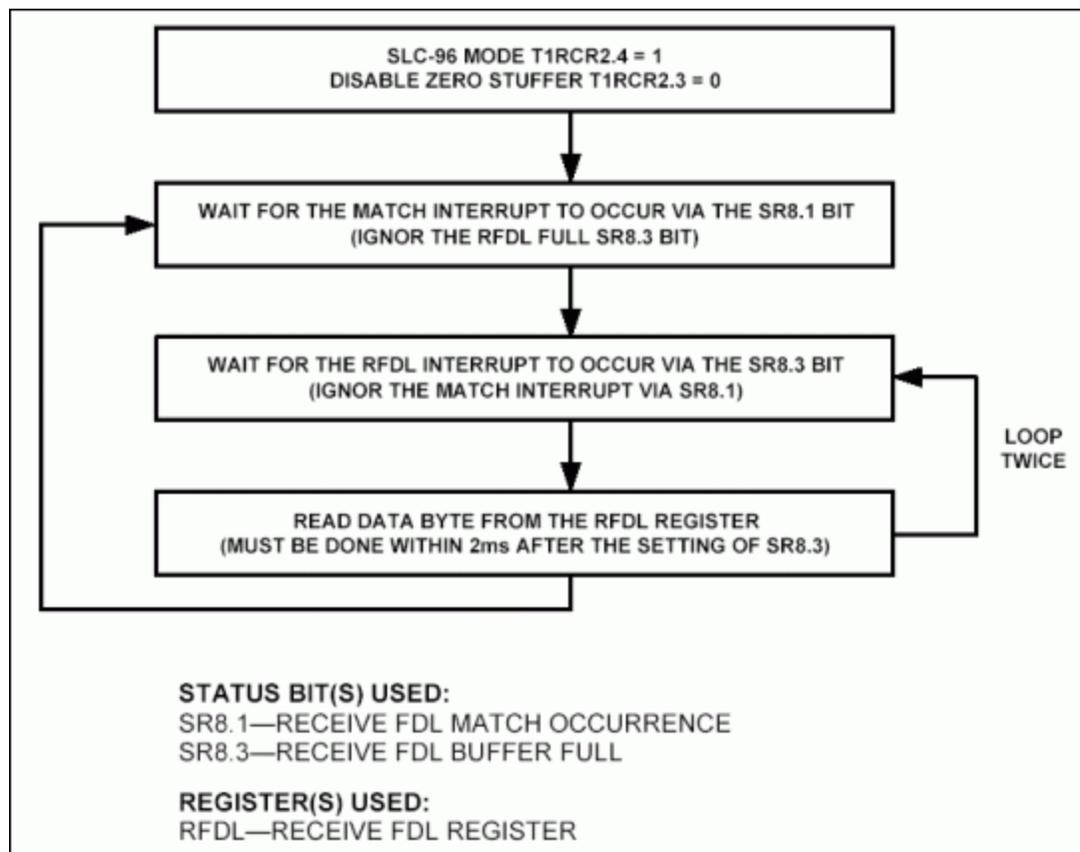

Figure 1. SLC-96 message field extraction via RFDL.

Table 1 details how the SLC-96 fields will be represented in the RFDL register on each read. Since the RFDL is also used in the ESF framing mode, the zero destuffer should be disabled (T1RCR2.3). (**Note:** The match registers (RFDLM1 and RFDLM2) are not used in SLC-96 mode and can be programmed with any value.)

Table 1. RFDL register byte sequence.

	(MSB)							(LSB)
READ #1	C8	C7	C6	C5	C4	C3	C2	C1
READ #2	M2	C1	S = 0	S = 1	S = 0	C11	C10	C9
READ #3	S = 1	S4	S3	S2	S1	A2	A1	M3

Transmit-Side SLC-96 Applications

To insert the SLC-96 message fields, the user has the option to either use the external TLINK pin or to

use the on-board TFDL register. Using the TLINK pin requires some external hardware. To enable this option, the T1TCR1.2 bit should be set to one. This application note refers solely to the use of the TFDL register to insert the SLC-96 message fields.

Figure 2 displays the method to enable the DS2155, DS21Q55, or DS2156 to insert the SLC-96 message fields via the TFDL register. On each normal D4 multiframe boundary, the framer signals to the user via the SR4.4 bit to write to the TFDL the sequence of bytes shown in **Table 2**. The user will write to the TFDL six times in each SLC-96 multiframe.
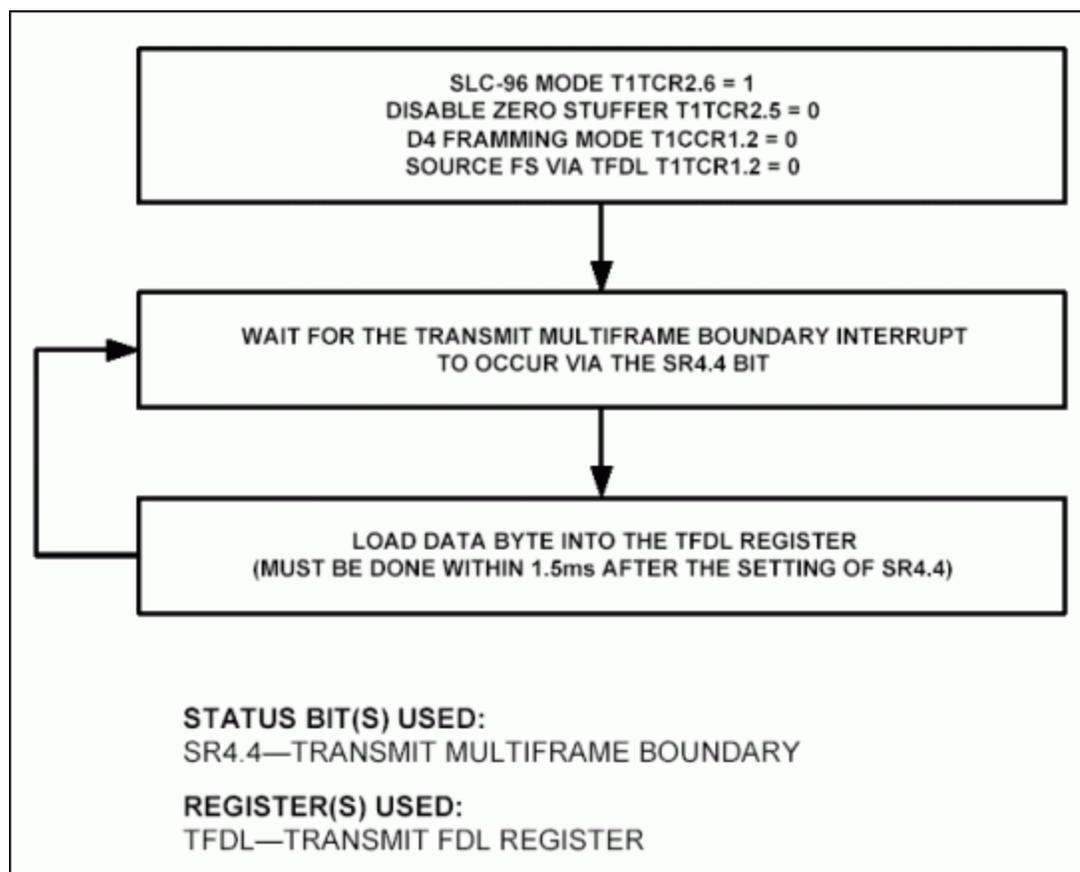

Figure 2. SLC-96 message field insertion via TFDL.

Table 2. TFDL register byte sequence.

	(MSB)						(LSB)
Write #1	X	X	C1	1	1	1	0	0
Write #2	X	X	C7	C6	C5	C4	C3	C2
Write #3	X	X	S = 1	S = 0	C11	C10	C9	C8
Write #4	X	X	A2	A1	M3	M2	M1	S = 0
Write #5	X	X	0	S = 1	S4	S3	S2	S1
Write #6	X	X	0	1	1	1	0	0

DS2155/DS21Q55/DS2156 Information

For more information about the Dallas Semiconductor's T1/E1 single-chip transceivers, please consult the data sheets available on our website at www.maximintegrated.com/telecom.

If you have further questions concerning the operation of our T1/E1 single-chip transceivers, please contact the Telecommunication Applications support team.

Related Parts		
DS2155	T1/E1/J1 Single-Chip Transceiver	Free Samples
DS2155	T1/E1/J1 Single-Chip Transceiver	Free Samples
DS2156	T1/E1/J1 Single-Chip Transceiver TDM/UTOPIA II Interface	Free Samples
DS2156	T1/E1/J1 Single-Chip Transceiver TDM/UTOPIA II Interface	Free Samples
DS21Q55	Quad T1/E1/J1 Transceiver	
DS21Q55	Quad T1/E1/J1 Transceiver	

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