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TUTORIAL 727

Filter Design Using Integrator Blocks

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Abstract: This application note explains a method that uses integrator blocks and some simple mathematical manipulation to produce filter responses of any order. The method is precise, easy to apply, and an alternative to a "standard" set of filter networks when a nonstandard filter response is needed.

Introduction

Much literature and software has been published on the design and implementation of standard filter responses. When a nonstandard filter response is required, it is often left to the circuit designer to produce a solution using his or her own "standard" set of filter networks. However, there is an alternative to this approach, a method that is precise, easy to apply, and uses integrator blocks and some simple mathematical manipulation to produce filter responses of any order.

Filter Design Method

The system uses simple op-amp integrator blocks, an example of which is shown in **Figure 1**. The method can be applied to both continuous-time and switching-filter (e.g., switched capacitor filter) designs.

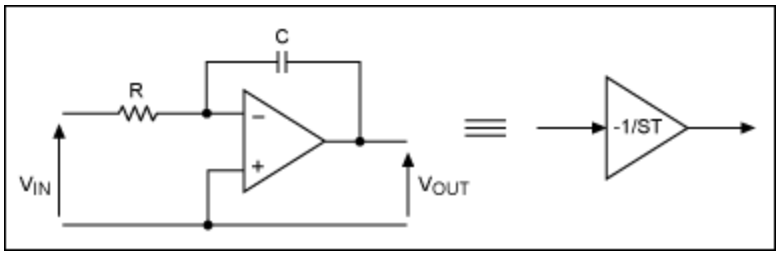

Figure 1. Op-amp-based (linear) integrator circuit block and symbolic representation.

The transfer functions of the integrator in Figure 1 and its symbolic representation are shown in the expression in **Figure 2**. The response (output) of this circuit to the input voltage is gain diminishing with frequency at a rate of 6dB per octave with unity gain occurring at a frequency in hertz of $1/2\pi CR$.

$$\frac{V_{OUT}}{V_{IN}} = \frac{-1}{SCR} = \frac{-1}{ST}$$

Where S is the complex frequency term of the Laplace transform and is given by the formula:

$S = j\omega$

Figure 2. Transfer function of the integrator circuit block in Figure 1.

Application of the Technique

The design process starts with the required filter transfer function. The equation in **Figure 3**, which represents a second-order lowpass-filter response, will be used for illustration. The technique can be employed for any filter type and is easily extended to higher order systems.

$$\frac{V_{OUT}}{V_{IN}} = \frac{\omega_0^2}{S^2 + S\frac{\omega_0}{q} + \omega_0^2}$$

Figure 3. Transfer function of a second-order filter with lowpass response.

A sequence of mathematical steps is then applied to the transfer function to obtain an expression of the form:

$$V_{OUT} = f(V_{IN}, V_{OUT}, 1/S)$$

Note that all frequency-dependent terms (occurrences of S) in the resulting expression must appear in the denominator terms. This is because the final circuit will be composed of integrators, i.e., functions of 1/S. Three basic mathematical steps are required. The expression obtained at each stage is given below.

Step 1. Cross-Multiply to Obtain

$$S^2 \times V_{OUT} + \omega_0/q \times S \times V_{OUT} + \omega_0^2 \times V_{OUT} = \omega_0^2 \times V_{IN}$$

Step 2. Divide by the Highest Power of S to Obtain

$$V_{OUT} + [(\omega_0/q) \times V_{OUT}]/S + (\omega_0^2 \times V_{OUT})/S^2 = \omega_0^2 \times V_{IN}/S^2$$

Step 3. Rearrange to Obtain an Expression for V_{OUT}

$$V_{OUT} = V_{IN} \times (\omega_0^2/S^2) - V_{OUT} \times (\omega_0^2/S^2) - V_{OUT} \times [(\omega_0/q)/S]$$

The equation produced in Step 3 is now the defining equation for a network of integrator blocks that will perform the required filtering function.

The remaining two design steps are somewhat intuitive, but the rules are simple. First, an integrator network drawing is produced. This uses a number of integrators and summing nodes to produce a network described by the defining equation in Step 3. To produce this network, start by considering the form of the defining equation. This expresses the output voltage (V_{OUT}) in terms of functions of V_{OUT} and V_{IN},where each function is a product of one or more integrator terms.

Considering these terms from left to right, the first term is a function of V_{IN} and two integrator stages ($1/S^2$). The signal V_{IN} must, therefore, pass through two integrator blocks before emerging at V_{OUT}. The first step in producing the diagram is then to draw V_{IN} supplying two integrator blocks in series, with the output of the second integrator connected to V_{OUT}. The second term is also a function of two integrator stages, but this time the integrator blocks are fed from the V_{OUT} signal. Furthermore, the coefficient of $1/S^2$ for both of these first two terms is the same, ω_0^2, so it is reasonable to have the source voltages for both of the first two terms sharing a common path to the output. A summing junction is, therefore, inserted before the first integrator stage and supplied by connections to both V_{IN} and V_{OUT}. The third

term of the equation is a function of V_{OUT} and a single integrator stage. To depict this, V_{OUT} must also be fed to the input of the second integrator block. This is done by inserting a second summing junction, this time before the second integrator block, with inputs taken from the first integrator block and from V_{OUT}.

To complete the network, the correct sign, inverting or noninverting, must be allocated to each summing-junction input. The transfer function of the integrator shown in Figure 1 is of the form -1/ST, so the integrator blocks will have a signal inversion built in. Signs are allocated to the summing junctions working from the output back toward the input. The third term in the equation of Step 3 shows that the feedback path from V_{OUT} through the second summing junction and the second integrator and back to V_{OUT} should be inverting. Because the integrator already contains an inversion, the input to the second summing junction from V_{OUT} should be noninverting. By similar analysis, it can be seen that, as the first term of the defining equation is positive, the path from V_{IN} to V_{OUT} should be noninverting. Because both integrators invert the signal, the result is a noninverting path if the inputs to the first and second summing junctions, i.e., from V_{IN} and the first integrator block, respectively, are each noninverting. Note that this would also apply if both inputs were inverting. As we shall see in the final design stage, however, the natural form of the simple integrator circuit is that of a noninverting summing junction followed by an inverting integrator. The integrator diagram is completed by allocation of a sign to the final summing-junction input, that is from V_{OUT} to the first summing junction. This is given by the second term in the defining equation, which is negative. Because the path through both integrators is noninverting, the required inversion must be placed at the input of the signal to the first summing from V_{OUT}. The resulting network for the defining equation of Step 3 is shown in **Figure 4**.

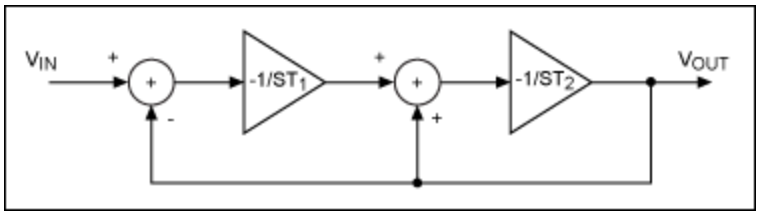

Figure 4. Integrator network representing the defining equation of Step 3.

The integrator time constants, T_1 and T_2 can now be assigned. From the integrator network, derivation and analysis of the third term of the defining equation we find:

$$-\omega_0/qS = -1/ST_2 \rightarrow T_2 = q/\omega_0$$

Similarly, from the first and second terms of the defining equation we find:

$$\omega_0^2/S^2 = 1/S^2T_1T_2 \rightarrow T_1 = 1/\omega_0^2T_2 = 1/\omega_0 q$$

Values for ω_0 and q are then chosen and the time constants T_1 and T_2 calculated as follows:

$$\begin{pmatrix} \omega_0 = 10000\text{rad/s} \\ q = 1/\sqrt{2} \end{pmatrix} \rightarrow \begin{pmatrix} T_2 = 7.071\mu s \\ T_1 = 14.14\mu s \end{pmatrix}$$

The final step is to translate the integrator network of Figure 4 into an operational amplifier/resistor/capacitor circuit. A standard, inverting, op-amp integrator block, comprising an op amp, a feedback capacitor, and an input resistor, is equivalent to a single (noninverting) summing node followed by an (inverting) integrator. Multiple input summing nodes are then accommodated by the addition of more input resistors to the op-amp integrator block.

The circuit in **Figure 5** shows the resulting active filter circuit, constructed from op-amp integrator blocks built around the MAX4322 op amp. The values given for R_1, R_2, C_1, and C_2 produce values for T of 14.96µs and 7.05µs, respectively. The gain response of the filter is shown in the plot of **Figure 6**.

Note the trick with the feedback to IC_1. Strict reproduction of the network in Figure 2 would have required an inverter to be placed in the feedback to the first summing node. Applying feedback directly from V_{OUT} to the noninverting input of IC_1 generates a signal at the output of IC_1 of (V_{OUT} + V_{OUT}/ST_1), which provides the necessary integrating output plus a duplicate of the signal applied from V_{OUT} to the second summing node. Removing the feedback path to the second summing node restores the correct transfer function.

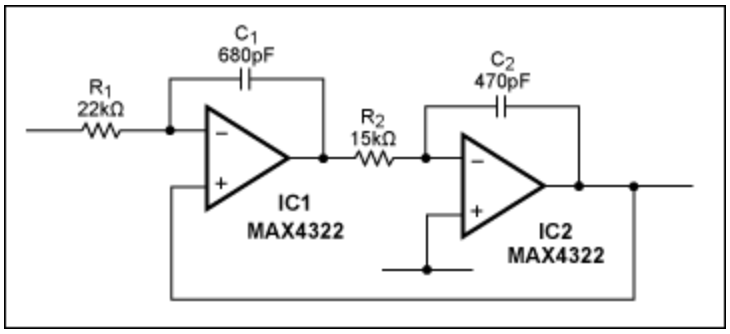

Figure 5. Circuit realization of the integrator network in Figure 2.

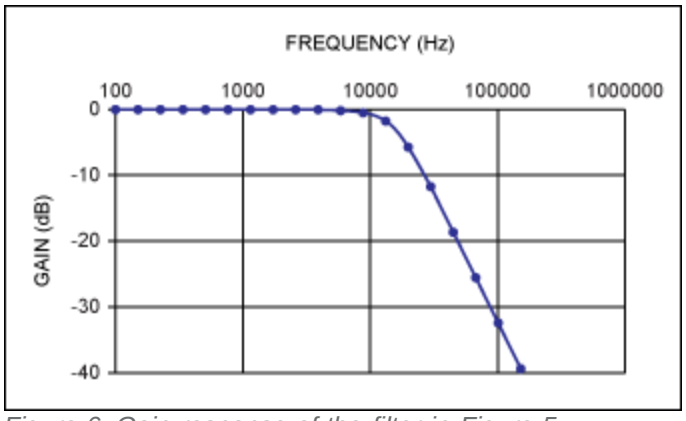

Figure 6. Gain response of the filter in Figure 5.

The above example can be implemented using a simple, dual-op-amp IC and a handful of passive components. Where higher order systems are being considered, the overall design task can be simplified considerably by the use of multistage filter ICs. Two examples of this type of component are the MAX274/MAX275. These devices provide, respectively, fourth- and eighth-order continuous-time filtering based on a series of integrator blocks. The filter time constants for these devices are defined by external resistor values only, as the feedback capacitor for each integrator stage is provided on-chip.

If the designer wishes a higher degree of programmability for the filter design, then a switched-capacitor-filter approach may well be suitable. There are switched-capacitor building-block ICs available that can be adjusted with a programmable clock or resistors. Some parts are also available with microprocessor-interface capability. The MAX260 and MAX268 families of switched-capacitor-filter building-block ICs provide a full range of control methods for anyone looking for programmable filtering functions.

The design process described here is powerful and versatile. It can be applied to virtually any active

filtering requirement and to functions of any order. In addition, the resulting implementation of simple integrator blocks eases the selection and the tolerance issues for components. Some active-filter implementations exacerbate the effects of basic component tolerances, whereas the integrator approach produces the same basic tolerance susceptibility as that furnished by a passive LCR filter circuit. Further, the effects of op-amp-bandwidth variation are relatively simple to calculate, because the (desired) operating unity-gain bandwidth of each integrator block is simply given by $1/T$ rad/s = $1/2\pi RC$ Hz.

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