30V, Dual Output Regulator Controller is Efficient, Rich in Features, and Saves Space

by Teo Yang Long and Theo Phillips

Introduction

The LTC3802 is designed to excel in generating low output voltages from high input voltages, a common problem for the power supplies of fast CPUs. It is the latest in Linear Technology's family of high speed, voltage feedback, synchronous step-down regulator controllers. It retains the constant frequency architecture and Burst Mode® operation of the LTC1702A, while improving on its performance and adding features (see Table 1).

The input supply operating range is extended from a nominal 5V to the entire 3V–30V range. The internal reference voltage has decreased, allowing the output to go as low as 0.6V. An advanced modulation scheme facilitates these low duty cycles and fast switching frequencies. The two channels are still run 180° out of phase—effectively doubling the frequency of the switching pulses seen by the input bypass capacitor and thereby lowering its RMS current and reducing its required value—but a new PLLIN pin extends these benefits by allowing two LTC3802s to control a 4-phase converter. This pin also allows external synchronization of the switching frequency from 330kHz–750kHz, rather than a fixed 550kHz. Output voltage tracking governs the 2 channels' output slew rate during power up and power down, to comply with various power sequencing requirements.

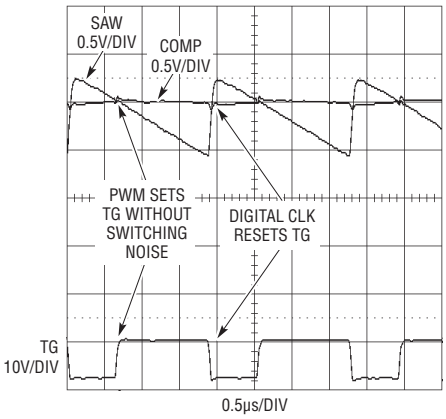

Figure 1. Leading edge modulation architecture PWM switching waveform for V_{IN} = 5V, V_{OUT} = 3.3V

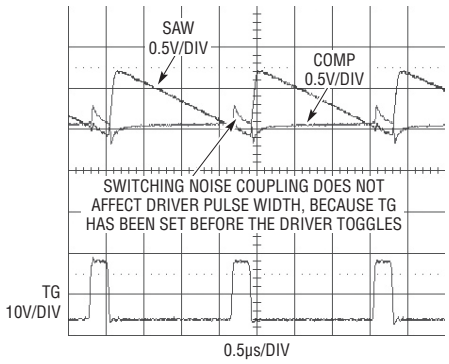

Figure 2. In a 20V to 3.3V buck converter, switching noise couples to the error amplifier output after the top gate (TG) turns on; this would cause unpredictable switching in traditional PWM converters.

Leading Edge Modulation

The LTC3802 uses a high switching frequency and precision voltage feedback architecture to provide exceptional regulation and transient response performance at each of its two outputs. The 10MHz gain-bandwidth feedback op-amps permit loop crossover in excess of one-tenth the switching frequency, whether that frequency is externally synchronized or running at the default 550kHz. Large integrated gate drivers allow the LTC3802 to control multiple MOSFETs efficiently throughout its range of switching frequencies.

A typical LTC3802 application down converts a high input voltage source to two low output voltage supplies and requires the two channels to run at low duty cycles. Such an application presents several challenges to a traditional PWM controller. First, the controller is forced to make a decision about pulse width after the control switch (top MOSFET) turns on. The turn-on of the control switch in the buck converter is the noisiest event in the whole switching cycle. The input supply current jumps from zero current to the loaded current, causing ground bounce; the large voltage swing at the inductor flying node can further induce noise in the controller. Either event can disrupt

Table 1. Comparison of the LTC3802 and the LTC1702/LTC1702A

	LTC3802	LTC1702/LTC1702A
V_{IN}	3V–30V	3V–7V
Switching Architecture	Leading Edge Modulation with Line Feedforward Compensation	Trailing Edge Modulation
Reference	0.6V ±1%	0.8V ±1%
Phase Lock Loop	330kHz–750kHz PLL Free Run at 550kHz	No Free Run at 550kHz
Tracking	Ratiometric or Coincident Power Up and Power Down Tracking	No
Packages	GN28 and QFN 32	GN24

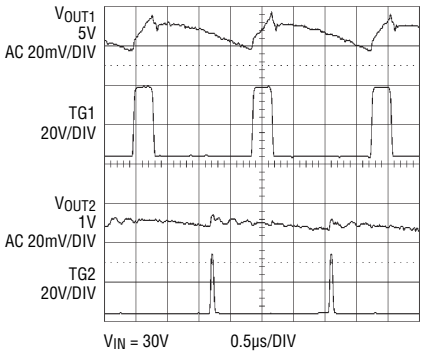

Figure 3. Switching waveform obtained from the LTC3802 dual out of phase buck converter

the operation of the PWM comparator within the first 100ns–200ns after the transition, producing random control pulse width variations and irregular inductor current ripple.

The second challenge to the traditional PWM operating scheme is that the PWM comparator response time limits the controller's minimum pulse width. A typical PWM comparator takes at least 100ns to toggle the output. This sets the minimum top gate on-time for the switcher. Third, traditional trailing edge modulation suffers from slow transient recovery. The internal clock turns on the control switch at a fixed time interval regardless of output voltage (V_{OUT}). If the load current jumps up after the top gate turns off, the controller must wait for the next clock cycle to charge up the output capacitor. In this situation, controllers with slower switching frequencies can have larger output droops.

The LTC3802 uses a leading edge modulation architecture to overcome these three obstacles. In a typical LTC3802 switching cycle, the PWM comparator turns on the top MOSFET; the internal master clock turns it off. The comparator makes a decision in a quiet interval before the MOSFETs toggle, avoiding pulse width jitter.

Figure 1 shows the leading edge modulation architecture PWM switching waveform. Figure 2 shows the noise at the error amplifier output due to relatively high input supply voltage—even with this noise, the LTC3802 maintains a stable switching waveform. At even lower duty cycles, the comparator's propagation delay no longer limits the minimum pulse width of the top gate; the switching

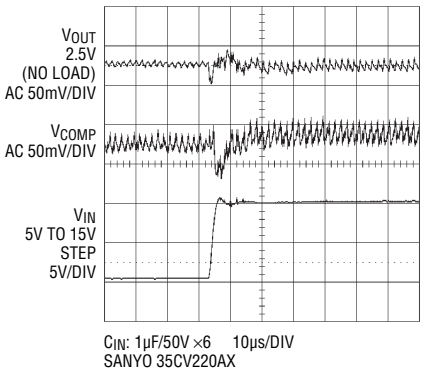

Figure 4. A large swing in V_{IN} produces a very small disturbance at V_{OUT}.

feedback loop adjusts the duty cycle to give the correct output voltage. Figure 3 shows the narrow TG pulse generated from a 30V to 1V buck converter. With a 550kHz switching frequency converter, the TG pulse width is only 60ns! The comparators in traditional PWM converters are not sensitive enough to permit such a narrow pulse width; otherwise they would be easily triggered by noise.

Leading edge modulation also yields fast load transient response. Once the output is loaded, the error

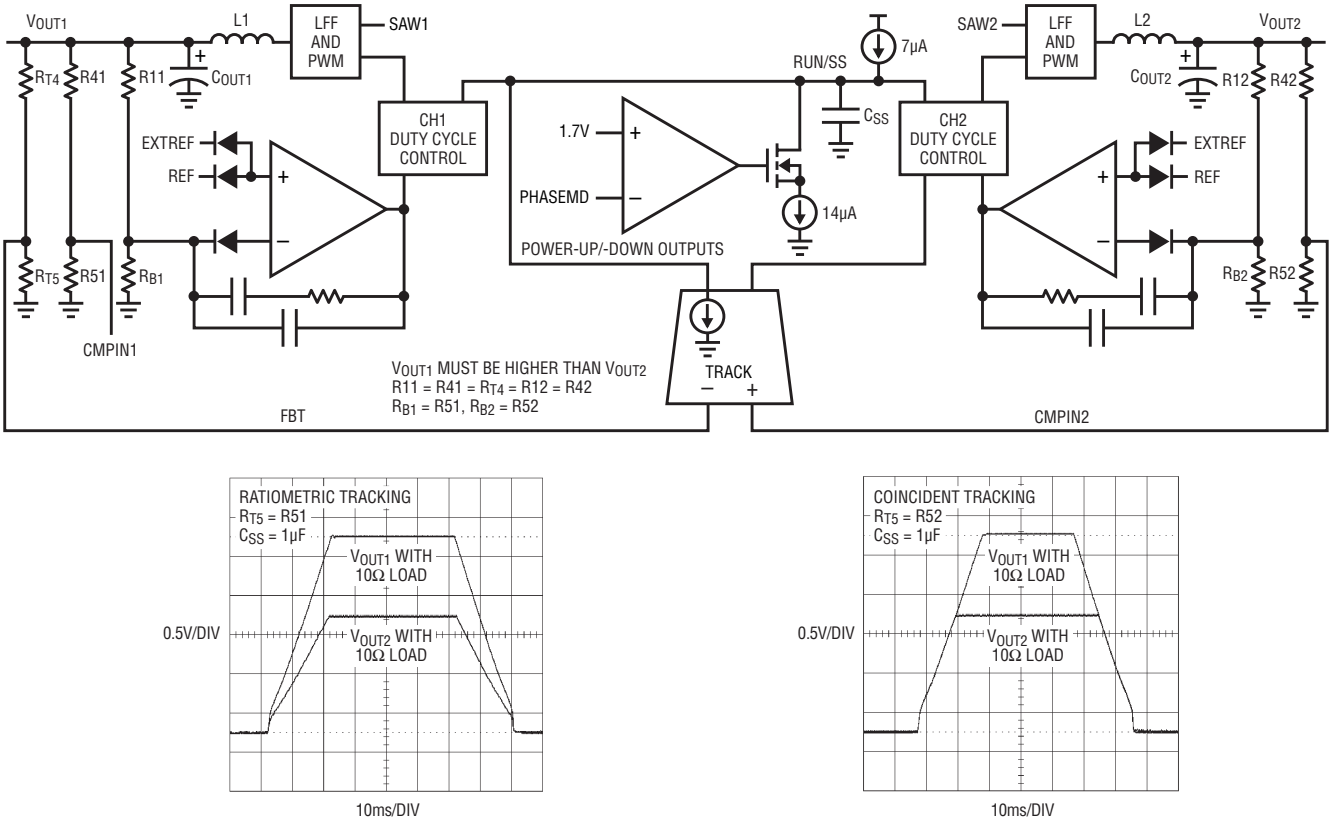

Figure 5. Simplified tracking schematic and associated power-up and power-down waveforms for ratiometric and coincident tracking

amplifier senses the output droop, and the controller immediately turns on the top MOSFET to replenish the output capacitor. The LTC3802 does not need to wait for the next clock cycle to enable the top gate. When the load is removed, the undershoot recovery time is determined by the error amplifier frequency compensation network. In either case, recovery times of well under 20µs are easily attained at a switching frequency of 550kHz. This fast transient response, combined with the low output ripple current produced at high switching frequencies, reduces the amount of output capacitance required to support the output voltage during a load transient.

The LTC3802 includes compensation for line transients. The line feedforward compensation input monitors the power supply (V_{IN}), immediately modulating the input to the PWM comparator and changing the pulse width in an inversely proportional manner. Instead of waiting for a droop in output voltage, feedforward compensation bypasses the feedback loop and provides excellent regulation during line transients (Figure 4).

Programmable Power Up, Power Down Tracking

Next generation power modules use power up, power down tracking to reduce the amount of external circuitry required to power up modern digital semiconductors, such as DSPs, microprocessors, FPGAs and ASICs. Such devices require at least two supply voltages, one to power the high speed core logic and another to power the I/O interface. These voltages must be applied in a well-controlled sequence.

During power-up and power-down, variations in the starting points and ramp rates of the supplies may cause current to flow between the isolation structures. When prolonged and excessive, these currents can shorten the life of the semiconductor devices, or trigger latch-up leading to device failure.

To meet these sequencing requirements, power system designers can avoid adding extra circuitry by using the LTC3802's easily programmable power up, power down tracking. The LTC3802 can adhere to two different schemes: ratiometric and coincident tracking.

With a ratiometric configuration, the LTC3802 produces two different output slew rates (with $V_{OUT1} > V_{OUT2}$). Because each channel's slew rate is proportional to its corresponding output voltage, the two outputs simultaneously reach their steady-state values.

The coincident configuration produces the same slew rate at both outputs, so that the channel with the lower V_{OUT} reaches its steady state value first.

Figure 5 shows the simplified schematic of how tracking is implemented. During power up or power down, the tracking amplifier, TRACK, servos the tracking feedback loop and forces

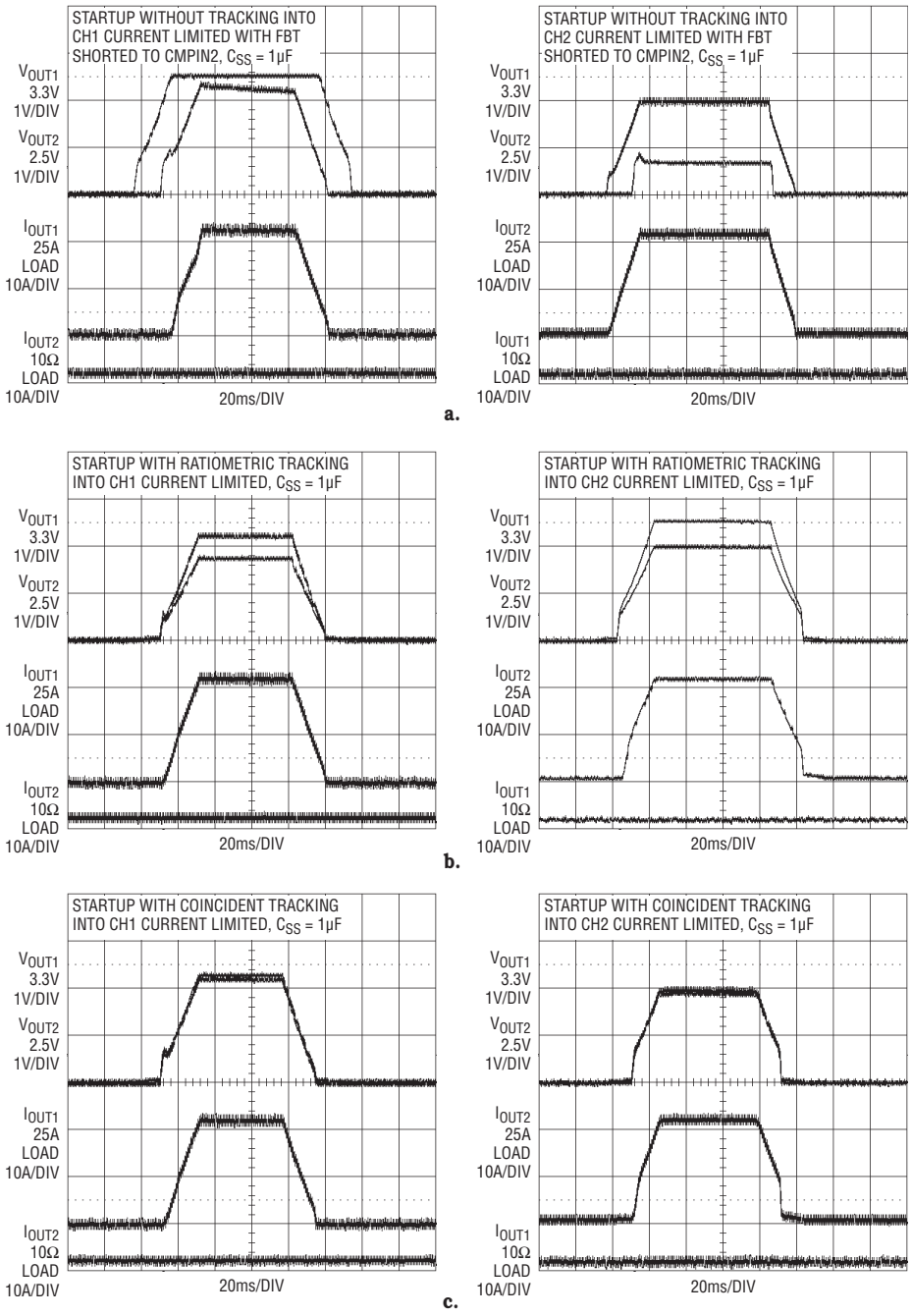

Figure 6. Power up and power down waveforms with one of the channels current limited. Results are shown without tracking (a), with ratiometric tracking (b), and with coincident tracking (c).

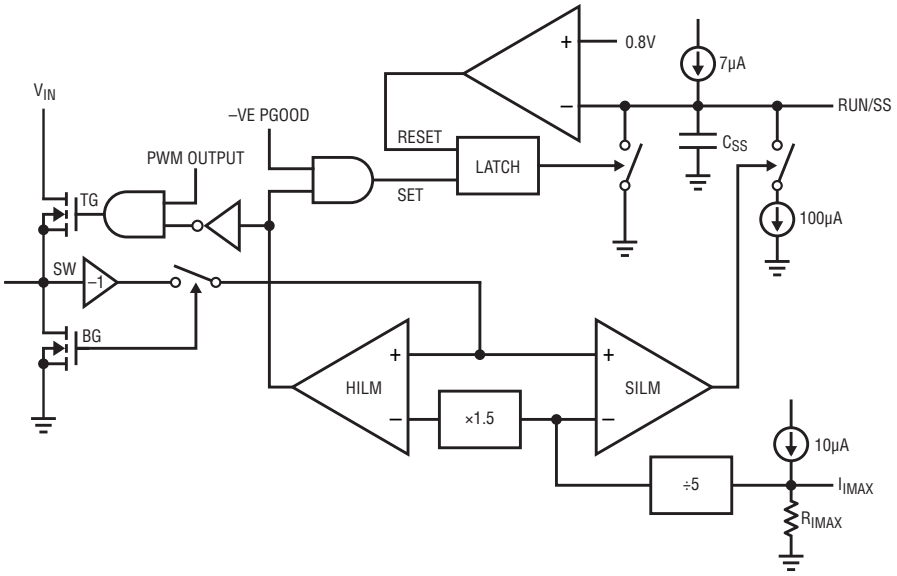

Figure 7. Simplified LTC3802 current limit circuitry

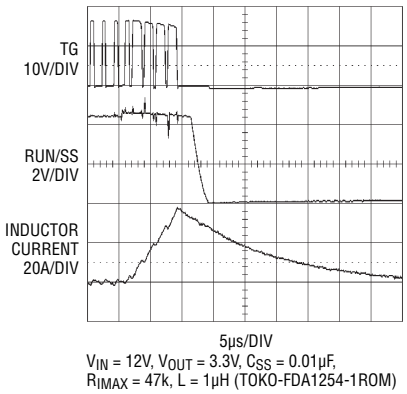

Figure 8. LTC3802 short circuit waveform

FBT to be at the same potential as CMPIN2. Setting R_{T5} = R51 creates the ratiometric startup, and setting R_{T5} = R52 produces the coincident start-up. The tracking function can be easily disabled by disconnecting the FBT resistive divider and shorting FBT to CMPIN2.

To have the proper power-down sequence, ground the PHASEMD pin. This turns on an internal current source that slowly discharges the soft-start capacitor. Once the RUN/SS potential is low enough to control the duty cycle, the tracking amplifier takes control and servos the tracking feedback loop to produce the selected output ramp. Note that in this tracking scheme, there is no master and slave assignment; if either output goes low, the other channel's output follows. Figure 5 includes the ratiometric and coincident tracking waveforms with 10Ω loads.

Figures 6a to 6c show the power up and power down waveforms with one of the channels current limited. Figure 6a shows that when FBT is shorted to CMPIN2, the tracking function is disabled. The first waveform shows that when channel 1 is current limited, channel 2's output potential is lowered due to the lower RUN/SS voltage (both channels share the same RUN/SS pin). The second photo shows that when channel 2 is current limited, channel 1's 3.3V output voltage is lower than nominal. Figures 6b and 6c show the output waveforms with ratiometric and coincident tracking. Figure 6b shows that for ratiometric tracking, if either output is current limited, the other output is pulled low such that both outputs maintain their voltage ratio. On the other hand, for the coincident Tracking configuration shown in Figure 6c, both channels have the same output voltages even if only one channel is current limited.

Current Limit

The LTC3802 bottom MOSFET current sensing architecture not only eliminates the external current sense resistors and the corresponding power losses in the high current paths, but also allows a wide range of output voltages, even at extremely low duty cycles.

The LTC3802's current limit scheme improves on that of the LTC1702A by employing a user-programmable current limit level. It works by sensing the V_{DS} drop across the bottom MOSFET when it is on and comparing that voltage to a programmed voltage at I_{MAX}.

The I_{MAX} pin includes a trimmed 10µA current, enabling the user to set the I_{MAX} voltage with a single resistor, R_{IMAX}, to ground. The current comparator reference input is equal to V_{IMAX} divided by 5 (see Figure 7). The current comparator begins limiting the output current when the voltage across the bottom MOSFET is larger than its reference. The current limit detector is connected to an internal 100µA current source.

Once current limit occurs, this current source begins to discharge the soft-start capacitor at RUN/SS,

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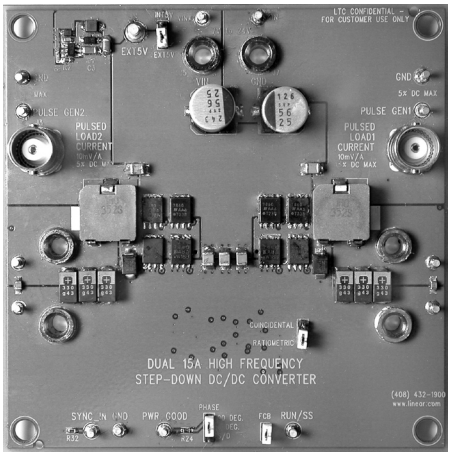
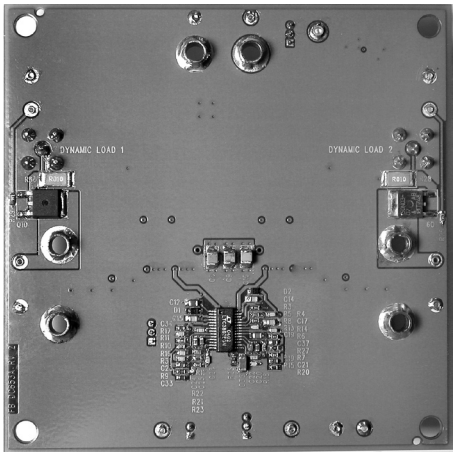


TOP



BOTTOM

Figure 9. An 87W, LTC3802 application circuit occupies less than 6in²

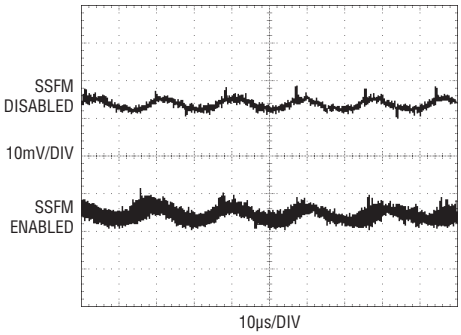


Figure 4. Output voltage ripple for 1.8V output using "envelope" oscilloscope function

Figure 4 shows the output voltage ripple for the circuit of Figure 1 with and without SSFM enabled. Note that since SSFM is constantly changing the LTC3736-1 switching frequency, it is difficult to show the true behavior of SSFM using a still oscilloscope snapshot—a video would be much more informative.

Nonetheless, the scope traces in Figure 4 have been acquired using the "envelope" oscilloscope function, which shows the leading and trailing waveform edges blending in with each other as the frequency is varied. The peak to peak ripple with SSFM enabled does increase slightly, but this is expected since output ripple is inversely proportional to switching frequency, and SSFM introduces some frequencies that are lower than the single fixed 550kHz frequency. Although it is not easily detected from this still snapshot, note that while the frequency is varying—one can think of SSFM as introducing frequency jitter—the duty cycle is constant. In other words, there is no duty cycle jitter or sub-harmonic instability with SSFM enabled on the LTC3736-1.

Figure 5 compares the efficiency of the circuit in Figure 1 with and without SSFM enabled. Figure 6 shows load step transients and Figure 7 shows tracking startup waveforms with SSFM enabled. In all cases, the behavior of the LTC3736-1 is unaffected by the addition of SSFM.

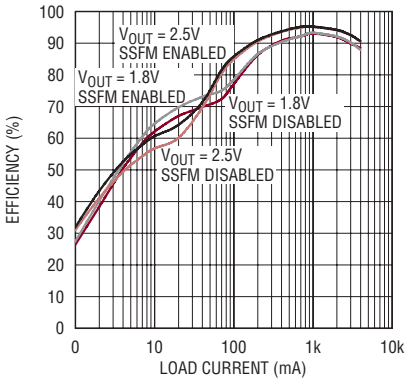


Figure 5. Efficiency for circuit of Figure 1. There is little difference with SSFM enabled

Conclusion

The LTC3736-1 is an easy-to-use dual synchronous switching DC/DC controller that requires few external components. Additionally, it features an internal spread spectrum oscillator that randomly varies the controllers' switching frequency, providing a simple solution to reduce power-supply-induced EMI that otherwise might require significant and costly troubleshooting and redesign.

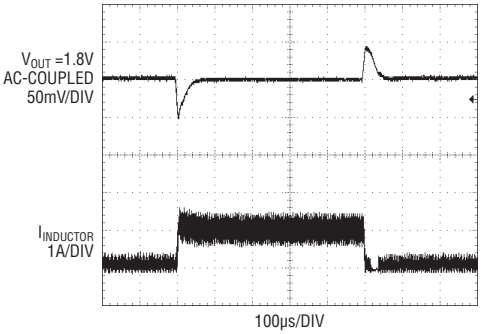


Figure 6. Load step response for circuit of Figure 1 with SSFM enabled

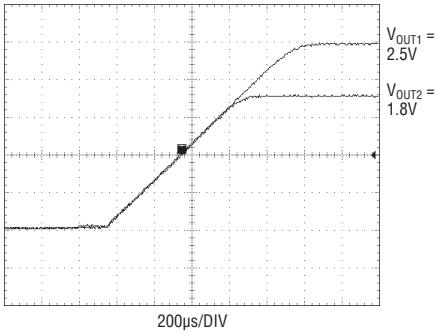


Figure 7. Startup of circuit of Figure 1 showing the two supplies tracking with SSFM enabled

LTC3802, continued from page 8

reducing the duty cycle and hence the output voltage until the current drops below the limit. The soft-start capacitor needs to move a fair amount before it has any effect on the duty cycle, adding a delay until the current limit takes effect. This allows the LTC3802 to experience brief overload conditions while maintaining output voltage regulation.

Nevertheless, at high input voltages, even a small RUN/SS time delay could cause the output current to overshoot badly during a severe short circuit. To avoid that situation, LTC3802 adds a hard current limit circuit.

If the load current is 1.5 times larger than the programmed current limit threshold, the LTC3802 shuts off the top MOSFET immediately. This stops the increase in the inductor current. At this moment, if CMPIN (which samples V_{OUT}) is 10% lower than its nominal value, the LTC3802 hard current-limit latches and discharges the RUN/SS capacitor with a current source of more than 1mA until RUN/SS hits its shutdown threshold. Once RUN/SS is completely discharged, the LTC3802 cycles its soft start cycle again. Figure 8 shows waveforms during a severe short circuit at the output of a 12V–3.3V converter.

Conclusion

The high efficiency LTC3802 is the latest member of Linear Technology's family of constant frequency, voltage feedback, synchronous N-channel controllers. With its unique set of powerful features and performance improvements (summarized in Table 1), it improves on the LTC1702/LTC1702A, and is ideal for high input voltage and low duty cycle applications. The LTC3802 is available in small 28-Lead SSOP and 32-Lead (5mm × 5mm) QFN Packages, allowing an entire 87W converter to be laid out in less than 6 square inches (Figure 9).