# Comparator Circuit Provides Automatic Shutdown of the LT1795 High Speed ADSL Power Amplifier by Tim Regan

### Introduction

Data transmission standards such as HDSL2, ADSL (both Full Rate and G.Lite) and VDSL (collectively known as xDSL) require the combined speed, output power and dynamic range capabilities of the LT1795 to drive the telephone line. In a typical data communications installation, in both the telephone central office and office building sites, hundreds of telephonewire pairs are brought together into a line multiplexer. These multiplexers compact the individual line driver and receiver circuits to save space. Eight lines per PC card are often implemented. This tight partitioning raises the challenges of both power and heat management in each installation.

A simple comparator circuit can be used to monitor the activity of an individual phone line and completely shut down the line driver when not in use. This provides a means of implementing activity-based power consumption with reduced overall heat generation.

#### **Controlling Power Dissipation**

The LT1795 is a dual, high speed, current feedback amplifier with high output current capability. With a

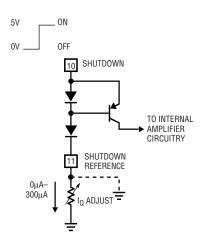


Figure 1. Shutdown/I<sub>Q</sub> adjust for the LT1795

50MHz Gain Bandwidth product, 900V/ms slew rate and an output stage that can source and sink 500mA, the LT 1795 is ideal for use as a low distortion differential line driver in very high data rate modem applications.

For the LT1795 to obtain full performance, a fair amount of quiescent operating current is required—typically 60mA. When supplied by  $\pm 15V$ power supplies to obtain maximum dynamic output range, the quiescent power dissipation with no load is typically 1.8 watts ( $30V \times 60mA$ ). In these applications, however, full performance is not required at all times or for all applications. To address this issue, the LT1795 provides the ability to completely shut down the driver or to tailor the quiescent operating current to match the actual requirements of a particular application. Figure 1 illustrates how this control is implemented.

Pins 10 and 11 of the LT1795 combine to control the operating current of the amplifiers. If the Shutdown Reference (pin 11) is grounded and the Shutdown input (pin 10) is driven to a voltage greater than two diode drops above ground, both amplifiers are biased to "full speed ahead" with maximum AC performance and also maximum quiescent power dissipation. The current through the two diodes shown in Figure 1 is internally limited to 300µA and results in 60mA of quiescent current for the amplifiers. Resistance can be added between the Shutdown Reference pin and ground to limit the maximum operating current of the amplifiers. This programmability can optimize the trade-off between AC performance (primarily slew rate and bandwidth) and quiescent package power dissipation. Many applications require the peak current drive capability of the LT1795 but do not need the full bandwidth and slew performance. Details of this control can be found on the LT1795 data sheet.

If the Shutdown input is grounded, both amplifiers are disabled and the total quiescent current drain for the package is reduced to only 200 $\mu$ A. This feature can be used to save a substantial amount of power when the line drivers are not in use at all times. A simple comparator circuit, as shown in Figure 2, provides a timed, automatic shutdown when no input signals are applied to the amplifiers.

#### **Timed Automatic Shutdown**

In this circuit, an LT1795 is configured as a unity gain differential driver for a  $100\Omega$  transformer-coupled wire pair. The two comparators in an LT1720 package monitor the signals on each of the input lines to the driver amplifier. If the signal on either input exceeds the threshold set by the sensitivity adjustment (shown to provide a range from 65mV to 500mV peak), the output of one or the other of the comparators goes high immediately and puts the LT1795 into action. The LT1720 comparators feature a propagation delay of only 4.5ns, allowing them to respond to input signals well beyond 10MHz in frequency.

The LT1720 outputs are wire-ORed through a simple timing network. When either output is high, timing capacitor  $C_T$  charges quickly to 5V through the diodes shown. While a signal is present, one or the other comparator output keeps  $C_T$  charged. The voltage on the timing capacitor is buffered by a third comparator, an LTC1440, to provide a sharp 0V to 5V shutdown/enable signal to the LT1795.

## ✓ DESIGN IDEAS

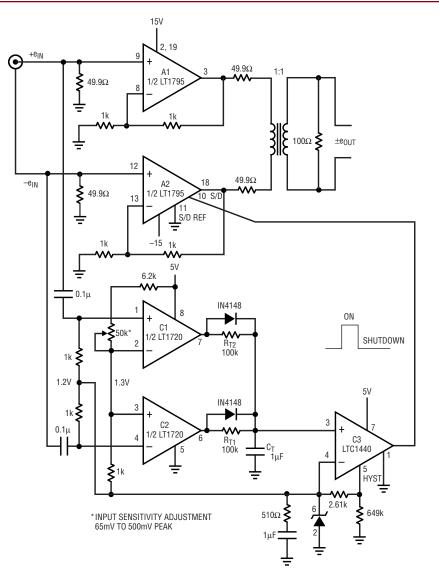


Figure 2. Automatic shutdown of the LT1795 power amplifier

The LTC1440 is a CMOS comparator with a built-in voltage reference and programmable hysteresis. The 1.18V reference is used for DC biasing to set a stable input threshold for the circuit. The input current of this comparator, 10pA, does not present a significant load on the timing capacitor. When the signals of both inputs to the driver amplifier drop below the threshold, both outputs of the LT1720 go low. While low, the timing capacitor discharges exponentially through the two 100k resistors,  $R_{T1}$  and  $R_{T2}$ . If the voltage on  $C_T$  is given time to discharge below the 1.18V threshold of the LTC1440—that is, when no further signals are applied to the input of the circuit—the output of the LTC1440 snaps low and immediately shuts down the LT1795 power amplifier. The discharge voltage of  $C_T$  is fairly slow moving but the input hysteresis set between pins 4 and 5 of the LTC1440 allows a clean ON-to-OFF transition.

With the component values provided in Figure 2, the circuit "wakes up" and properly amplifies the input signal in approximately 50 $\mu$ s. Most of this delay is in the charging of C<sub>T</sub> and the propagation delay of 8 $\mu$ s through the LTC1440. With the Shutdown pin driven high, the LT1795 is fully up to speed in only 1 $\mu$ s. For a DSL application, this wake-up time occurs during the initial line "training-up" interval of the data transmission sequence.

When the input signal is removed,  $C_T$  discharges in approximately 65ms to put the driver into a low power dissipation state until the next data transmission. This time-out interval and wake-up time can be easily tailored through the selection of  $C_T$  and  $R_{T1}$  and  $R_{T2}$ . If the two timing resistors are of equal value, the OFF time interval is set by the relationship: t =  $0.713 \cdot R_{TX} \cdot C_T$ .

#### Conclusion

This simple comparator sensing and timing circuit provides automatic control over the power dissipation of a high speed power amplifier line driver. With no signal present there is no wasted quiescent power. This same system enhancement can also be achieved through direct logic control of the LT1795 shutdown feature. This would require a 0V to 5V control signal for each line, which is set or cleared in synchronization with each data transmission interval.

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