Versatile Dual Hot Swap Controller/ Power Sequencer Allows Live Backplane Insertion

by Bill Poucher

Introduction

When a circuit board is inserted into a live backplane, the supply bypass capacitors on the board can draw large transient currents from the backplane power bus as they charge. These transient currents can destroy capacitors, connector pins and board traces and can disrupt the system supply, causing other boards in the system to reset. The new dual-channel LTC1645 Hot Swap controller is designed to ramp a circuit board's supply voltages in a controlled manner, preventing glitches on the system supply and damage to the board.

The LTC1645's two channels can be set to ramp up and down separately, or they can be programmed to rise and fall simultaneously, ensuring power supply tracking at the two outputs. Using external N-channel pass transistors, the supply voltages can be ramped at a programmable rate. Two high-side switch drivers control the external N-channel FET gates for supply voltages ranging from 1.2V to 12V. Programmable electronic circuit breakers protect against shorts at either output. The LTC1645 is available in the 14-pin and 8-pin SO packages. The 14-pin version additionally provides a system reset signal and a second "spare" comparator to indicate when board supply voltages drop below user-programmable levels. It also has a fault signal to indicate an overcurrent condition and a timer pin to create a delay before ramping up the supply voltages and deasserting the system reset signal.

Typical Hot Swap Application

Figure 1 shows a typical Hot Swap application using the LTC1645. Q1 and Q2 control the board's power supplies, R_{SENSE1} and R_{SENSE2} provide current fault detection and R1 and R2 prevent high frequency oscillation. By ramping the gates of the pass transistors up and down at a controlled rate, the transient surge current (I = C • dv/dt) drawn from the main backplane supply is limited to a safe value when the board makes connection.

The timing for the board is shown in Figure 2. When power is first applied to the chip, the gates of the FETs (GATE1 and GATE2 pins) are pulled low. Once the ON pin rises at time point 1, the LTC1645 must complete a timing cycle before the GATE pin voltages are allowed to rise. This allows the connector pins to finish bouncing and make a solid connection. C_{TIMER} charges to 1.23V with a 2µA current source, setting the delay timing cycle equal to t = (1.23V • C_{TIMER})/2µA. In this example, the undervoltage lock-

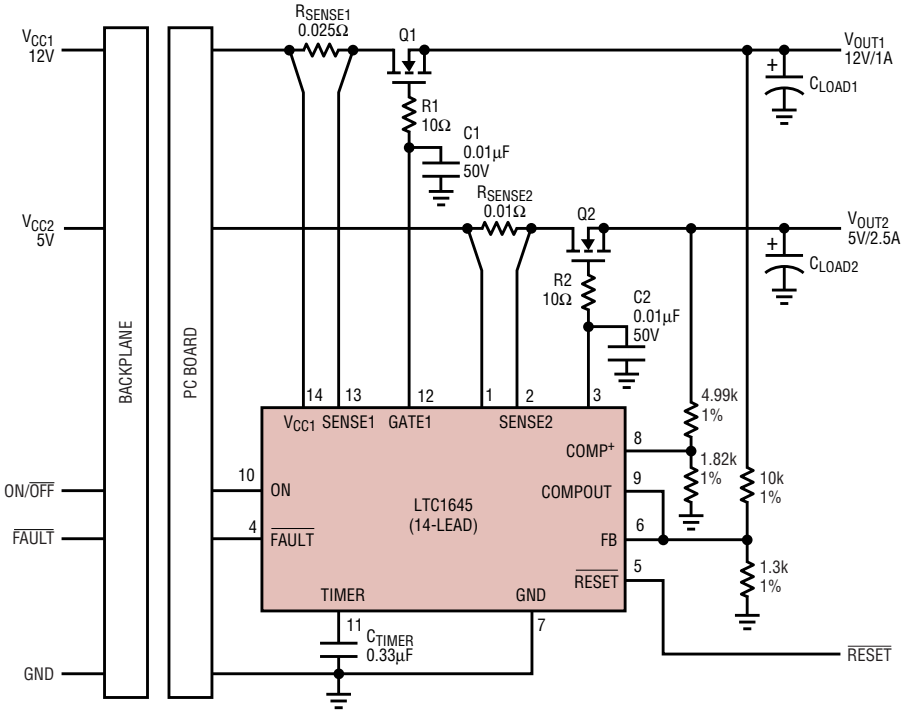

Figure 1. LTC1645 typical application

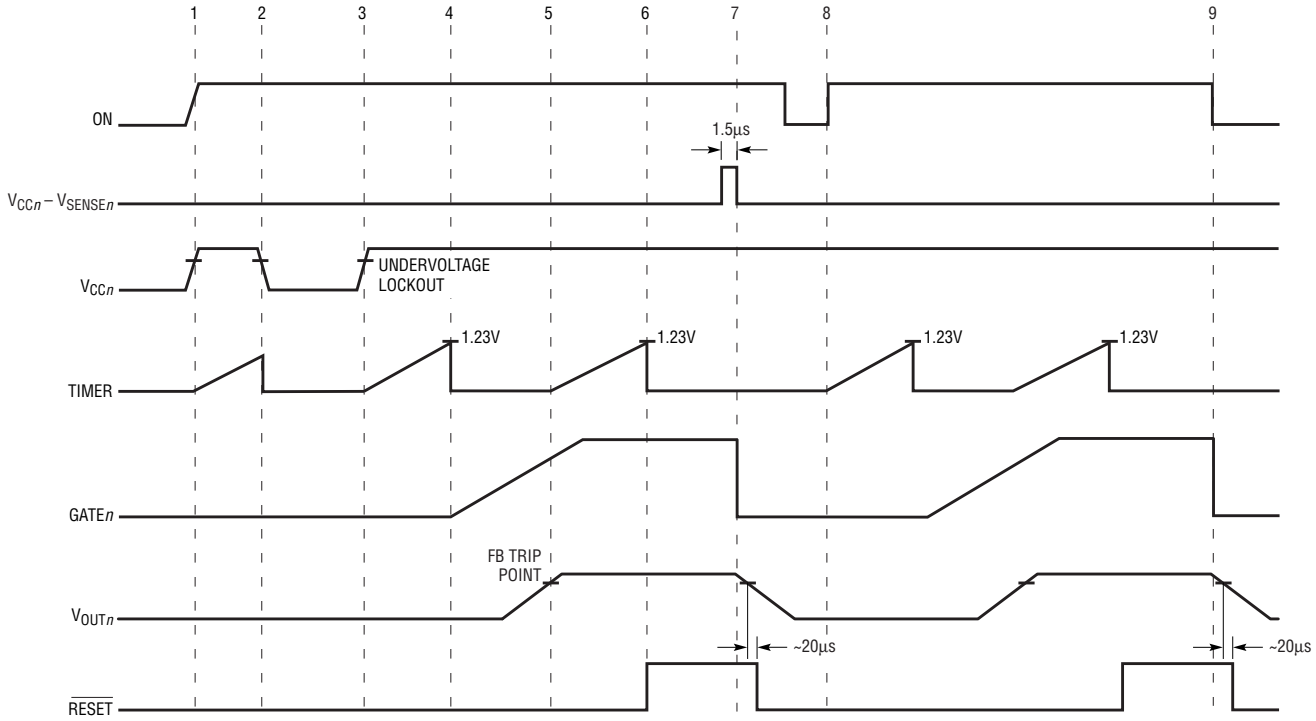

Figure 2. Typical insertion and electronic-circuit-breaker timing

out circuit discharges the TIMER pin and prevents both channels from turning on when $V_{CC1} < 2.23V$ or $V_{CC2} < 1.12V$ (time point 2). At time point 4, the timing cycle is completed and the GATE pins are pulled up by an internal 10µA current source; the voltage at GATE1 begins to rise with a slope of 10µA/C1 and the voltage at GATE2 begins to rise with a slope of 10µA/C2. The supply voltages follow their respective gate voltages minus the external FET threshold voltage; the ramp time for each supply is $(V_{CCn} \bullet Cn)/10\mu A$.

Voltage Monitor and Spare Comparator

The 14-pin version of the LTC1645 provides two precision comparators for monitoring input or output voltage levels. Both comparators have a 1.238V reference as the negative input and have open-drain outputs that require an external pull-up to generate a logic high. The spare comparator monitors COMP+ and releases COMPOUT immediately whenever COMP+ is above 1.238V. The FB comparator releases RESET one timing cycle after the FB pin rises above 1.238V (Figure 2, time points 5 and 6) and includes a glitch filter to prevent system resets during short negative transients on the FB pin. The filter time is 20µs for large transients (greater than 150mV) and up to 100µs for smaller 10µA transients.

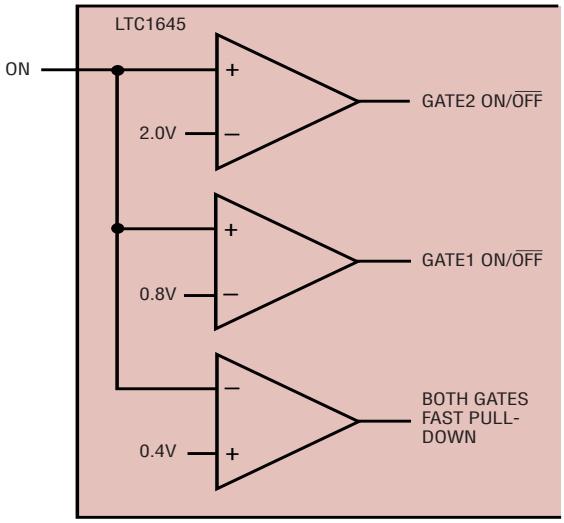

Figure 3. On-pin operation

In Figure 1, the COMPOUT pin has been tied to the FB pin so that RESET will not release until both output supplies remain above their programmable voltages for one timing cycle.

Electronic Circuit Breaker

The LTC1645 features an electronic circuit breaker function that protects against short circuits or excessive output current. Load current for each supply is monitored by a sense resistor between the supply input and sense pin of the chip. The circuit breaker trips whenever the voltage across the sense resistor exceeds 50mV for more than 1.5µs. When the circuit breaker of either channel trips, both GATE pins are immediately pulled to ground and the external FETs are quickly turned off (Figure 2, time point 7). When the ON pin is cycled off and on (time point 8), the circuit breaker resets and another timing cycle starts. If the circuit breaker feature is not required, short the SENSE pins to their respective V_{CC} pins.

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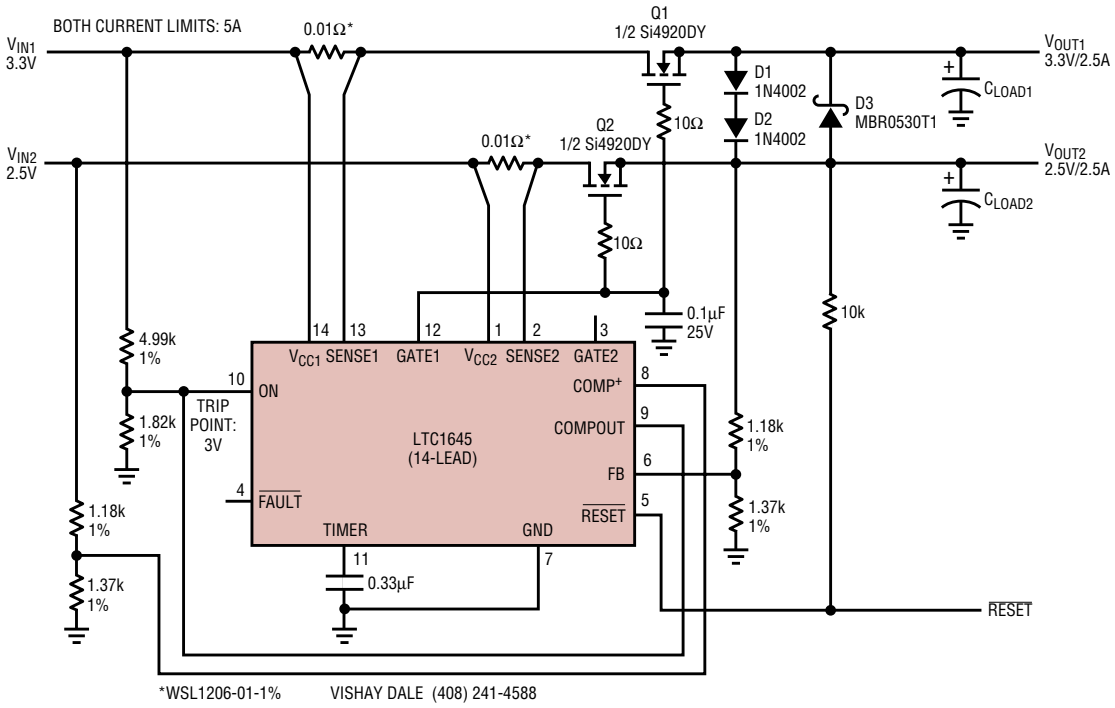

Figure 4. Ramping 3.3V and 2.5V up and down together

The ON Pin

The ON pin has multiple thresholds to control the ramping up and down of the GATE*n* pins. Figure 3 is a block diagram showing operation of the ON pin. If the ON pin voltage is below 0.4V, GATE1 and GATE2 are immediately pulled to ground. While the voltage is between 0.4V and 0.8V, GATE1 and GATE2 are each pulled to ground with a 40µA current. Between 0.8V and 2V, the GATE1 10µA pull-up is turned on after one timing cycle, but GATE2 continues to be pulled to ground with a 40µA current. When the voltage exceeds 2V, both the GATE1 and GATE2 10µA pull-ups are turned on one timing cycle after the voltage exceeds 0.8V.

Power Supply Tracking and Sequencing

Some applications require that the difference between two power supply voltages not exceed a certain value. This requirement applies during power-up and power-down, as well as during steady state operation; often this is done to prevent latch-up in a dual-supply ASIC. Other systems require one supply to come up after another, for example, when a system clock needs to start before a block of logic. Typical dual supplies or backplane connections may come up at arbitrary rates depending on load current, capacitor size, soft-start rates and so on. Traditional solutions can be cumbersome or require complex circuitry to meet the necessary requirements.

The LTC1645 provides simple solutions to power supply tracking and sequencing needs. The LTC1645 can guarantee supply tracking by ramping the supplies up and down together and allows nearly any combination of supply ramping to satisfy various sequencing specifications. Figure 4 shows an application ramping V_{OUT1} and V_{OUT2} up and down together. The ON pin must reach 0.8V to turn on GATE1, which ramps up V_{OUT1} and V_{OUT2}. The spare comparator pulls the ON pin low until V_{CC2} is above 2.3V, and the ON pin cannot reach 0.8V before V_{CC1} is above 3V.

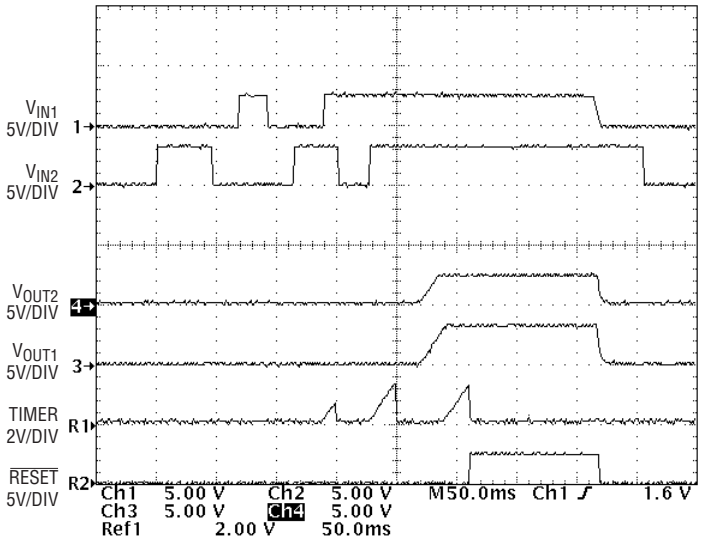

Figure 5. Input, output and control signals of Figure 4's circuit

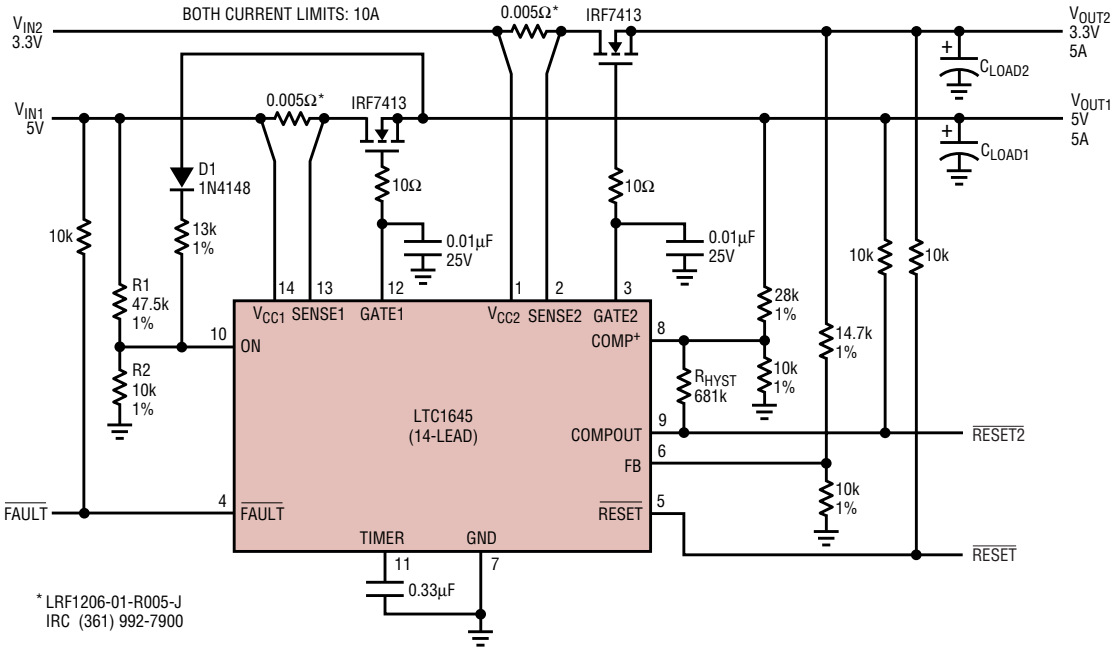

Figure 6. Ramping up 5V followed by 3.3V

Thus, both input supplies must be within regulation before a timing cycle can start. At the end of the timing cycle, the output voltages ramp up together. If either input supply falls out of regulation or if an overcurrent condition is detected, the gates of Q1 and Q2 are pulled low together.

Figure 5 shows an oscilloscope photo of of Figure 4's circuit in action. On power-up, V_{OUT1} and V_{OUT2} ramp up together. On power-down, the LTC1645 turns off Q1 and Q2 simultaneously. Charge remains stored on C_{LOAD1} and C_{LOAD2} and the output voltages will vary depending on the loads. D1 and D2 turn on at ≈1V (≈0.5V each), ensuring that V_{OUT1} never exceeds V_{OUT2} by more than 1.2V, while D3 guarantees that V_{OUT2} is never greater than V_{OUT1} by more than 0.4V. Barring an overvoltage condition at the input(s), the only time these diodes can conduct current is during a power-down event, and then only to discharge C_{LOAD1} or C_{LOAD2}. In the case of an input overvoltage condition that causes excess current to flow, the circuit breaker will trip if the current limit level is set appropriately.

Figure 6 shows the LTC1645 configured to ramp up V_{OUT1} before V_{OUT2}. C_{LOAD1} is initially discharged and D1 is reverse-biased, thus the voltage at the ON pin is determined only by V_{CC1} through the resistor divider R1 and R2. If V_{CC1} is above 4.6V, the voltage at the ON pin exceeds 0.8V and V_{OUT1} ramps up one timing cycle later. As V_{OUT1} ramps up, D1 forward-biases and pulls the ON pin above 2V when V_{OUT1} ≈ 4.5V. This turns on GATE2 and V_{OUT2} ramps up. The FB comparator monitors V_{OUT2}, and the spare comparator monitors V_{OUT1} with R_{HYST} creating ~50mV of hysteresis. To ensure that V_{OUT1} does not fall much below V_{OUT2} as the load capacitors discharge during power down, a Schottky diode can be connected from V_{OUT2} to V_{OUT1}.

Conclusion

Designing a traditional hot-insertion system requires a significant effort by an experienced analog designer. An easy way to reduce the design effort is to use the LTC1645, which offers charge-pump gate drivers, a user programmable delay, voltage level monitors and other specialized features. With the LTC1645, it is easy to create reliable Hot Swap systems.