Micropower Octal 10-Bit DAC Conserves Board Space with SO-8 Footprint

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Introduction

Historically, many circuits have relied on potentiometers for adjustment or control. Increasingly, microcontrollers and microprocessors are finding applications in these circuits. The inclusion of processors can eliminate potentiometers, replacing them with digital-to-analog converters (DACs). Fulfilling this need is the LTC1660.

Features

Eight DACs in 0.045in^2

The LTC1660 is the latest multichannel DAC from Linear Technology. This 10-bit, voltage-output, octal DAC is designed to conserve board space. Packaged in a 16-pin narrow SSOP, it has an 8-pin SO footprint. Figure 1 is a block diagram showing the LTC1660's major circuit features.

Inherent 10-Bit Monotonicity and Linearity (DNL) Performance

The LTC1660 uses a DAC architecture that features excellent ±0.5dB differential linearity accuracy, ensuring inherently monotonic performance. This is important for closed-loop control applications, since nonmonotonic operation compromises loop stability. Figures 2a and 2b show the LTC1660's INL and DNL performance, respectively.

Reference Input

The LTC1660 uses a single external reference voltage for all its internal DACs. This voltage sets its full-scale output range. The reference voltage magnitude has a range of 0V to V_{CC}. Figure 3 shows a micropower LT1460-2.5 voltage reference setting the LTC1660's full-scale output to 2.5V.

Rail-to-Rail Output Amplifiers

Each internal DAC has an amplifier that buffers its output. The amplifiers' output voltage can swing rail-to-rail; they can source or sink up to 5mA while maintaining guaranteed linearity and monotonicity performance. Additionally, the amplifiers can easily drive 1000pF and remain stable. Higher capacitive loads (such as 0.1µF) can be driven by placing a small value resistor (100Ω typical) in series with the output pin.

Single Supply, 60µA per DAC

The LTC1660 maintains its specified operation over the wide supply range of 2.7V to 5.5V. To ensure efficient operation on this supply range, the total typical supply current drawn is just 480µA. The wide supply range and low current requirements make this DAC ideal for battery-powered applications.

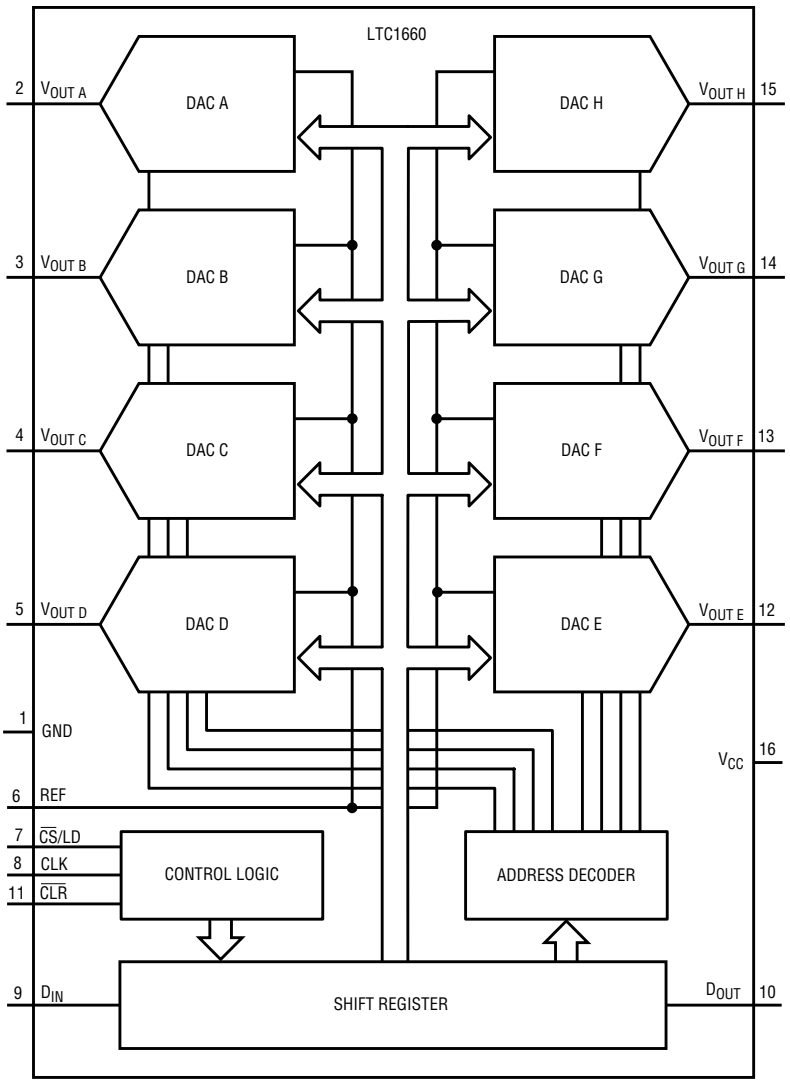

Figure 1. LTC1660 block diagram

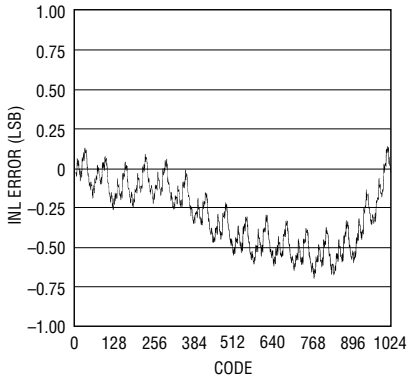

Figure 2a. LTC1660 integral nonlinearity error

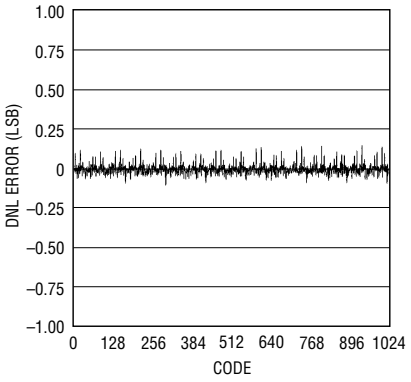

Figure 2b. LTC1660 differential nonlinearity error

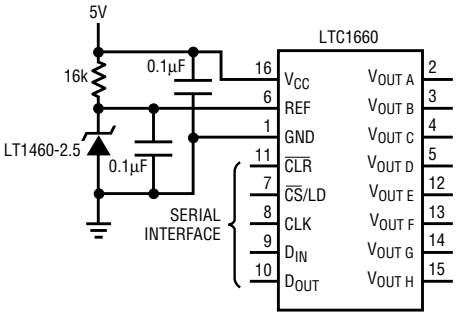

Figure 3. An LT1460 2.5V reference sets the LTC1660's full-scale output to 2.5V.

SLEEP Mode

Further power saving is possible when the LTC1660 is placed in SLEEP mode. Activating SLEEP mode shuts off all internal bias currents and places the output amplifiers in a high impedance state. The SLEEP mode reduces current consumption to 1µA or less. The digital circuitry remains active, retaining the stored values for each DAC. There are two ways to take the part out of SLEEP mode: loading any ADDRESS/CONTROL value other than SLEEP mode or applying a logic low to the $\overline{CLR}$ pin. The last technique awakens the LTC1660 and sets all eight outputs to 0V.

Serial Interface

The eight internal DACs are addressed individually over a 3-wire, SPI-compatible interface. The three signals are Chip Select/Load ($\overline{CS}$/LD), Serial Clock (CLK) and Data In (D_{IN}).

Schmitt Trigger Inputs

The LTC1660's Schmitt trigger digital inputs prevent false triggers when responding to noisy signals or those having slow rise or fall times. This quality makes the LTC1660 ideal for remote placement at the end of long serial transmission lines or lines that use optoisolators.

D_{OUT} Daisy Chain

Another feature of the LTC1660's serial interface is its D_{OUT} pin. The current contents of the internal shift register are shifted out on this pin as new data is shifted in on the D_{IN} pin. This pin makes it possible to connect multiple LTC1660s and other LTC DACs to the same serial data line. The daisy chain is linked by connecting a part's D_{OUT} pin to the D_{IN} pin of the next part in the chain. The advantages of the single serial data line include reduced circuit board space, reduced radiation that results from fewer circuit traces and conservation of limited microcontroller or microprocessor I/O lines.

Power-On Reset

The LTC1660's power-on reset ensures that the output voltage on each DAC is set to 0V when power (2.7V–5.5V) is first applied to the V_{CC} pin.

Asynchronous CLEAR

This active low input will asynchronously reset all eight DAC outputs to 0V when a logic low is applied to this pin. It also deactivates the SLEEP mode.

Applications

The LTC1660 shines brightly in applications that take advantage of its micropower, linearity and versatility. The applications include offset and gain adjust in industrial control systems and AGC and transmit power adjustment in wireless communication.

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Table 1. DAC address/control functions

Address/Control				Action
Bit_{14}	Bit_{13}	Bit_{12}	Bit_{11}	
0	0	0	0	No Update
0	0	0	1	Load DAC A
0	0	1	0	Load DAC B
0	0	1	1	Load DAC C
0	1	0	0	Load DAC D
0	1	0	1	Load DAC E
0	1	1	0	Load DAC F
0	1	1	1	Load DAC G
1	0	0	0	Load DAC H
1	0	0	1	None
1	0	1	0	None
1	0	1	1	None
1	1	0	0	None
1	1	0	1	None
1	1	1	0	SLEEP Mode
1	1	1	1	Load all DACSs with the same 10-bit code

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Accessing the Functionality

Table 1 shows the DAC ADDRESS/CONTROL codes that update each of the DACs, activate the SLEEP mode, cause "No Update", or update all DACs with the same 10-bit value.

The four MSBs (Bit_{15}–Bit_{12}) of the 16-bit data word sent to the LTC1660 select a DAC for updating or a control function such as SLEEP. The next ten bits (Bit_{11}–Bit_2) are the data that sets the selected DAC's output voltage. For example, with a 2.5V reference voltage applied to the LTC1660's pin 6, a value of 819 (1100110011) on Bit_{11}–Bit_2 sets the DAC's output voltage to 819/1024 • 2.5V, = 2.0V. The last two bits (Bit_1–Bit_0) are "don't care." When a 4-bit "no update" code is sent (Bit_{15}–Bit_{12} = 0000 and 1001–1101), the contents of Bit_{11}–Bit_0 are ignored. The SLEEP mode is selected by sending Bit_{15}–Bit_{12} = 1110. The LTC1660 is awakened by applying a logic low to the $\overline{CLR}$ pin or by completing a data load cycle. To awaken the part with a load cycle and return to the same output voltages as before SLEEP, use address/control locations Bit_{15}–Bit_{12} = 0000 or 1001–1101. Using $\overline{CLR}$ to awaken the LTC1660 changes the contents of all DAC registers to zeros and the output voltage to 0V. Finally, all DACs can be forced to the same output voltage by using address/control location Bit_{15}–Bit_{12} = 1111.

Layout, Bypassing and Grounding Considerations

Like all data converters, the LTC1660 performs best when it is properly grounded, bypassed and placed on a PCB layout optimized for low noise. Proper grounding is achieved by placing the part over an analog ground plane. Ideally, no traces should cut through the analog ground plane. If a digital ground plane is present, it should make contact with the analog ground plane at only one point, usually where the board is grounded to the power supply ground. If the board consists of multiple layers, the digital and analog ground planes should not overlap each other. The ground pin (pin 1) should be connected to the analog ground plane.

Two 0.1µF bypass capacitors should be connected between the LTC1660 and the analog ground plane. One capacitor is connected to the V_{CC} input (pin 16) and the other is connected to the reference input (pin 6). Lead lengths should be as short as possible.

To help ensure that digital switching noise does not contaminate the analog output, pins 7–11 should be placed over the digital ground plane and not cross the analog ground plane.

Conclusion

The LTC1660 10-bit octal DAC features a very small narrow SSOP-16 package, micropower operation and power saving SLEEP mode. These features make this the ideal part for dense circuit boards and battery-powered applications.