I²C Dual Fan Speed Controller Increases Efficiency and Reduces Noise

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Busy servers and rack-based network and telecom equipment rely on hard-working cooling systems to keep from melting down. The simplest cooling system is a bank of fans running at full tilt, all of the time. This approach ensures a cool environment, but overcompensation is neither efficient, nor is it good for the fans. High output fans that work full time do not last very long (their bearings wear out), are not very efficient (they use power also), and are noisy (especially when their bearings wear out). The LTC1840 dual fan speed controller reduces the wear on bearings, and noise, by continuously adjusting fan speed to match the instantaneous cooling requirements of the system.

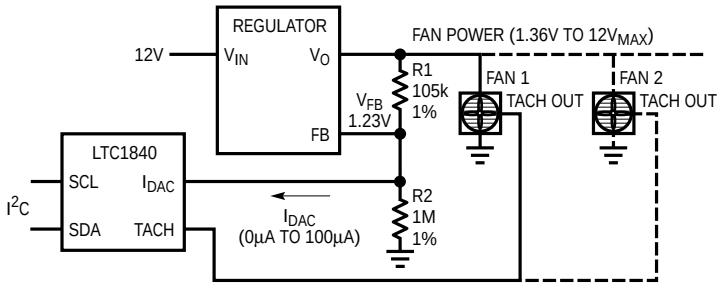

Figure 1. LTC1840 fan speed control block diagram

The LTC1840 monitors and controls multiple fans via an I²C and SMBus compatible 2-wire serial interface. It provides two fan speed control channels, features fan tachometer and fault monitoring, nine slave addresses and four general-purpose programmable I/O pins, all in a convenient 16-pin SSOP package.

Figure 1 shows a block diagram for a fan speed control system using the LTC1840. The LTC1840 contains two current output DACs that control fan speed. The scaled currents individu-

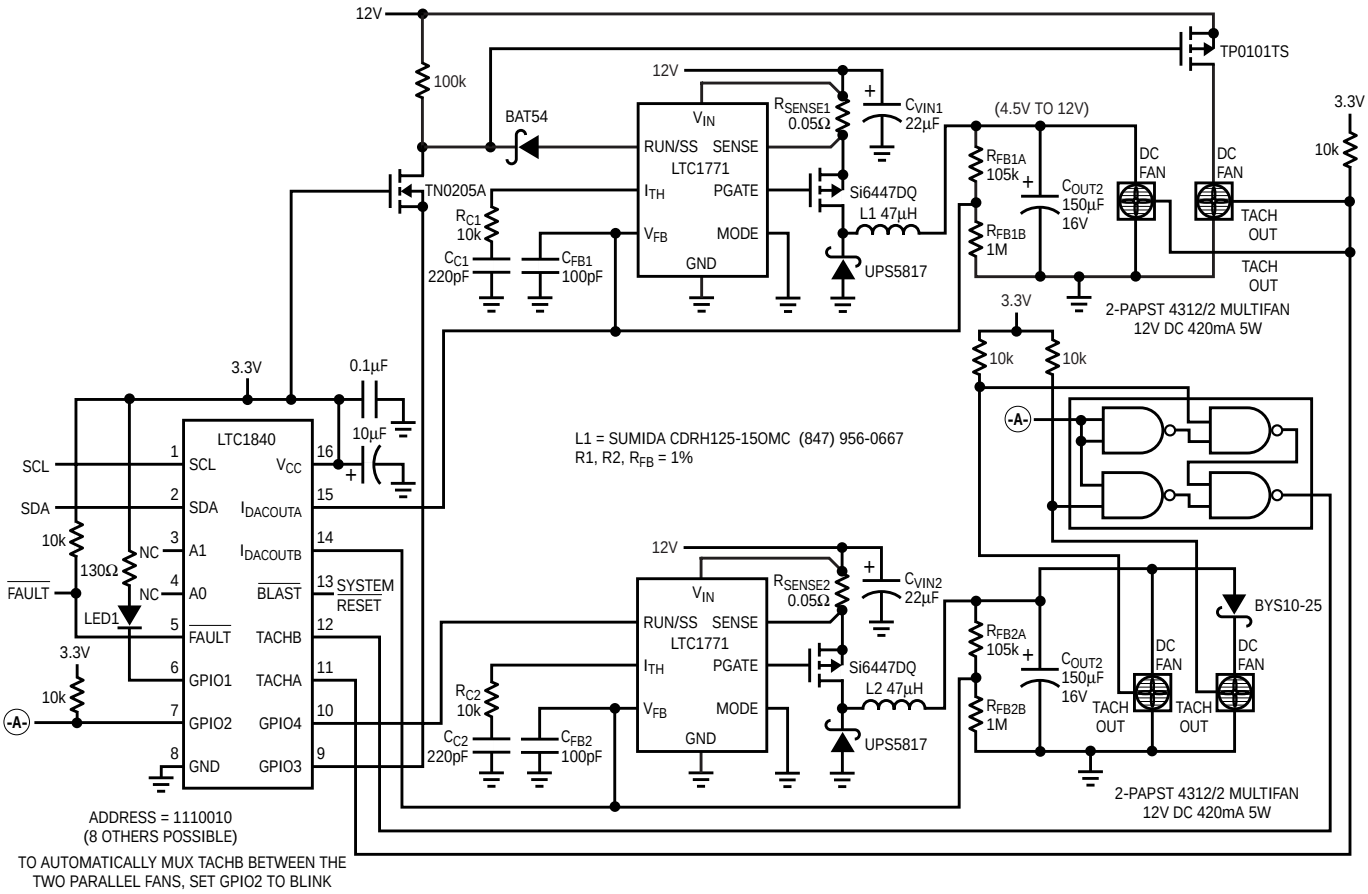

Figure 2. Controlling four fans with the LTC1840

ally adjust the fan-driving output voltage of a switching regulator. V_O increases as the current I_{DAC} is increased under command of the serial interface. The number of fans controlled by one DAC is limited only by the switching regulator output power.

The TACH pin of the LTC1840 monitors the speed of fans that include a tachometer output. Internal logic accumulates a maximum of 255 counts between the fan tachometer's rising edges. The rate of the counter is determined by a divisor (2, 4, 8 or 16 chosen via the serial interface) from the 50kHz internal oscillator. Fans slowing down due to worn bearings or halted from a jam will cause an overflow in the internal counter and a corresponding bit is set low in the fault register. The system controller can then take action, shutting down the faulty fan and summoning maintenance.

The chip contains four general-purpose input/output (GPIO) pins, which are configured independently. As open-drain outputs, they can be set high, low or to pulse at a 1.5Hz rate. The outputs are rated at 10mA sink current so they can drive LEDs. When the GPIO pins are configured as inputs, they can monitor thermal switches, push buttons and the fault or power good outputs of switching regulators and Hot Swap™ controllers. A fault register detects and flags state changes.

Internal data registers are read and programmed via I^2C by specifying device address and register address. DACA and DACB registers control the 100µA current outputs on a 255-step scale. The STATUS register allows the user to enable the TACHA and TACHB fault data and set the divisor for the internal counter frequency. The internal count, which is inversely proportional to tachometer speed, is stored in the TACHA and TACHB registers. Unmasked faults set the FAULT pin high as an instant hardware alert. The GPIO setup and GPIO data registers configure the GPIO pins, assign output and fault status, and read input state.

Continuous System Cooling and Tachometer Monitoring

The circuit in Figure 2 demonstrates the capabilities of the LTC1840. Each of the two LTC1771 high efficiency step-down regulators can supply power for up to four 12V, 420mA fans. As shown, the upper LTC1771 drives a single fan backed up by an idle, redundant fan. In the event the primary fan fails, GPIO3 turns off the LTC1771 and simultaneously activates the backup fan at full speed. These two fans operate one at a time so their tachometer outputs are wired OR, and only one input (TACHA) is required to monitor their speed.

The other two fans are driven in parallel by the second LTC1771 and alternately monitored by TACHB. These fans operate concurrently, so their tachometer outputs are muxed by a quad NAND gate. GPIO2 operates in pulsing mode and serves to clock the mux.

Additional Features

For applications requiring multiple fan controllers, the LTC1840's three-state (high, low, no connect) address programming inputs support nine user-selectable slave addresses. The $\overline{\text{FAULT}}$ output bypasses the serial interface and brings immediate attention to fault conditions detected by the LTC1840, including slowdowns in the tachometer and changes in GPIO logic state.

If the $\overline{\text{BLAST}}$ pin is high at startup or presented with a high to low transition at anytime, the DAC output currents are immediately forced to full scale and the chip awaits commands from the serial bus. In addition, when $\overline{\text{BLAST}}$ is set high the LTC1840 guards against system controller crashes with an internal watchdog timer. If the device is not accessed for a period of more than 1.5 minutes, both DAC outputs go to full scale to guarantee adequate cooling.