Phase-Shift Full-Bridge Controller Enables Efficient, Isolated Power Conversion for High Power Applications

Introduction

The distributed power supply systems of large data processing and communications equipment use isolated, high power converters to generate intermediate bus distribution voltages and lower voltages for CPU, mass storage and I/O circuitry. Power supply isolation is necessary for regulatory agency requirements, shielding of sensitive circuitry and ground loop elimination. Unfortunately, adding isolation increases complexity and reduces efficiency due to a variety of factors, including magnetic core and copper loss of the power transformer. These problems increase as the power level and input voltage increase. In addition, parasitic leakage inductance can generate high voltage transients across the power MOSFETs reducing efficiency even further and generating undesirable EMI. Any efficiency improvement to these power supplies results in

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reduced cooling requirements, shrinking volume, weight and cost. Phase-shifted full-bridge power converters have gained attention because of their ability to harness the usually undesirable elements of the power transformer and MOSFETs to significantly reduce switching losses and noise.

The 20-pin G or N packaged LTC1922-1 (Figure 1) is a full featured controller for the phase-shifted



Figure 1. LTC1922 block diagram

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What is a Phase-Shifted Full Bridge?

Rather than hard switching the power MOSFETs like a conventional full bridge or forward converter, the phaseshifted full-bridge converter clamps and recycles the energy stored in the power transformer's leakage induc-



Figure 3. LTC1922 timing diagram

Figure 2. Instantaneous switching loss from capacitive discharge

tance to softly turn on each of the four power MOSFETs in the full bridge. ZVS (zero voltage switching) occurs when the external power MOSFETs are turned on and off when their respective drain to source voltages are at or near zero volts, effectively eliminating the instantaneous turn on-power loss of the MOSFETs caused by C_{OSS} (drain-to-source capacitance) and parasitic capacitance discharge (see Figure 2). This improves efficiency, reduces switching related EMI and eliminates the need for primaryside snubbers.

Phase-Shift Control

Referring to Figure 3, alternate diagonal switches in the full bridge (A-D or B-C) conduct simultaneously in order to deliver energy to the load (secondary). Each switch-drive signal has a 50% duty cycle less a small ZVS turnon delay. Outputs A and B are 180 degrees out of phase and change state every time the oscillator clocks the internal PWM flip flop. Similarly, outputs C and D are 180 degrees out of phase and change state every time RAMP exceeds the PWM control level defined by COMP. As the PWM control level is increased, a corresponding increase of switch conduction overlap (A–D or B–C) or phase shift occurs. The maximum overlap per switch pair is 50%. Since both pairs of switches conduct during a transformer cycle, the maximum attainable duty cycle is 100%. Once a switch turns off, the inherent momentum of the transformer's magnetizing and leakage inductances under phase-shift control help to commutate the respective bridge leg voltages toward a zero voltage condition.

Adaptive DirectSenseTM Technology

The LTC1922-1 implements ZVS with closed loop DirectSense technology. Optimal ZVS delay time is a complex nonlinear function of load current, MOSFET C_{OSS} , transformer interwinding capacitance, leakage and magnetizing inductance and output inductance. In addition, each bridge leg exhibits unique behavior necessitating different delays. An optimal delay time prevents hard switching and/or increased body diode conduction, maximizes the duty cycle range and minimizes EMI. Referring to



Figure 4. Direct sensing of full bridge

Figure 4, the LTC1922 senses each leg of the full bridge with a voltage divider on PDLY and ADLY and senses the input supply with a voltage divider on SBUS. Internal high speed latching comparators, state and PWM logic and fail-safe circuits command the respective high-side MOSFETs (MA, MC) to turn on when the rising voltages on PDLY and ADLY cross the threshold level determined by the voltage on SBUS. In addition, every rising edge on ADLY and PDLY initiates an accurate current out of ADLY and PDLY, respectively. This current, along with the external resistor divider, produces a lower threshold level for use when the bridge legs commutate towards ground, providing ZVS to the lower MOSFETs (MB, MD). After the falling edge transition occurs, the current is reset. By sensing the bridge and input supply directly, the LTC1922-1 can intelligently adapt to any change in load current, temperature, component tolerances, driver circuitry delay offset

or input voltage. The benefits include simple design, high efficiency, increased duty cycle capability, lower EMI and consistent performance without tweaking.

Synchronous Rectification

Synchronous rectification can provide significant efficiency improvements, especially at lower output voltages and when the synchronous switch timing is optimal. The LTC1922-1 includes the internal timing and logic required to produce drive signals for secondary-side synchronous rectifiers, as shown in Figure 3. These switching intervals have been internally programmed to prevent premature turn on and delayed turn off of the external synchronous rectifiers, maximizing the benefit over silicon or Schottky rectifiers and eliminating external glue logic and discrete timing circuitry.

The synchronous rectifier MOS-FETs and transformer secondary



Figure 5. Output inductor ripple vs duty cycle

power stage are configured as an interleaved current doubler. The current doubler employs two inductors that share the output current equally and, more importantly, are driven 180 degrees out of phase. These properties reduce output capacitor ripple current significantly depending on duty ratio (see Figure 5), reducing voltage ripple and improving output capacitor reliability while producing twice the output current per inductor volume of comparable single inductor power stages.

48V to 3.3V/40A Isolated Converter

The circuit of Figure 6 features the LTC1922-1, regulating 3.3V at up to 40A from an isolated 36V to 72V input voltage. Only surface mount components are used in this design. Peak efficiency is just over 90%, drop-



"B" LEG 50V/DIV PRIMARY CURRENT 5A/DIV 0A INDUCTOR CURRENTS 5A/DIV



Figure 7. 48V to 3.3V conversion efficiency

Figure 8. 48V input to 3.3V/20A output waveforms

1us/DIV

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Figure 6. LTC1922 all-surface mount 3.3V/40A converter

ping to 85% at a 40 amp load (Figure 7). The high efficiency eliminates the need for forced air cooling, faceplates or bulky heat sinks. A single LTC1693-1 and tiny signal transformers are used to provide gate drive to the two high-side bridge MOSFETs. A second LTC1693-1 provides the drive to the secondary synchronous rectifiers. The LT1431 and a standard optical coupler provide voltage regulation information across the isolation boundary. Primary side scope waveforms (Figure 8) exhibit the very clean transitions typical with the phase-shifted full bridge. Since the LTC1922-1 is a current mode controller, it is easily adaptable to standard load-sharing techniques used in redundant power system applications. Additional features of this converter include undervoltage lockout, soft start, leading edge blanking, current limit and short-circuit protection.

Conclusion

The phase-shifted full-bridge converter is an ideal candidate for high power isolated power conversion, as evidenced by its high efficiency and low noise performance. The LTC 1922-1 is a next generation control solution for this type of converter offering optimal zero voltage switching and integrated synchronous rectification control among several other features tailored to high power applications.