1.4GHz Low Jitter PLL with Clock Distribution Solves Difficult Clocking Problems: Multi-Clock Synchronization and Data Converter Clocking
Chris Pearson

Two of the more difficult challenges facing clock system designers are synchronizing multiple system clocks and creating low jitter data converter clocks. The LTC6950 overcomes these challenges by featuring Linear Technology's easy-to-use EZSync™ technology and providing five clock outputs with less than 100fs RMS additive jitter.

Other multi-clock synchronization solutions involve aligning the edges of two or more high speed input signals within an extremely precise time window, sometimes within a couple nanoseconds. Such devices, hinting at the unreliability of this synchronization method, often include a SYNCRESULT pin to indicate whether the synchronization passed or failed, requiring a retry. The elegance of EZSync is it eliminates the need for precision alignment of any high speed input signals, while assuring consistent edge alignment of all outputs on one or multiple EZSync clock devices. With EZSync, synchronizing multiple devices, multiple boards and even multiple system level clock edges is as easy as pressing a button.

The LTC6950 produces five low jitter, high slew rate differential clocks. These clock characteristics allow designers to clock multiple high speed data converters directly, without the typical additional expense of onboard clock filtering and clock shaping components. The LTC6950 simplifies overall system design and cost compared to traditional data converter clock architectures.

The first part of this article summarizes the LTC6950's features and how it works. The second part covers the LTC6950's EZSync functionality. The third part describes the benefits of clocking ADCs

and DACs directly with the LTC6950. Finally, a complete LTC6950 design example shows exactly how easy it is to design a typical LTC6950 application using Linear's ClockWizard™ tool.

LTC6950 OVERVIEW

The block diagram in Figure 1 shows how the LTC6950 is divided into three main circuit blocks: the phase-locked loop (PLL) section, the clock distribution section and the digital control section.

The PLL section works in conjunction with the external reference and external VCO to generate a desired VCO frequency (f_{VCO}) as follows:

$$f_{VCO} = f_{REF} \cdot N/R \qquad (1)$$

where f_{REF} is the reference input frequency, R is the reference input divide value and N is the VCO feedback divide value. f_{VCO} is fed into the clock distribution section.

The clock distribution section receives a signal at f_{VCO} and distributes this signal

Figure 1. LTC6950 block diagram
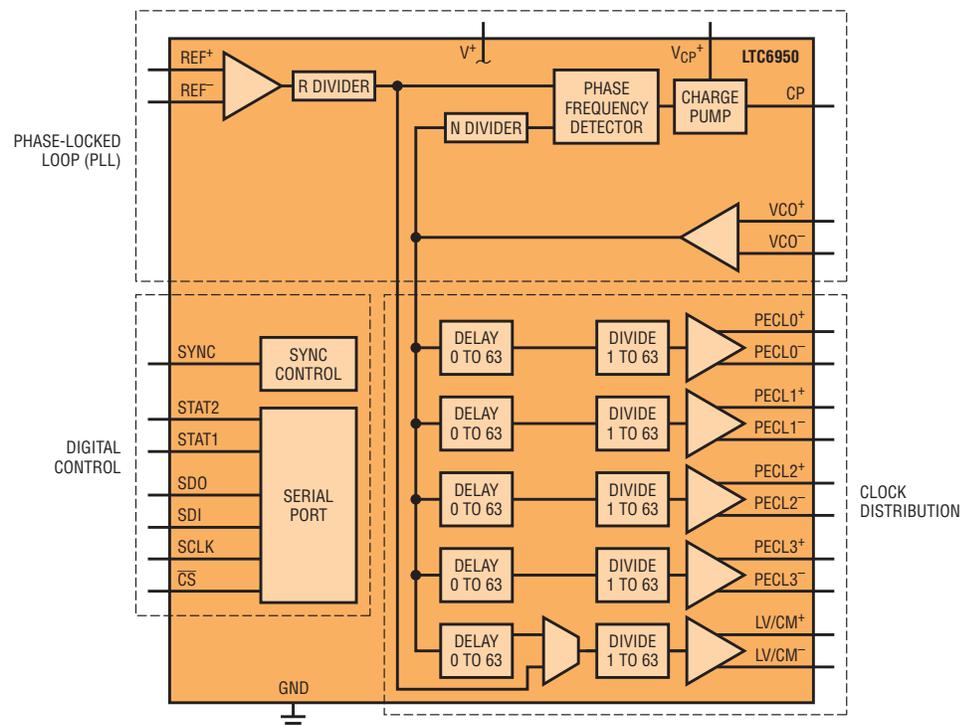
The LTC6950 is the first device to offer Linear Technology's EZSync technology, which simplifies aligning multiple clocks across multiple parts, boards and systems. LTC6950 performance levels enable direct clocking of high performance data converters, simplifying system design and reducing system cost.

to five separate channels. Each of the five channels has the independent ability to delay the first synchronized clock edge by 0 to 63 VCO clock cycles and to divide f_{VCO} by any integer from 1 to 63.

The output signals from the dividers are sent to a buffer that determines the output signal type. Four channels produce an extremely low noise differential LVPECL clock signal capable of output frequencies up to 1.4GHz. The fifth channel creates a configurable differential LVDS output or a pair of CMOS outputs. The LVDS output can produce clock

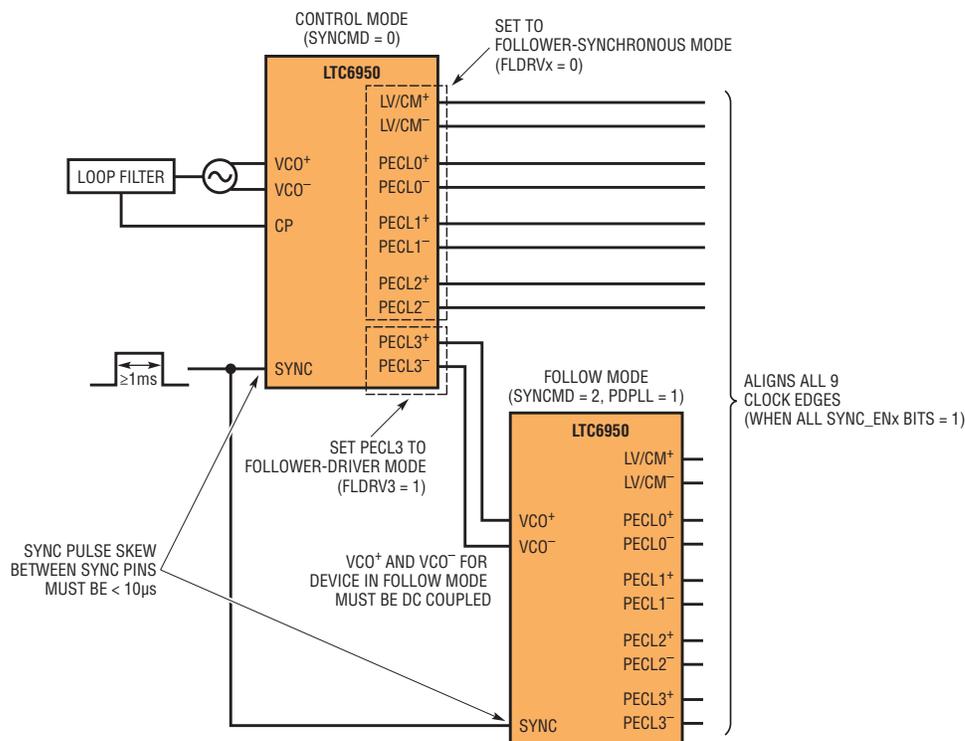Figure 2. EZSync STANDALONE mode
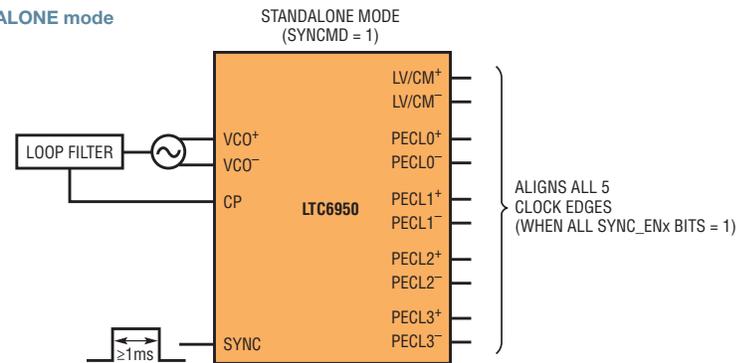
frequencies up to 800MHz, while the CMOS output is limited to 250MHz.

The third and final section is the digital control section. The box labeled

SYNC CONTROL in Figure 1 is the EZSync control circuitry—functionality described in detail below. The digital control section includes a standard 4-wire serial interface and two pins to monitor the status of certain register bits.

EZSync GUARANTEES MULTI-CLOCK SYNCHRONIZATION

As mentioned, synchronizing multiple high speed clocking devices is traditionally difficult due to tight timing constraints and unreliable architectures. In contrast, EZSync guarantees clock synchronization and has relaxed the timing constraints. EZSync functionality is best described visually, as shown in Figures 2, 3 and 4. EZSync has three modes: STANDALONE (Figure 2), CONTROL (Figures 3 and 4), and FOLLOW (Figures 3 and 4).

STANDALONE mode synchronizes the five LTC6950 clock outputs after a 1ms high pulse is applied to the LTC6950 SYNC pin, as shown in Figure 2. Once the SYNC pin goes high, all Sync Enabled clock outputs are held at a logic low once they transition to that state. After the SYNC pin is returned low, all Sync Enabled clock outputs

Figure 3. EZSync FOLLOW mode and CONTROL mode using follower-driver and follower-synchronous outputs

Linear Technology's ClockWizard tool includes a Scope Plot simulation tool that allows the user to quickly predict the output delay response in the STANDALONE, FOLLOW or CONTROL modes.

resume clocking synchronously. The designer can also chose to disable synchronization on a per output basis by setting the output's SYNC_ENx register bit to a logic low. These outputs will not be disturbed during a synchronization operation.

CONTROL and FOLLOW modes are used in tandem when a LTC6950 clock output is connected to the VCO input of another EZSync device, as illustrated in Figures 3 and 4. Figures 3 and 4 introduce some new terminology: CONTROLLER, FOLLOWER, follower-driver and follower-synchronous, defined below:

- **CONTROLLER:** EZSync device set to CONTROL mode. A device in CONTROL mode controls the timing for all other EZSync devices.

- **FOLLOWER:** EZSync device set to FOLLOW mode. The clock input of a FOLLOWER has a DC coupled connection from a clock output of the CONTROLLER.

- **Follower-Driver:** CONTROLLER's clock output that is connected to a FOLLOWER's clock input. DC coupling is required between the CONTROLLER output and FOLLOWER input.

- **Follower-Synchronous:** CONTROLLER's clock output that is synchronized to its FOLLOWER devices' clock outputs.

In Figure 3, the EZSync CONTROLLER and FOLLOWER architecture synchronizes the four follower-synchronous outputs of the CONTROLLER and the five FOLLOWER outputs after applying a 1ms high pulse to both LTC6950 SYNC pins.

In Figure 4, the EZSync CONTROLLER and FOLLOWER architecture synchronizes 20 FOLLOWER outputs and one follower-synchronous output after applying a 1ms high pulse to all five LTC6950 SYNC pins.

Compared to the STANDALONE architecture, the CONTROLLER and FOLLOWER architecture has an additional modest timing requirement that the max skew between all SYNC signals is < 10µs. The outputs are held in a logic low state during the time the SYNC pin is set to a logic high value

and for a few additional VCO cycles after the SYNC pin is returned to a logic low. The user can choose to disable synchronization on any output by setting the appropriate SYNC_ENx register bit to a logic low. These outputs will not be disturbed during a synchronization operation.

MAKING EZSync EASIER

While applying a 1ms high pulse to the LTC6950's SYNC pin is easy, it does require some familiarity with the EZSync specification to predict how the outputs will
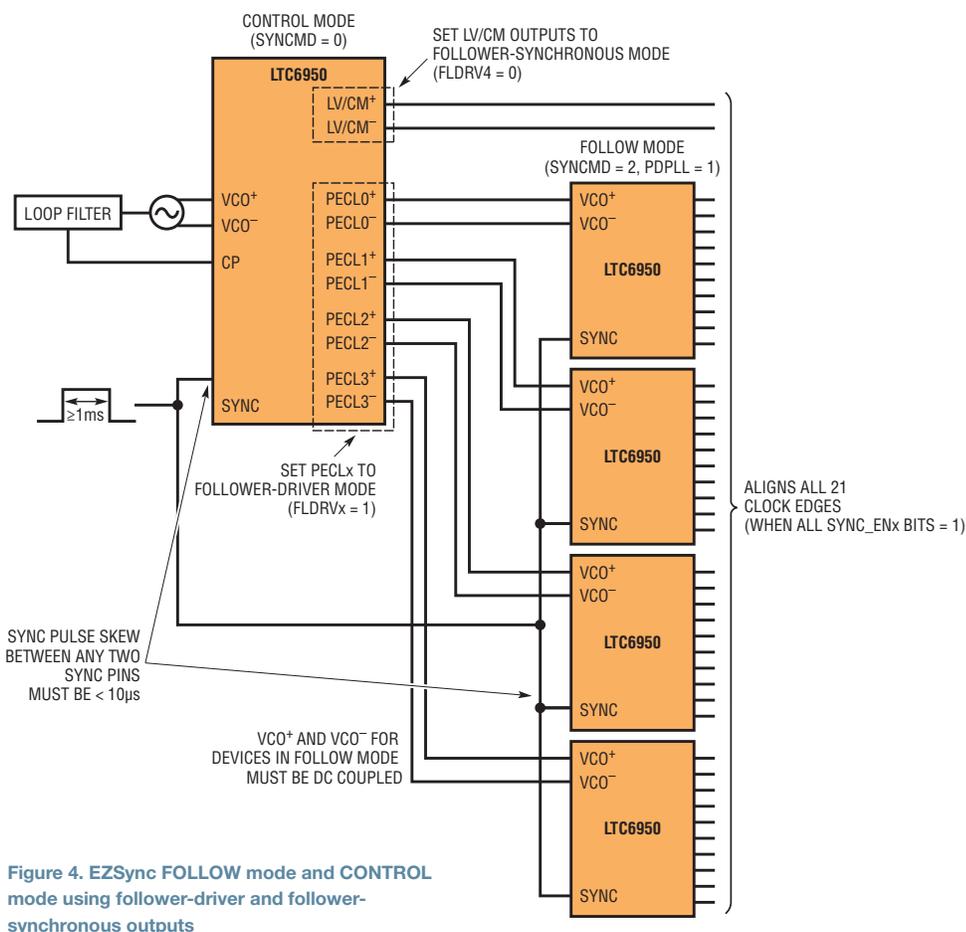

CONTROL MODE (SYNCMD = 0)

SET LV/CM OUTPUTS TO FOLLOWER-SYNCHRONOUS MODE (FLDRV4 = 0)

FOLLOW MODE (SYNCMD = 2, PDPLL = 1)

SET PECLx TO FOLLOWER-DRIVER MODE (FLDRVx = 1)

SYNC PULSE SKEW BETWEEN ANY TWO SYNC PINS MUST BE < 10µs

VCO⁺ AND VCO⁻ FOR DEVICES IN FOLLOW MODE MUST BE DC COUPLED

ALIGNS ALL 21 CLOCK EDGES (WHEN ALL SYNC_ENx BITS = 1)

Figure 4. EZSync FOLLOW mode and CONTROL mode using follower-driver and follower-synchronous outputs

1. Select Loop Design
2. Select Sync
3. Set to STANDALONE
4. Set each output to Synchronized and to 0 Output Delay
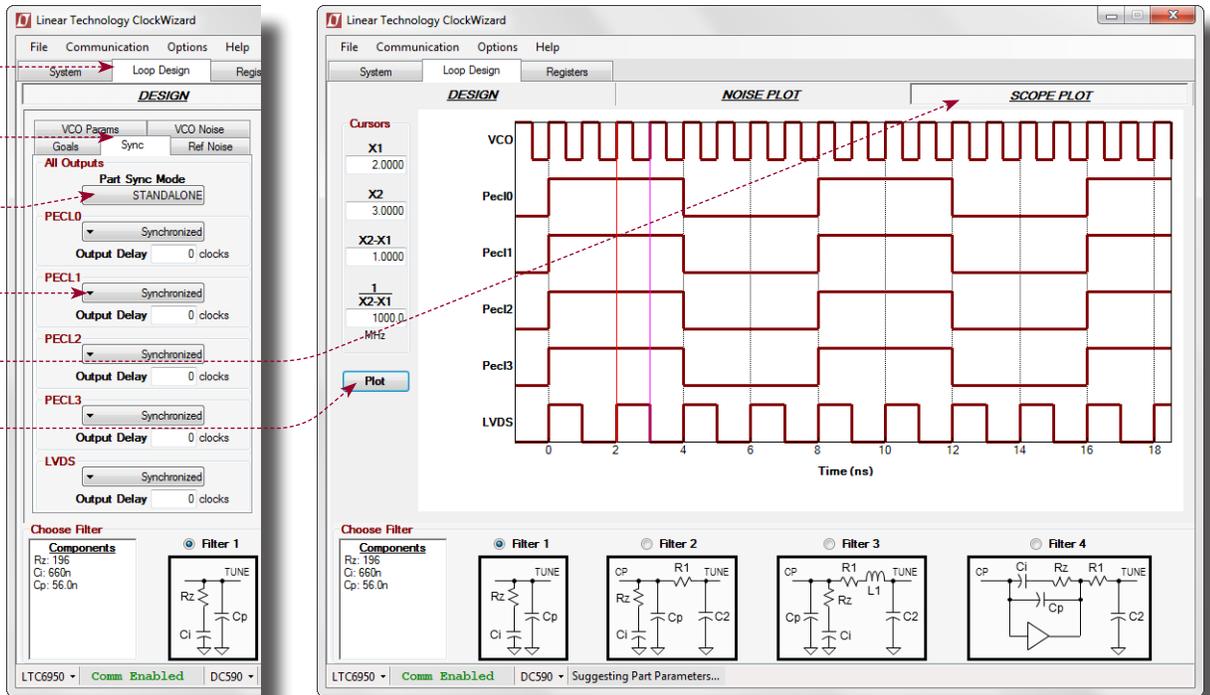5. Select Scope Plot
6. Click Plot

Figure 5. Simulating the LTC6950's output frequencies and output delays in STANDALONE mode using ClockWizard

respond after the LTC6950 SYNC pins are returned to a logic low state. Linear Technology's ClockWizard tool includes a Scope Plot simulation tool that allows the user to quickly predict the output delay response in the STANDALONE, FOLLOW or CONTROL modes. Figures 5 and 6 demonstrate ClockWizard's Scope Plot simulation capability.

DIRECT CLOCKING HIGH SPEED CONVERTERS WITH THE LTC6950

For high performance clocks, high speed ADCs are the de facto benchmark, due to their industry leading clock jitter requirements. There is a tremendous amount of literature that discusses requirements and recommendations for clocking high speed ADCs, but all can be summarized with the following statement: ADCs require a really low phase noise/jitter clock to meet signal to noise ratio (SNR) targets, and it is

recommended that the ADC input clock is a differential clock and has fast clock edges.

Historically, these high speed ADC clocking requirements have been attainable, but only at high cost. This section shows the value of the LTC6950's ability to directly clock high speed ADCs, especially in regards to simplicity and performance.

ADC documents often start out with the following two equations.

$$JITTER_{TOTAL} = $$
$$= \sqrt{\left(JITTER_{CLK\_IN}\right)^2 + \left(JITTER_{APERTURE}\right)^2} \quad (2)$$

$$SNR_{ADC} = 20 \bullet LOG \frac{1}{2\pi f_{IN} \bullet JITTER_{TOTAL}} \quad (3)$$

where f_{IN} = ADC analog input frequency

Equation 2 reminds the user the clock circuitry internal to the ADC also has jitter, known as aperture jitter. Most ADC data sheets provide a typical aperture jitter number for use with Equation 2. Equation 2 then states the

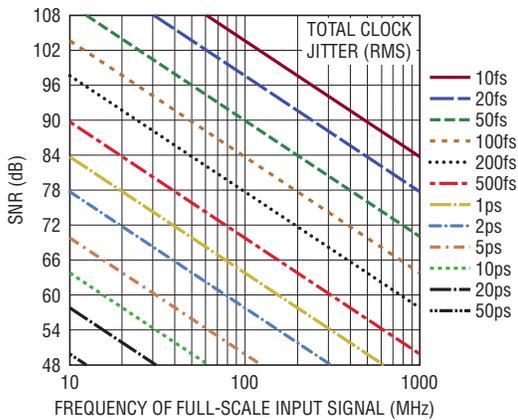Figure 6. ClockWizard's Scope Plot tool shows simulated results of LTC6950 CONTROL mode
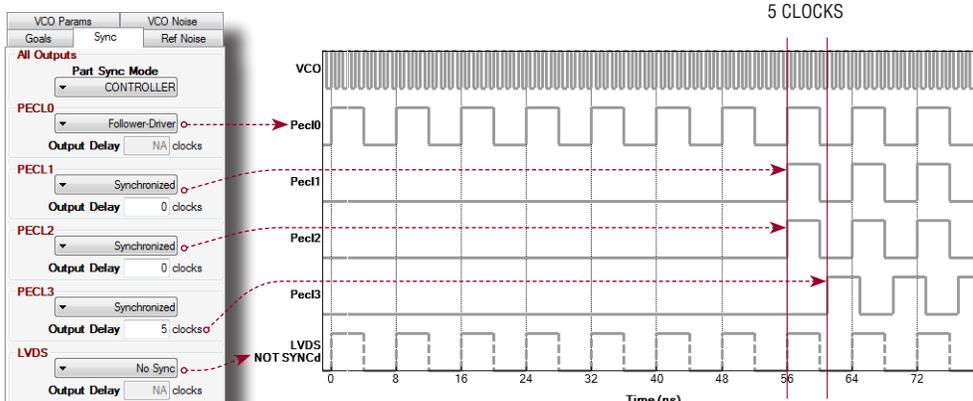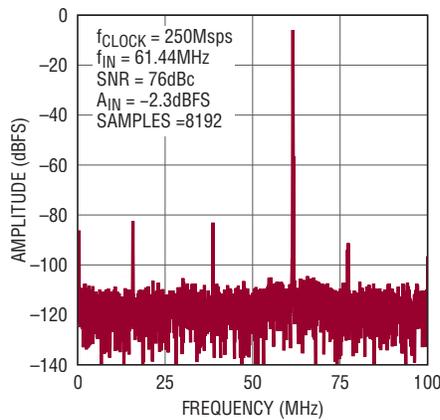
Figure 7. Graphical representation of Equation 3

Figure 8. LTC6950 direct ADC clocking performance

ADC aperture jitter and the clock jitter at the input of the ADC add together in a square root of the sum of squares fashion to produce a total clock jitter.

Equation 3 relates total clock jitter to the ADC SNR performance. This equation is often best visualized by Figure 7. The main point to remember from Equation 3 is as the ADC input frequencies and SNR levels increase, the total clock jitter requirements become more stringent. It is worth clarifying that Equation 3 is dependent on the ADC's analog input frequency, not the clock frequency.

The LTC6950 achieves <100fs RMS jitter. Figure 8 is an SNR plot using the LTC2107 16-bit ADC at a f_{IN} = 61.44MHz (see Figure 8). Traditionally, to achieve this level of SNR performance from the ADC, additional onboard circuitry was needed to condition the clock signal. For example, in Figure 9, a single channel of a traditional ADC clock architecture is compared to a LTC6950 direct ADC clocking architecture. A single LTC6950 has four differential PECL channels that can drive four ADC clocks simultaneously. To drive four ADC clocks, the traditional clock architecture would repeat four times. As a result, the LTC6950 reduces design

complexity, saves board space and lowers the cost of the overall board design.

LTC6950 DESIGN AND SIMULATION EXAMPLE

ClockWizard is a tool that greatly simplifies the clock system design process. In addition to being able to read and write to the LTC6950's SPI registers, the ClockWizard includes a PLL loop filter design tool, a clock output divider/delay configuration tool, a phase noise simulation tool and a clock output timing simulation tool. A typical design for the LTC6950 utilizes the four differential PECL outputs to clock four data converters and the remaining LVDS/CMOS output to clock an FPGA. The following example highlights the ClockWizard design and simulation capabilities when designing a typical application circuit.

Designing the PLL

Download ClockWizard at www.linear.com/ClockWizard and install. The design presented here assumes use of the onboard VCO and reference that arrive installed on the LTC6950's demonstration circuit DC1795A. The values for these onboard components are pre-programmed into the ClockWizard under the VCO Params, VCO Noise and Ref Noise tabs shown in Figure 11. Using ClockWizard, enter the design goals and components required to complete the design, as shown in Figure 11.

> "All things are difficult before they are easy."
> —Thomas Fuller

Figure 9. Advantages of direct ADC clocking with the LTC6950

TRADITIONAL ADC CLOCK ARCHITECTURE

Clock Source
Does not meet ADC phase noise/jitter requirements

Narrow Bandpass Filter
Improves clock phase noise/jitter, outputs lower amplitude sine wave

Transformer
• Single ended to differential conversion
• Step-up transformer for additional amplitude, increases sine wave slew rate

Amplitude Limiting Diodes
Increases in sine wave amplitude can damage ADC

CLOCK SOURCE

Optional Pre-Gain LNA
For additional amplitude, increases sine wave slew rate after filter

CLK+
ADC
CLK−

LTC6950 ADC CLOCK ARCHITECTURE

PECLx+
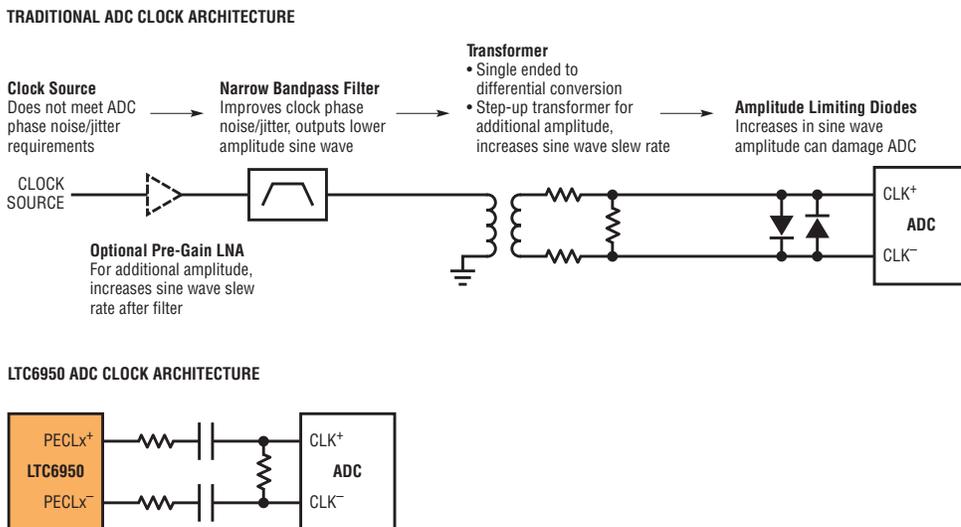**LTC6950**
PECLx−

CLK+
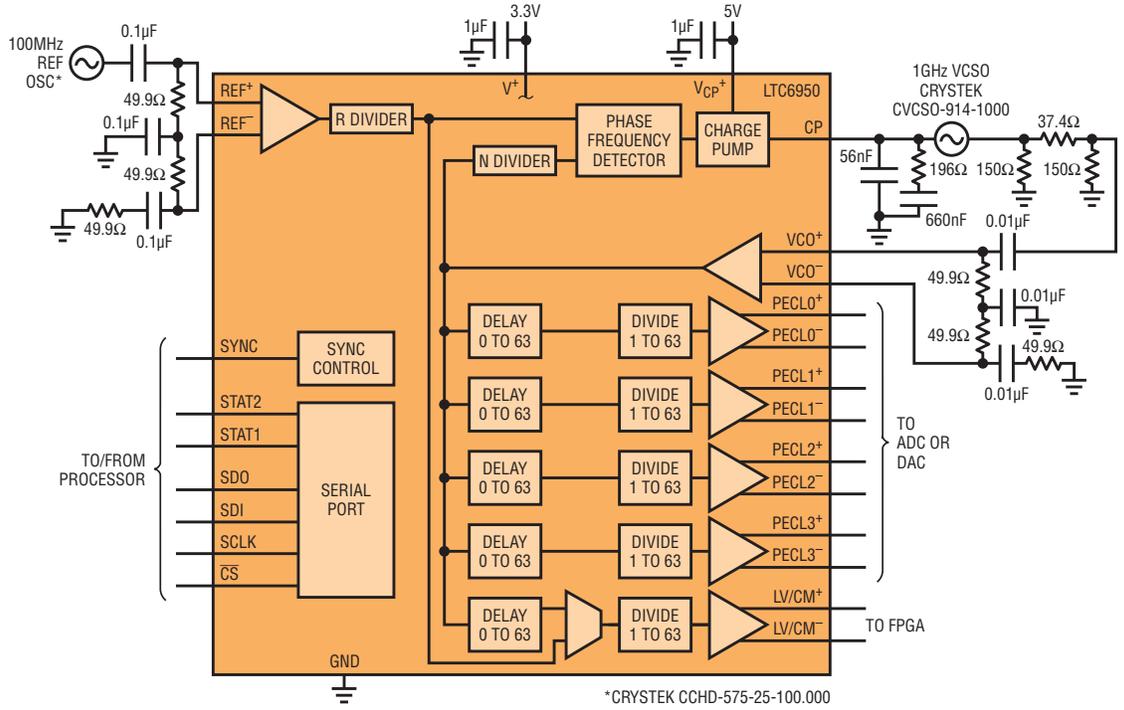**ADC**
CLK−

Figure 10. LTC6950 typical application

Figure 11. ClockWizard LTC6950 loop filter design

1. Select Loop Design

2. Enter reference frequency

3. Enter desired PFD frequency

4. Enter VCO frequency

5. Enter clock frequencies for each of the five clock outputs

6. Click Compute Params

7. Click Design Filter—Filter 1

8. Update component values with the practical component values shown

9. Choose Copy Loop to System from the Options menu. (This updates the System and Register Tab with the correct Serial Interface Values. If a demo board is connected, its serial interface registers are also updated.)
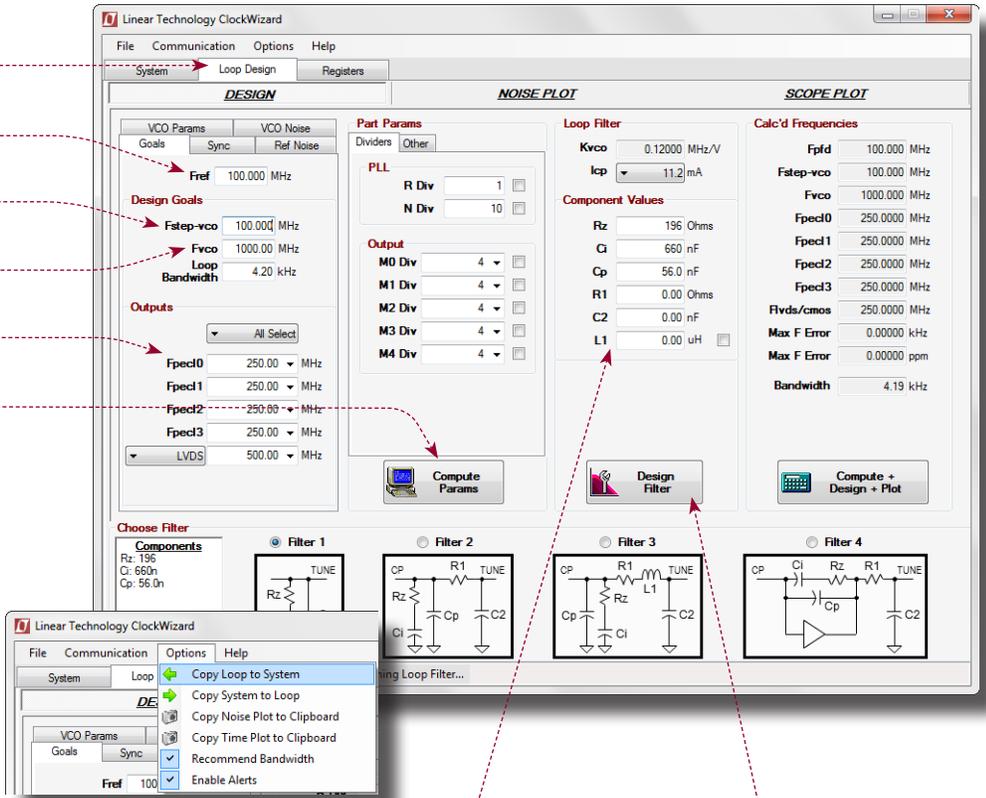
Simulating and Building the PLL

As shown in Figure 11, replace the filter components determined by ClockWizard with the nearest standard component values. In Figure 12, ClockWizard predicts the phase noise of the LTC6950 and the new loop filter for any of the five clock outputs selected in the noise plot. This plot shows how the VCO and reference phase noise affects the total noise, helping the designer choose the VCO and reference components. Once the output phase noise simulation meets the design goals, install the simulated loop filter values onto the DC1795A.

Evaluating the PLL

At this point the LTC6950 can be powered up and evaluated using the DC1795A. Download the DC1795A demonstration circuit manual at linear.com/product/LTC6950#demoboards and follow the power up instructions under the quick start procedure. Verify the output of this example by connecting one of the PECL outputs of the DC1795A to a signal source analyzer, such as Agilent's E5052. Figure 13 shows the measured result, which aligns closely with ClockWizard's simulated results in Figure 12.

CONCLUSION

The LTC6950 is the first device to offer Linear Technology's EZSync technology, which simplifies aligning multiple clocks across multiple parts, boards and systems. The LTC6950 performance levels enable direct clocking of high performance data converters, simplifying system design and reducing overall system cost. To further simplify the design process, ClockWizard was developed to design the loop filter, simulate phase noise and simulate clock output timing and cycle delays. ∎

Figure 12. Simulating the LTC6950 loop filter performance using ClockWizard

1. Select Noise Plot

2. Select desired Plot option

3. Select outputs to plot

4. Click Plot

5. View results

RMS JITTER= 73fs
(INTEGRATE 100Hz to 40MHz)
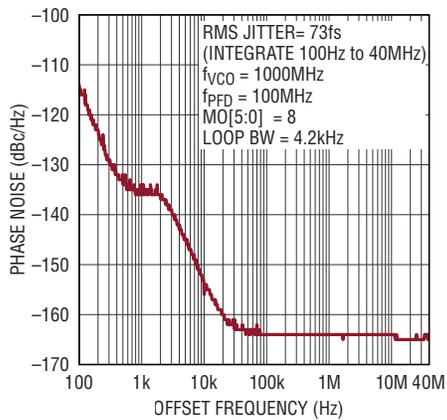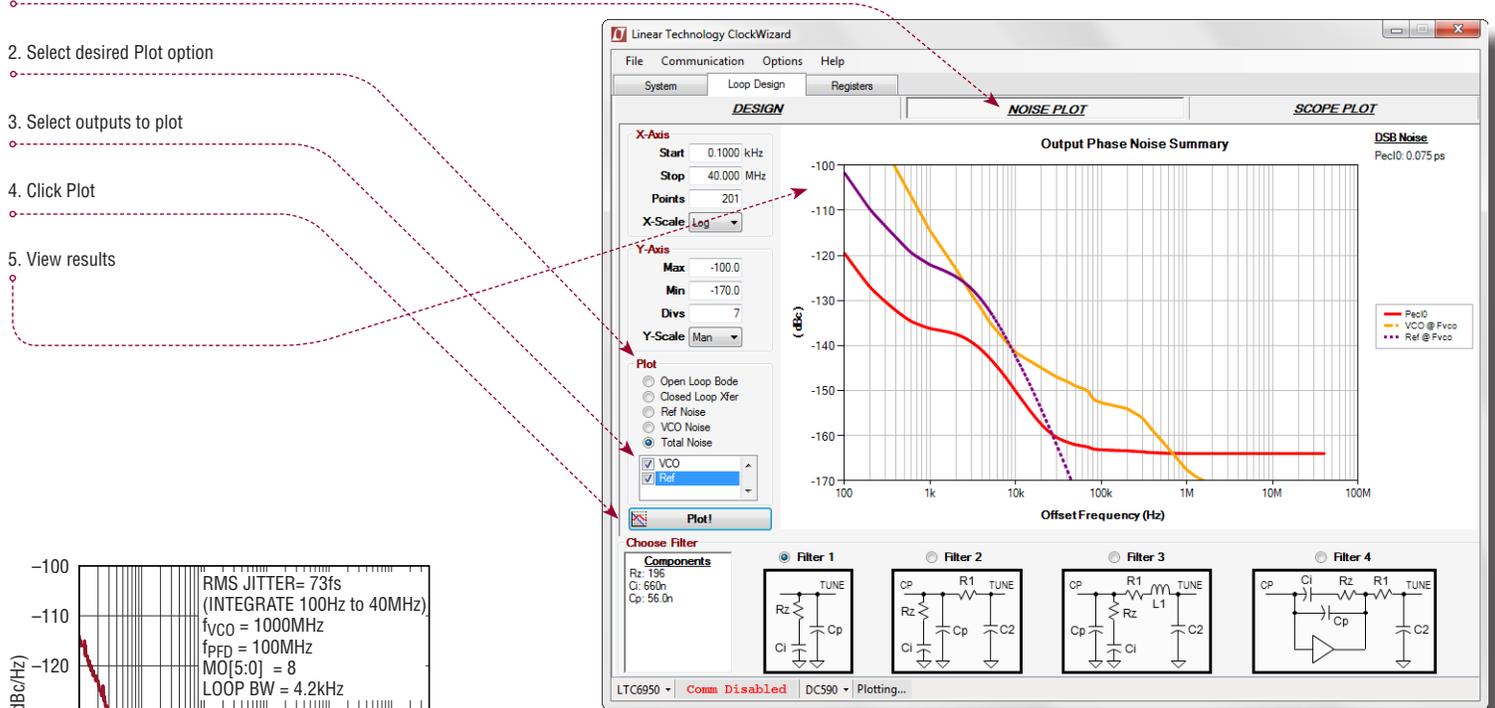f_VCO = 1000MHz
f_PFD = 100MHz
MO[5:0] = 8
LOOP BW = 4.2kHz

Figure 13. LTC6950 PECL0+ measured result at 125MHz