ADSL Line Driver Design Guide, Part 2

by Tim Regan

Part one of this article appeared in *Linear Technology* X:1 (February 2000) and is also available on the Linear Technology web site at www.lineartech.com/ezone/dsl.html. It discusses the different DSL standards, characteristics of the DSL signals, the design of differential drivers for DSL and the requirements for amplifiers used in this application.

Design Calculations, Volts, Amps and Power Dissipation

It is very important to consider the power requirements of the line driver in DSL applications. Although a nominal power level of $100mW_{RMS}$ or less into a 100Ω load does not seem to be a lot of power, the driver must handle large peak signals and therefore requires a larger than nominal power supply voltage. This increases both the power dissipation in the driver package and the peak current capability needed from the power supply. This issue becomes most critical in central office designs, where many DSL ports are included on a single card powered from one supply. Additionally, the heat generated by the drivers must be handled properly to ensure reliable operation.

This section will provide the calculations necessary to determine the voltages, currents and power dissipation for an ADSL driver of either standard. It can be quite useful to place these equations in a spreadsheet to allow quick observation of the effect of different design variables on the overall system. Assuming that a wide band, low distortion driver has been selected (the LT1795 and LT1886 are excellent choices), the three most important system issues to consider are the total supply voltage, the peak output current and the driver power dissipation required.

For these calculations, the RMS voltages required are treated as DC levels for the purpose of estimating the power dissipation. In an actual DSL design this approach overestimates the typical power dissipation with a DMT signal by 10% to 20% because a data transmission is not always at the maximum output power level. The DSP intelligence built into the system automatically adjusts the transmitted power level and frequency spectrum for each connection made. With shorter phone-line loops, the transmitted power is reduced; with longer loops, not all of the channels are used and the number of data bits per channel is reduced. The maximum transmitted power is provided when the connection loop length is in the range of 4000 feet to 10,000 feet and there happens to be a significant level of noise interference and/or low line impedance conditions. Designing to handle the conservative estimate provides a margin of safety for reliable operation.

The Input Variables

Before a design can begin, the following information must be known: which DSL standard is to be used, Full Rate or G.Lite, whether upstream (CPE) or downstream (CO). These same equations apply for any DSL standard (HDSL and HDSL2 for example) with some changes to the input parameters (see Table 1).

Table 1. Input variables

Symbol	Parameter	Description	Typical Values for ADSL
P_{LINE} (dBm)	Line Power	RMS power to be put on the line	20dBm (Full Rate, CO)
			16.3dBm (G.Lite, CO)
			13dBm (Full Rate and G.Lite, CPE)
PAR	Crest Factor	Peak-to-average ratio for the DMT signal	5.3
Z_{LINE}	Line Impedance	Characteristic impedance of the line	100Ω
n	Turns Ratio	The turns ratio of the line coupling transformer	1:1 or higher
P_{LOSS} (dBm)	Insertion loss	The power loss of the transformer being used	0.2dBm to 2dBm
V_{HR}	Headroom Voltage	A function of the output saturation voltages (positive and negative swing) of the driver used. Headroom is twice the larger of the two saturation voltages.	2V to 5V
I_Q	Quiescent Current	Total quiescent (no input signal) supply current of the driver that is not diverted to the load.	10mA to 30mA
e_{IN}	Input Voltage	Maximum peak-to-peak differential input voltage from the AFE (analog front end)	1.5V to $4.5V_{P-P}$

Basic System Requirements

The following equations determine the essential operating requirements independent of the driver amplifier used in the design:

Line Power in Watts:

$$P_{LINE(W)} = 10^{\frac{P_{LINE(dBm)}}{10}} \bullet 1mW \quad (1)$$

example: 20dBm = 100mW.

RMS Line voltage:

$$e_{LINE(RMS)} = \sqrt{P_{LINE(W)} \bullet Z_{LINE}} \quad (2)$$

Power to the primary of the transformer:

$$P_{PRI(dBm)} = P_{LINE(dBm)} + P_{LOSS(dBm)} \quad (3)$$

$$P_{PRI(W)} = 10^{\frac{P_{PRI(dBm)}}{10}} \bullet 1mW$$

Impedance of primary of the transformer:

$$Z_{PRI} = \frac{Z_{LINE}}{n^2} \quad (4)$$

Transformer termination resistors:

$$R_{BT1},\ R_{BT2} = \frac{Z_{PRI}}{2} \quad (5)$$

Primary RMS voltage:

$$e_{PRI(RMS)} = \sqrt{P_{PRI(W)} \bullet Z_{PRI}} \quad (6)$$

Transformer primary RMS current:

$$I_{PRI(RMS)} = \frac{e_{PRI(RMS)}}{Z_{PRI}} \quad (7)$$

Driver amplifier RMS output voltage:

$$e_{AMPLIFIER(RMS)} = \left(\frac{Z_{PRI} + (2 \bullet R_{BT})}{Z_{PRI}}\right) \bullet e_{PRI(RMS)} \quad (8)$$

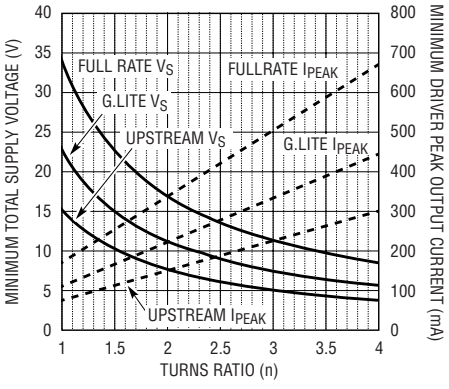


Figure 1. Minimum peak-to-peak driver output voltage and peak output current required, ideal amplifier and transformer

This is the RMS voltage between the two amplifier outputs. If the R_{BT} resistors are properly sized this voltage is twice the RMS voltage of the transformer primary.

Peak driver amplifier output current:

$$I_{PEAK} = \frac{E_{PRI(RMS)} \bullet PAR}{Z_{PRI}} = I_{PRI(RMS)} \bullet PAR \quad (9)$$

The peak current handling capability is key to selecting the driver amplifiers.

Power supplied by the driver amplifiers:

$$P_{OUT} = e_{AMPLIFIERS(RMS)} \bullet I_{PRI(RMS)} \quad (10)$$

Overall line driver voltage gain:

$$A_{V(TOTAL)} = \frac{e_{LINE(RMS)} \bullet 2 \bullet PAR}{e_{IN}} \quad (11)$$

Differential amplifier voltage gain:

$$A_{VDIFF(AMPLIFIERS)} = \frac{e_{AMPLIFIERS(RMS)} \bullet 2 \bullet PAR}{e_{IN}} \quad (12)$$

The turns ratio of the transformer used is critical to the overall design. Figure 1 illustrates the minimum total supply voltage across the driver and the peak driver output current required as a function of the turns ratio. These are the absolute minimum requirements based on an ideal amplifier that has 0V headroom and is therefore able to swing fully to either supply voltage rail, and an ideal transformer, with zero insertion power loss. A practical implementation will require a larger supply voltage, as determined from the next section. Trying to design a system with less supply voltage or current capability using conventional transformer termination resistors will result in clipping and transmission data errors.

Figure 1 also compares the different ADSL standards with the central office, downstream, Full Rate ADSL, which requires the most current and voltage. The reduced line power requirements for the downstream G.Lite and the upstream Full Rate and G.Lite modems produce designs with lower voltage and current requirements.

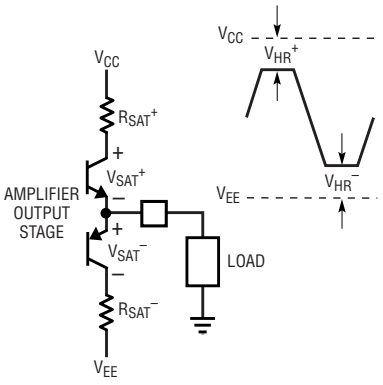
Important Driver Characteristics: Headroom Voltage and Quiescent Current

To determine the required supply voltage, power consumption and power dissipation of the driver, the headroom voltage and required quiescent current of the driver amplifier must be considered.

Minimum total supply voltage for the amplifiers:

$$V_{SUPPLY(MIN)} = E_{AMPLIFIER(RMS)} \bullet PAR + V_{HR} \quad (13)$$

The actual supply voltage for the driver amplifier must be set above the minimum peak-to-peak amplifier output swing to provide for the headroom voltage to prevent peak signal clipping. Using a supply voltage greater than this minimum value will increase the power dissipation in the driver amplifiers.



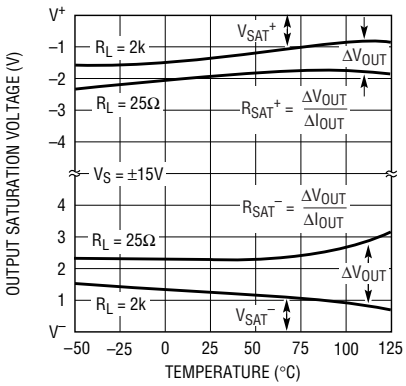


Figure 2. Typical output stage model and common data sheet curves are used to determine amplifier headroom voltage

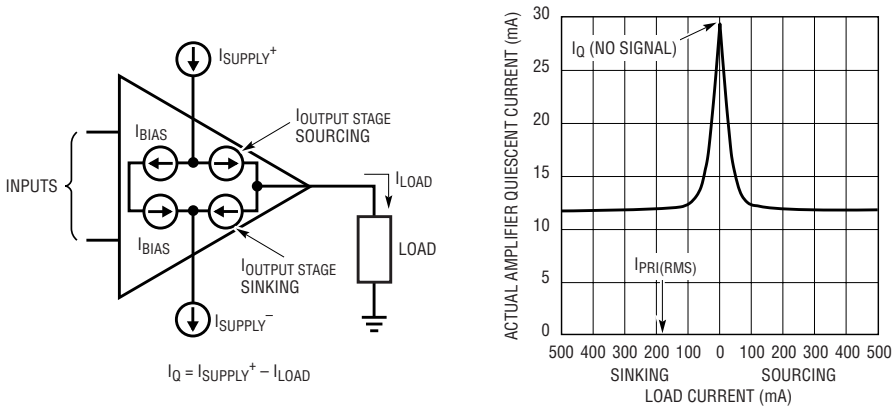


Figure 3. Much of an amplifier's quiescent current is transferred to the load current

The headroom voltage of an amplifier is determined from either the guaranteed specification for output voltage swing or from characteristic curves showing output saturation voltage vs output current or vs temperature with different load currents. The headroom voltage is the difference between the supply voltage rail and the maximum output voltage swing, both positive and negative, for a given load current. Figure 2 shows a simple model for determining an amplifier's output saturation voltages and an example of a useful data sheet curve.

During large signal transients, the transistors in the output stage of the amplifier will fully turn on to pull the output as close as possible to the supply voltage rails. The limitation on how close the signal can swing can be modeled as a fixed voltage drop across the transistor being driven with a resistance in series. This resistance increases the voltage swing limitation in proportion to the amount of load current the transistor must source or sink. The combined total of the fixed voltage drop and the voltage across the resistor is called the output saturation voltage. The values to use to model this characteristic can be determined from a data sheet curve. Figure 2 shows the curve that appears on the LT1795 data sheet.

This curve shows the positive and negative amplifier saturation voltages vs junction temperature with two different values of load resistance. DSL line drivers typically run warm, so the area of interest on the curve will be in the range of junction temperature around 50°C. To determine the fixed voltage part of the model for the positive output swing, V_{SAT}^+, evaluate the top curve with R_L = 2k. From the curve it can be seen that the output will swing to within 1.2V of the positive supply. Because the curve was generated using supplies of ±15V, the load current at 50°C is only 13.8V/2kΩ or 7mA. To determine the value for the series resistance in the model, determine the change in output saturation voltage with a change in load current. At the same 50°C junction temperature point, evaluate the upper curve with R_L = 25Ω. With this load the output swings to within 1.8V of the positive rail and the load current is 13.2V/25Ω or 528mA. The series resistance is then $\Delta V_{SAT}/\Delta I_{OUT}$ (0.6V/521mA), which is 1.15Ω. From these values, the positive amplifier saturation voltage will be 1.2V + 1.15Ω • I_{PEAK} where the value of I_{PEAK} depends on the particular modem design. Applying the same approach for the amplifier swing towards the negative rail results in saturation voltage model parameters of 1.2V in series with a resistance of 2.2Ω.

With these values modeling the output saturation characteristics of the LT1795, at any level of peak output current the output stage will saturate or clip when swinging towards the negative supply before it will clip on the positive swing, due to the higher effective series resistance voltage drop. Transmission errors can occur if either output swing excursion clips, so when sizing the total supply voltage requirement for the driver the total headroom voltage of the amplifier, V_{HR}, should be twice the larger of the two output saturation voltages. This will ensure that the output will not clip at all during maximum peak signal conditions.

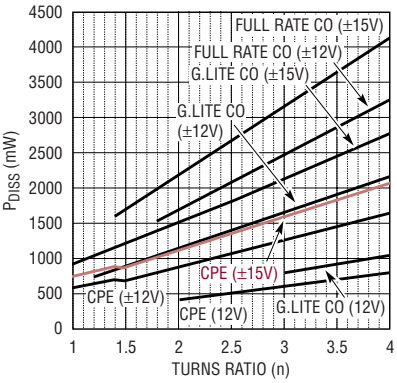
With V_{SUPPLY} set large enough to prevent signal clipping the total power consumption from the supplies can be determined with Equation 14:

Power consumption of the complete line driver:

$$P_{IN} = V_{SUPPLY} \bullet (I_Q + I_{PRI(RMS)}) \quad (14)$$
$$= (V_{EXTRA} + V_{HR} + V_{AMPLIFIER(RMS)} \bullet PAR) \bullet (I_Q + I_{PRI(RMS)})$$

This equation introduces two new terms, V_{EXTRA} and I_Q. V_{EXTRA} is the total additional power supply voltage above $V_{SUPPLY(MIN)}$ that is actually used to power the driver amplifiers. For example, if the minimum total supply voltage for a design is determined to be 20V (or ±10V) but the actual supplies available are ±12V, then the V_{EXTRA} term will be 24V – 20V or 4V. The total power consumption of each line driver is very important when sizing the power supply for both voltage and current capability to be used in the system. This becomes most significant when multiple DSL ports are to be powered from a predesigned power supply. The power supply could become the limiting factor to the number of ports allowable.

The quiescent current, I_Q, is basically the operating supply current of the driver amplifiers. This is the cur-



ASSUMPTIONS

	FULL RATE	G.LITE	CPE
I_Q	28mA	18mA	14mA
V_{HR}	3V	2.5V	2V
P_{LOSS}	0.5dBm	0.5dBm	0.5dBm

Figure 4. Driver power dissipation vs turns ratio: a practical implementation

rent required to bias the internal circuitry of the amplifiers. In general, high speed, high output current amplifiers that process signals with very low distortion require significantly more operating current than general-purpose amplifiers. This current adds to the power consumption and power dissipation of the driver package, because it must always be supplied whether there is signal applied or not. However, the power dissipation in the driver for the quiescent current is not just a fixed DC power of $I_Q \bullet V_{SUPPLY}$. As seen in Figure 3, much of the quiescent current is diverted to the amplifier output stage and becomes part of the load current while processing a signal. The curve shown is again for the LT1795 driver. With no load, all of the 30mA quiescent current flows from the positive supply through the amplifier to the negative supply. However, when the load is sourcing or sinking 500mA, only 12mA flows through the amplifier, the remaining 18mA is taken by the output stage and diverted to become part of the load current. To obtain an accurate estimate of the average power dissipation of the drivers, this sharing of the quiescent current should be taken into account. This will prevent overdesign of the thermal management area of concern. The I_Q term in Equation 14 should be the only current that continues to flow through the amplifier at the load current level of $I_{PRI(RMS)}$. The diverted quiescent current is included in the $I_{PRI(RMS)}$ term.

Unfortunately, this curve of quiescent operating current vs load current is not found on typical data sheets. Some characterization of the chosen amplifier should be done. The design of amplifier power output stages is varied and has a direct effect on the diversion of the total supplied operating quiescent current.

Power dissipated in the line driver amplifiers:

$$P_{AMPLIFIERS} = P_{IN} - P_{OUT} \quad (15)$$
$$= e_{AMPLIFIERS(RMS)} \bullet [PAR \bullet I_Q + I_{PRI(RMS)} \bullet (PAR - 1)] + (V_{HR} + V_{EXTRA}) \bullet (I_Q + I_{PRI(RMS)})$$

The power dissipated in the driver package is important to consider when addressing heat management issues.

To minimize power dissipation, the driver should be powered from a power supply with voltages set to the minimum required. Most implementations, however, use existing power supply voltages, typically ±15V, ±12V or just the 12V rail for the line driver/receiver. Figure 4 provides an indication of the actual power dissipation in the line-driver amplifier package with commonly available supply voltages and a range of transformer turns ratios. This is a practical example where values have been assumed for the amplifier headroom and quiescent current and some transformer power loss. The lower power upstream modems require less operating current, which helps to minimize the package power dissipation. If the turns ratio is too low for the given supply voltage, the lines on the graph terminate because the supply voltage is not large enough to prevent clipping of the DMT signal peaks.

As previously stated, the power dissipation in the driver is an important concern as it generates heat in the system. For each of the ADSL standards, a certain minimum amount of power dissipation is required. Three factors that add to this power dissipation are the amplifier headroom voltage, the amplifier quiescent operating current and the power loss of the line-coupling transformer. Attention to these three factors when selecting an amplifier and transformer can optimize the overall power dissipation. Analysis of the sensitivities of the amplifier power dissipation (see Equation 15) for each of these three terms is summarized in Table 2. This shows the effect on total package dissipation for each factor taken individually with the other two factors set to zero. The term *n* is the transformer turns ratio.

The factors in Table 2 provide a rough indication of the additional power dissipation from these three system variables. The combined effect on power dissipation from I_Q, V_{HR} and P_{LOSS} must still be determined from Equation 15.

Optimizing Power Dissipation, Adjustable Quiescent Current and Shutdown

Several high speed power amplifiers from Linear Technology provide the ability to externally set the operating quiescent current. For the design of any of the DSL standards, this allows for fine tuning the amplifier's

Table 2. Additional power dissipation factors

Standard	ADSL Full Rate Downstream	G.Lite Downstream	Full Rate and G.Lite Upstream	Additional Power Dissipation
Minimum Power Dissipation, P_{MIN}	860mW	367mW	172mW	
Amplifier Quiescent Current, I_Q	33.5mW/n	22.14mW/n	15mW/n	Per 1mA of I_Q, P_{DISS} = (FACTOR) • (I_Q/1mA)
Total Amplifier Headroom Voltage, V_{HR}	n • 31.6mW	n • 20.9mW	n • 14.1mW	Per 1V of V_{HR}, P_{DISS} = (FACTOR) • (V_{HR}/1V)
Transformer Insertion Loss, P_{LOSS} in dBm	2.3%	2.3%	2.3%	Per 0.1dBm of P_{LOSS}, P_{DISS} = $P_{MIN} \bullet 1.023 \bullet \left(\frac{P_{LOSS(dBm)}}{0.1dBm} - 1\right)$

operating point for minimum power dissipation and adequate distortion performance. There is a direct trade-off between the two, however. Designing for very low quiescent current significantly reduces the power dissipation, but obtaining the lowest distortion performance requires additional biasing current for the internal amplifier circuitry. Figure 5 illustrates the adjustability of the operating current for the LT1795. An internal current source is programmed via a single external resistor. The current through this source is mirrored and scaled up to become the biasing current for the two amplifiers. Also shown in Figure 5 is the effect of adjusting the operating current on distortion. The spectrum analyzer plots show the intermodulation components from twenty carrier tones (from 200kHz to 500kHz). With too low of an operating current, the signal on the line is far too distorted and interference with other channels is inevitable. However turning up the current drops all of the distortion products into the noise floor. This adjustment should be made during the evaluation of the driver under actual transmission conditions and optimized for the highest data rates obtainable.

The best power and thermal management technique in multiple-port systems or energy efficient standalone modem designs is to shut off the driver when the line is inactive. The digital circuitry always knows when there is no data transmission activity and can issue a signal to the driver to shut down operation. Many drivers accept this control signal and completely power down the internal circuitry. The LT1795, for example, can be shut down to consume less than 200µA of current when not required to transmit data. When commanded to power up, the driver requires only a few microseconds to reestablish full performance, an insignificant time when compared to a typical communication training-up interval. When powered down, however, the output stage of the amplifier loses all bias and enters a high impedance state. This essentially opens the connection to the transformer back-termination resistors. As these resistors are often used to sense the received signal from the line, no signal can be developed across them if they are left floating.

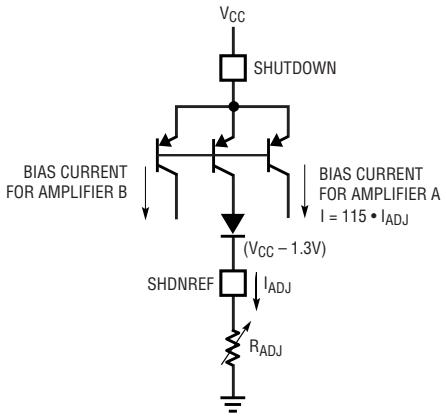


Figure 5a. Proper adjustment of the operating current minimizes spectral components, adjusting the sujpply current

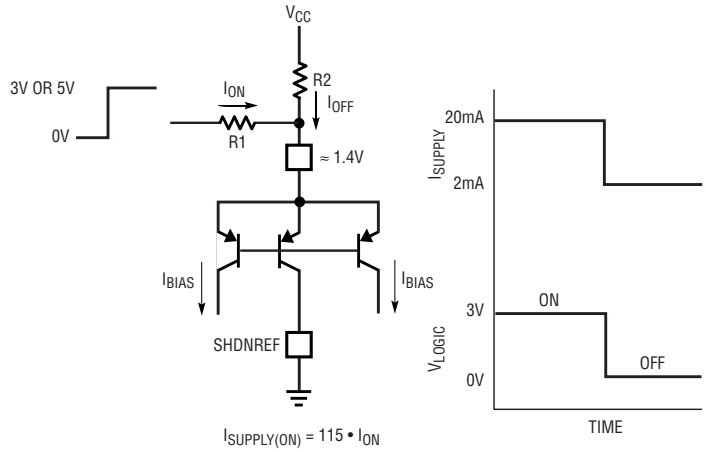


Figure 6. How to reduce driver supply current in an idle channel while maintaining the receiver function

Figure 6 illustrates a power saving function, called partial shutdown, that keeps the amplifier slightly biased and thus allows the modem to continue to monitor the line for transmission signals to be received. Here, two resistors are carefully chosen to control the amount of operating quiescent current as well as to retain a small amount of "keep-alive" current when shut down. Resistor scaling can accommodate a direct connection to an I/O pin from the DSP processor with any logic voltage level. Shutting down to a quiescent current level of 2mA keeps the output stage active and terminates the received signal sensing resistors, resulting in a better than 10-to-1 reduction in idle-channel power consumption and dissipation.

Thermal Management

Depending on the ADSL standard being applied, the power supplies and the transformer turns ratio used, the driver amplifier package will dissipate somewhere between 500mW and 2W. The average power dissipation

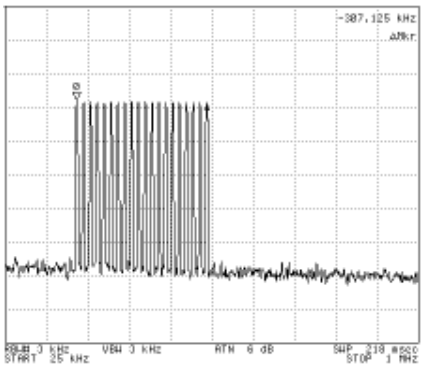


Figure 5b. Spectrum of 20 carrier tones with I_Q of 12mA/amplifier

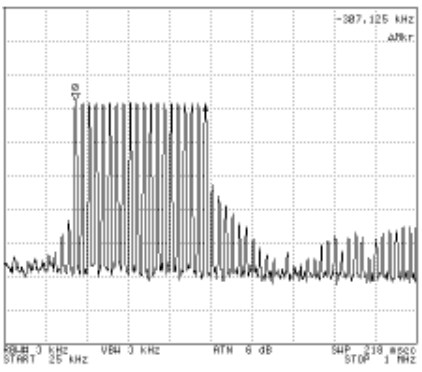


Figure 5c. Spectrum of 20 carrier tones with I_Q of 2.2mA/amplifier

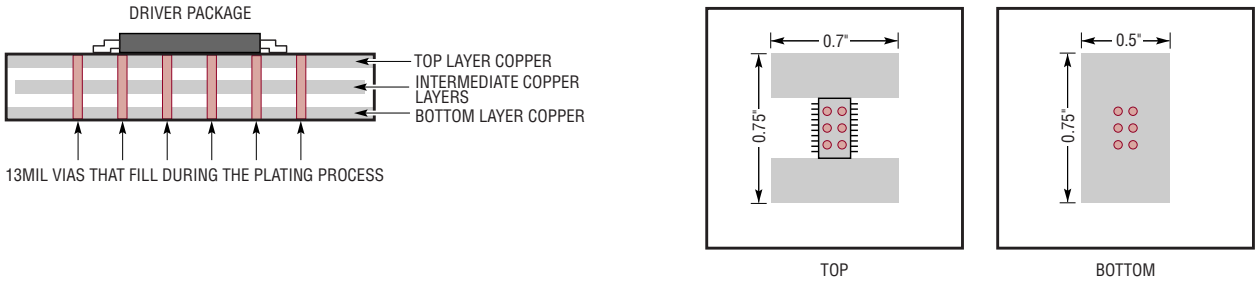


Figure 7a. Using PCB copper foil for heat sinking

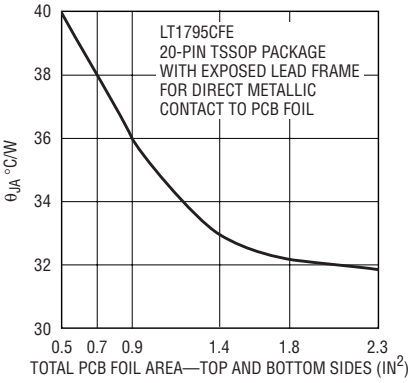


Figure 7b. Improving Heat dissipation with increased copper foil area

times the overall thermal resistance from the junction of the driver to the ambient air will determine the rise in operating junction temperature above the maximum ambient temperature. Most power amplifiers have a built in thermal protection mechanism that will disable the output stage when the junction temperature exceeds typically 160°C. Should this temperature ever be reached, the amplifier will protect itself, but data transmission errors will abound and most likely result in a data transmission disconnect. Designing a heat-spreading system to limit the driver junction temperature to less than 125°C at the highest expected ambient temperature will ensure continuous operation.

Fortunately, the power dissipation levels are not so high that external heat sinks are necessarily required, so heat spreading can usually be managed through planes of PCB copper foil. In addition, the packaging of most power amplifiers uses thermal conduction enhancements, such as fused or exposed lead frames. Fused lead frames have several package pins connected directly to the metal pad where the IC is attached. This provides a continuous path for heat transfer from the junction of the IC, out of the plastic encapsulation, to pins that are directly connected to PCB copper planes. An exposed lead frame does not plastic encapsulate the underside metal where the IC is attached. This provides a metal pad that can be connected directly to PCB copper for direct transfer of heat from the IC mounting junction heat source to the ambient air. An exposed lead frame allows for very small packages, such as that used for the LT1795CFE, a 20-pin TSSOP, to have thermal conductivity characteristics similar to much larger sized packages. Very small packages with good thermal conductivity can result in very dense multiport ADSL systems for central office applications.

The best way to spread the heat generated by the driver is to use as many planes of copper as are available and to "stitch" them together through small vias from the topside of the board to the bottom, as shown in Figure 7. These vias should be small enough in diameter (15 mils or less) that they are completely filled with solder during the plating process. This provides a continuous thermal conductivity path from the top of the board to the bottom for the most exposure to the ambient environment. There are no fixed rules for determining the lateral area of the copper planes on the PCB, other than "bigger is better," and 2oz copper is a thicker and therefore better thermal conductor than 1oz copper. Figure 7 also provides an indication of the improvement in the heat spreading thermal resistance from junction to case with various amounts of copper foil area on the top and bottom sides of a PCB.

As most of the heat is dissipated in the area immediately surrounding the driver amplifier package, there comes a point of diminishing returns where more copper area does not provide much additional benefit. This can be seen in the plot of thermal resistance in Figure 7 where, beyond a total PCB area of $1in^2$, further reduction in thermal resistance is minimal. One word of caution regarding PCB planes for heat spreading is that the fiberglass material (typically FR-4) is a fairly good thermal insulator. Any component interconnect traces that cut through the plane of copper significantly reduce the effectiveness of the lateral area. Interconnect traces should be made on the inner layers of multilayer boards to minimize the distance between components. The complex interconnect of the logic circuits used in DSL modems usually requires a multilayer PC board that can be put to good use in the line driver area.

Another measure that can be taken is to provide some forced airflow cooling. A linear flow of air across the driver package can significantly reduce the effective thermal resistance from junction to ambient (θ_{JA}) of the heat-spreading system. A reduction of 2°C/W to 3°C/W for each 100lfpm (linear feet per minute) can

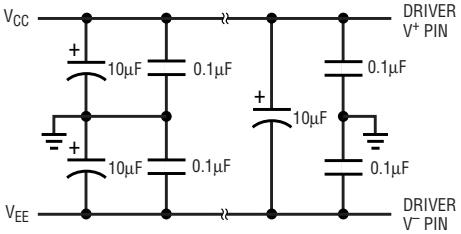


Figure 8. Recommended power supply bypassing for any design

be achieved. This is particularly important in a multiport system housed in an enclosed case.

A Gallery of Design Recommendations

This section will provide examples of driver and receiver circuits for each of the ADSL standards. These circuits provide a good starting point for implementing the line interface functions for a DSL modem. The circuits were designed with all of the considerations mentioned so far, but other system variables, such as available supply voltages or AFE output and input dynamic range, could mandate some modifications. The total voltage gain of each line-driver design, from the differential input voltage to the actual voltage output to the phone line, has been scaled to a value that requires less than $3V_{P-P}$ from the AFE providing the transmitted signal. The gain of the amplifier stage is adjusted to take into account the signal boost of the transformer used as well as the signal loss through the back-termination resistors.

Common to all of the designs is a good power supply bypassing approach. This is shown in Figure 8. A large- and a small-valued bypass capacitor at the points where the supplies connect to the board provide decoupling of noise and ripple over a wide frequency range. Additional high frequency decoupling at the driver and receiver supply pins is recommended. Another large-valued bypass capacitor connected directly between the supply pins of the driver helps to reduce the 2nd harmonic component of ripple on the supply lines. This component comes from the peak current demands from each supply, which occur twice for each input signal cycle due to the differential amplifier topology (each amplifier sources and sinks the peak current once each signal cycle).

The Differential Receiver

Not all DSL modems will require a receiver circuit. Some analog front end ICs have sophisticated circuitry for a very wide dynamic input range to directly pick the small received signals out of the noise floor after passing through the receive/echo filter. Other designs may use a second transformer to process the differential received signal directly to the filter/AFE. Many designs still prefer to sense the differential signal across the termination resistors and provide gain to the received signal before passing it through the filter to the AFE. This basic differential receiver circuit

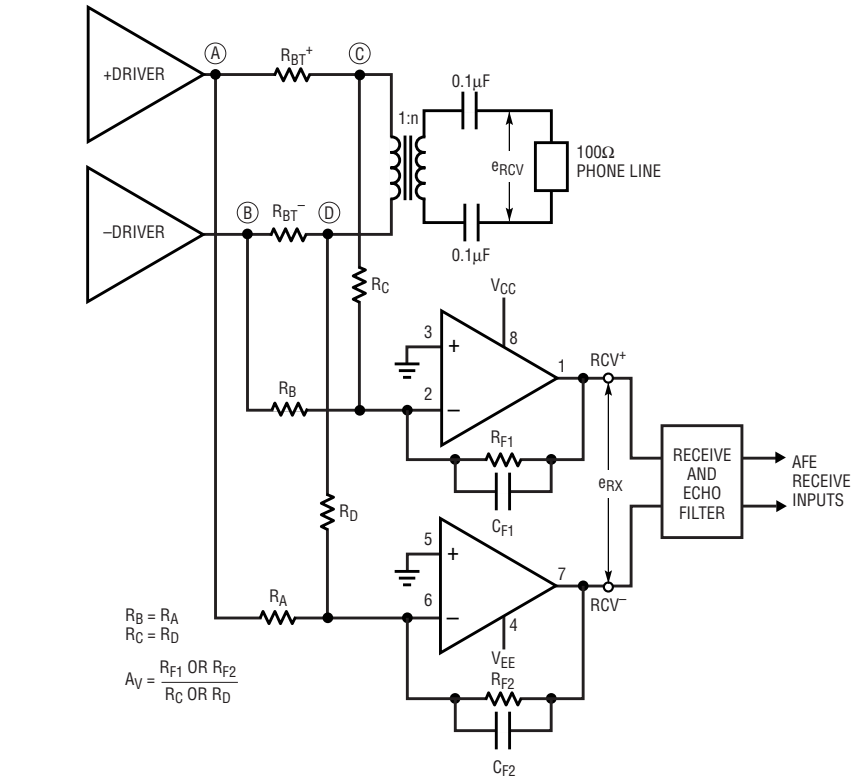


Figure 9. Basic differential receiver (4-wire to 2-wire)

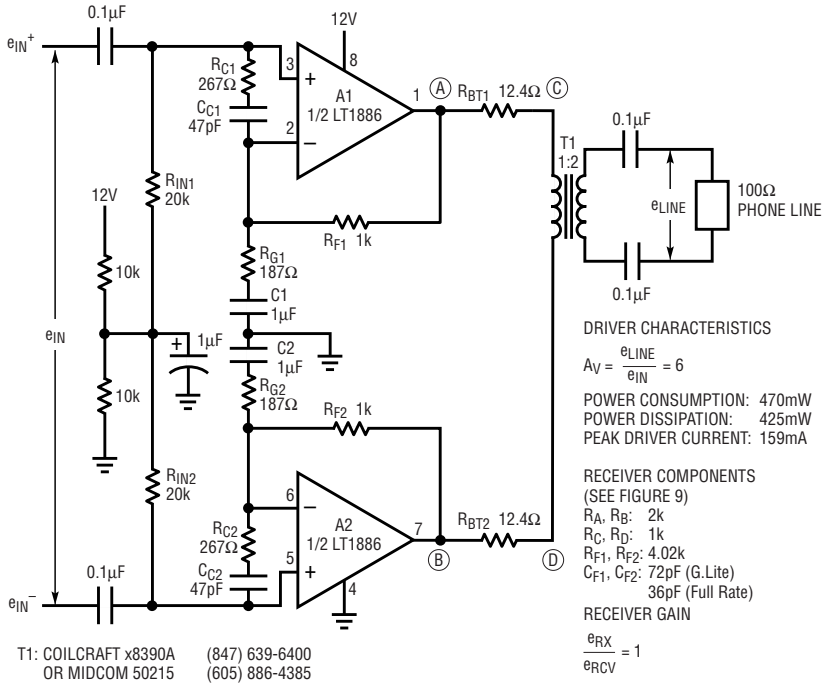


Figure 10. Full Rate or G.Lite upstream (CPE) driver

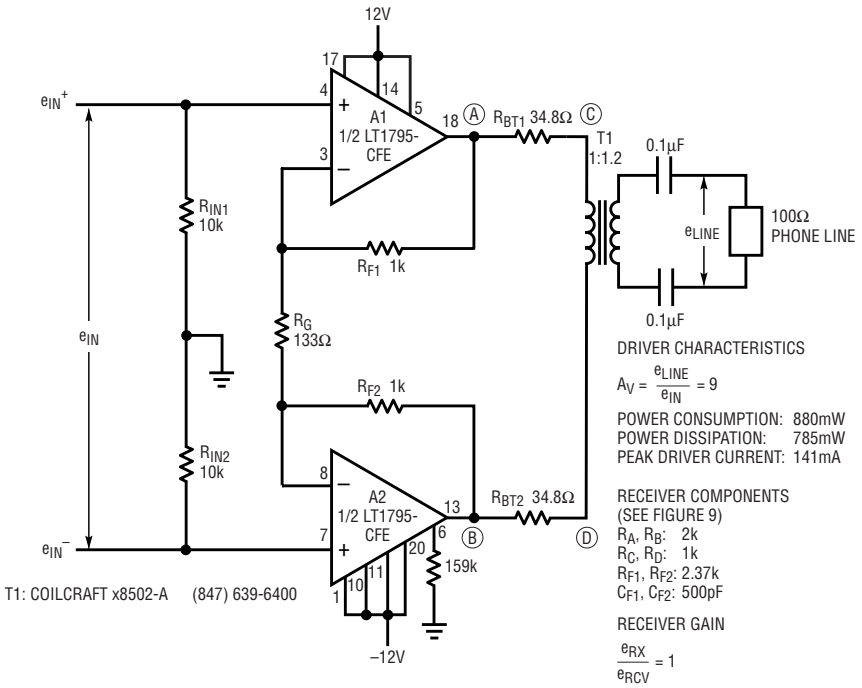


Figure 11. ADSL G.Lite downstream (CO) line driver

is shown in Figure 9. Each receiver amplifier is a summing stage that sums the received signal and the attenuated transmitted signal seen at the primary of the transformer with a weighted, opposite-phase transmitted signal. This weighted summing of the transmitted signal ideally cancels the 180° out-of-phase signals, leaving only the received signal at the differential amplifier outputs. This is called local echo cancellation. In a standard line-driver design, the transmit signals at nodes A and B in Figure 9 are twice the magnitude of the signals at nodes C and D. To cancel these signals in the receiver requires resistors R_A and R_B be set to exactly twice the value of resistors R_C and R_D.

The gain of the receiver is simply the inverting gain of the received signal path, R_{F1}/R_C and R_{F2}/R_D. In the driver design examples to follow, the receiver input resistors connect to the driver at nodes A through D. The recommended component values for the receiver provide for unity gain from the received signal appearing at the line to the differential receiver output. This takes into account the attenuation of the line-coupling transformer. A small feedback capacitor is also shown that reduces the gain at a frequency just above the received signal bandwidth, which varies depending on the application.

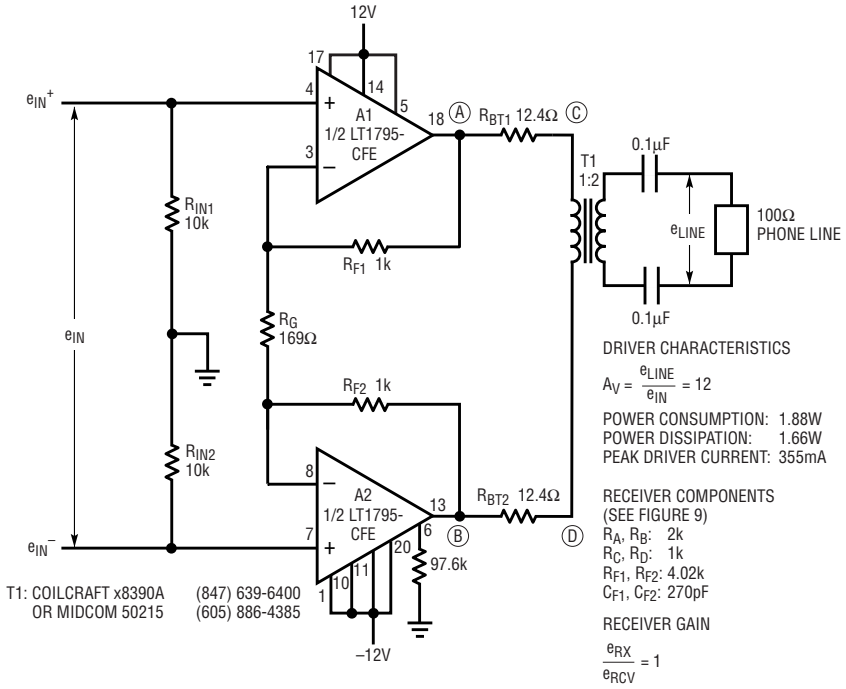


Figure 12 ADSL Full Rate downstream (CO) line driver

ADSL Full Rate or G.Lite Upstream (CPE) Line Driver

This driver (Figure 10) is the lowest powered of the ADSL standards, consuming less than 500mW. The lower line power, 13dBm, and resulting lower peak current requirement allows the use of the LT1886, which is a high speed 200mA dual amplifier. The use of a 2:1 transformer turns ratio allows this driver to be powered from a single 12V power supply.

In order to obtain the highest open-loop gain and bandwidth to minimize distortion, the LT1886 is decompensated and is only stable with closed-loop gains of ten or greater. In this design the signal gain of each amplifier is only 6.35. To remain stable with this low value of gain requires the addition of gain-compensation components R_{C1}, C_{C1}, R_{C2} and C_{C2}. These components, which come into play only at frequencies greater than 15MHz, parallel the gain-setting resistances, R_{G1} and R_{G2}, to make the feedback factor of each amplifier a value of 0.9, which is the same as having a closed-loop gain of ten; thus, stability is ensured.

The LT1886 is a 700MHz gain bandwidth amplifier. The combination of gain at such high frequencies and not being unity gain stable requires that the gain-setting resistors be returned to a low impedance at all frequencies. For this reason, the two gain setting

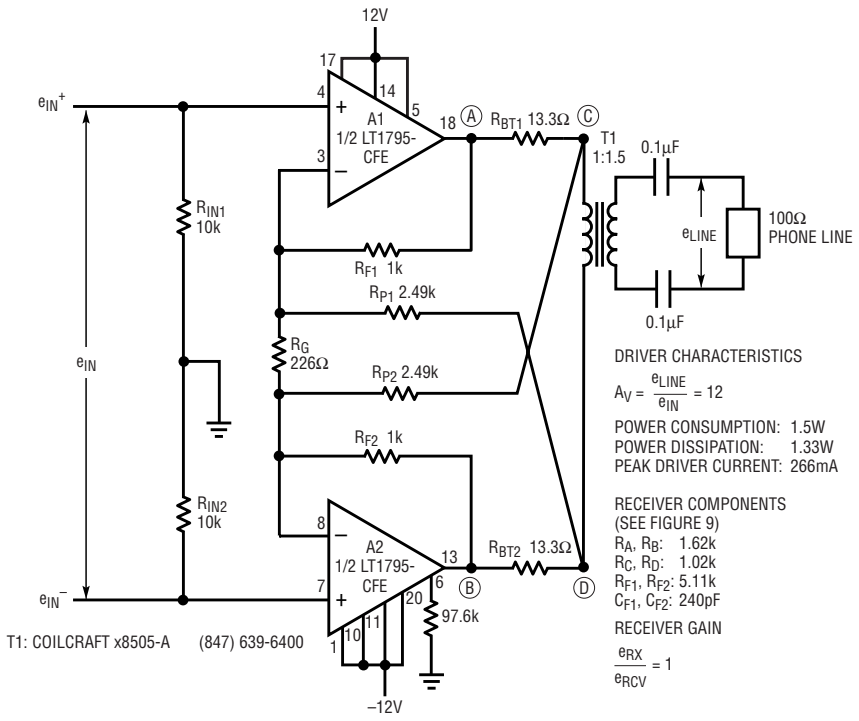


Figure 13. Reduced power dissipation ADSL Full Rate downstream (C) line driver

resistors are connected to ground rather than using a single resistor connected to the other amplifier's inverting input. Capacitors C1 and C2 are included to prevent applying gain to the DC offset voltages of the amplifiers. The different values of feedback capacitors for the receiver amplifier account for the frequency spectrum of the downstream information from the CO modem in either the Full Rate (1104kHz) or G.Lite (552kHz) implementation.

ADSL G.Lite Downstream (CO) Line Driver

This moderate power (16.4dBm) driver requires less than 1W and is shown in Figure 11. This design is biased from ±12V supplies and uses a transformer with a turns ratio of only 1:1.2. Although the peak current is only 140mA, the LT1886 cannot be used due to its limited operating supply voltage of 13.2V total. Instead the LT1795CFE, which is in a very small TSSOP power package, is used. This small package is ideal for central office, multiple DSL port designs for compacting a high number of drivers on a single PC card.

ADSL Full Rate Downstream (CO) Line Driver

Figure 12 is the highest powered DSL line driver application, used in central office applications to obtain up to 8Mbps data rates throughout the Internet. This design uses standard back termination and can be powered from ±12V supplies by using a 2:1 turns ratio transformer. This results in a fairly high, 355mA peak output current demand from the amplifiers. The LT1795, with a 500mA output current rating, once again is capable of the task.

Reduced Power Dissipation ADSL Full Rate Downstream (CO) Line Driver

To address the power consumption and dissipation issues for Full Rate ADSL drivers, a slightly modified topology can be used, as shown in Figure 13. Recognizing that one-half of the power provided by the amplifiers is lost in the transformer back-termination resistors, an obvious approach to reduce power is to simply reduce the value of these resistors. Doing so, however, modifies the output impedance of the modem as seen from the phone line and also reduces the amount of received signal developed across these sensing resistors. Although it is powered by ±12V supplies, the circuit of Figure 13 achieves 300mW of power savings. The driver current is substantially reduced by using a transformer turns ratio of only 1.5:1. Normally, this would require a higher supply voltage of ±14V and R_{BT} resistors of 22.2Ω. However, although the R_{BT} resistors are reduced to 13.3Ω, the circuit still maintain the proper line-impedance termination of 100Ω and operates from ±12V supplies. It is not suitable for every application, however, because it still reduces the amount of received signal. It is most applicable for systems that use a sensitive receiver AFE that can still detect the reduced received signal.

The approach is termed active termination. A small amount of positive feedback in each amplifier is obtained from the opposite amplifier output. This feedback makes the effective output impedance seen looking into the circuit at nodes C and D the proper value even though the R_{BT} resistor has been reduced by 40% from what is should be. The design equations for this topology are as follows.

Instead of using the standard value of R_{BT} resistance, it can be reduced to any value desired, with attendant received-signal loss. A factor called K can be used to define the new R_{BT} resistance:

$$R_{BT} = \frac{K \bullet Z_{LINE}}{2 \bullet n^2} \quad (16)$$

With standard termination and a 1:1.5 turns ratio transformer, the value of R_{BT} should be 22.2Ω. In the design of Figure 13, this resistor is reduced by 40% to 13.3Ω, therefore the factor K = 0.6.

The normal forward path circuit gain from the noninverting input of each amplifier to the output nodes A and B is a term called G where $G = 1 + R_F/R_G$.

The gain of the positive feedback signal path for each side (from node D to A and from node C to B, is called P where $P = R_F/R_P$.

Table 3. Driver and receiver amplifier characteristics

Line Drivers						
Part	**LT1795**	**LT1207**	**LT1886**	**LT1497**	**LT1206**	**LT1210**
Single/Dual	Dual	Dual	Dual	Dual	Single	Single
Output Current	500mA	250mA	200mA	125mA	250mA	1.1A
Supply Voltage	10V to 30V	10V to 30V	5V to 13V	5V to 30V	10V to 30V	10V to 30V
Gain Bandwidth Product	50MHz	60MHz	75MHz	50MHz	60MHz	35MHz
Slew Rate	900V/µs	900V/µs	200V/µs	900V/µs	900V/µs	900V/µs
I_Q/Amplifier	1mA to 30mA	1mA to 30mA	7mA	10mA	1mA to 30mA	1mA to 50mA
V_{SAT}^+	1.2V	1.2V	0.75V	1.2V	1.2V	1.2V
V_{SAT}^-	1.2V	1.2V	0.9V	1.15V	1.2V	1.25V
R_{SAT}^+	1.2Ω	3.2Ω	3.1Ω	14Ω	3.2Ω	0.9Ω
R_{SAT}^-	2Ω	5.3Ω	2.3Ω	10Ω	5.3Ω	1.7Ω
Dual-Amplifier Receivers						
Part	**LT1355**	**LT1358**	**LT1361**	**LT1364**	**LT1813**	**LT1253**
Supply Voltage	5V to 30V	5V to 30V	5V to 30V	5V to 30V	5V to 12V	10V to 24V
Gain Bandwidth	12MHz	25MHz	50MHz	70MHz	100MHz	90MHz
Slew Rate	400V/µs	600V/µs	800V/µs	1000V/µs	750V/µs	250V/µs
Noise Voltage	10nV/√Hz	8nV/√Hz	9nV/√Hz	9nV/√Hz	8nV/√Hz	3nV/√Hz
I_Q/Amplifier	1.25mA	2.5mA	5mA	7.5mA	3mA	6mA

Using these abbreviations:
For proper impedance matching: P = 1 – K.

To obtain a desired voltage gain from the AFE output to the line, A_V, the term G is set to:

$$G = \frac{A_V \bullet e_{PRI}}{e_{LINE}} \bullet (1 + K - P) - P \qquad (17)$$

where e_{PRI} and e_{LINE} are the voltages at the transformer primary and on the line, determined by taking into account the turns ratio and transformer insertion loss.

The use of a high performance amplifier such as the LT1795 does not result in any degradation of distortion performance when modifying the closed-loop gain by positive feedback. Significant power savings can be obtained but the design may not be suitable for all applications as previously mentioned.

Conclusion

Following the design procedures described in this article should make the design and implementation easy and accurate. At the very least, it will ensure that power and heat issues receive proper consideration.

Linear Technology offers a variety of high speed, low distortion power amplifiers and low noise dual amplifiers that can be used to implement the driver/receiver functions of the DSL modem (see Table 3).

Authors can be contacted at (408) 432-1900

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