DESIGN SOLUTIONS
POWER

maxim integrated™

Power Your Computationally Intensive Application Processor with a Single PMIC

Demand for highly flexible and adaptive PMICs to power application processors (APs) is growing thanks to new applications like virtual reality (Figure 1), embedded vision, object action, pedestrian detection, and gesture recognition, which all require deep learning algorithms. APs must be highly flexible and reconfigurable to implement the newest and most efficient algorithms and add new features as necessary. The system solution mandates low power consumption since many of these applications are portable. Accordingly, the PMIC must support dynamic loads and low-power mode transitions, while being small and highly efficient, to minimize energy waste and extend untethered operation. This article discusses the challenge of powering APs in these applications and provides an example PMIC which is best-in-class for size and efficiency.

Figure 1. Virtual Reality Device in Action

Typical Virtual Reality System

The block diagram of a virtual reality (VR) headset is shown in Figure 2. The VR headset is a computationally intensive environment. The image display requires a specialized graphics processing unit (GPU) and an image processing unit (IPU) to enhance customer experience. Audio processing requires fast digital signal processing (DSP), while the entire system is orchestrated by the central processing unit (CPU).
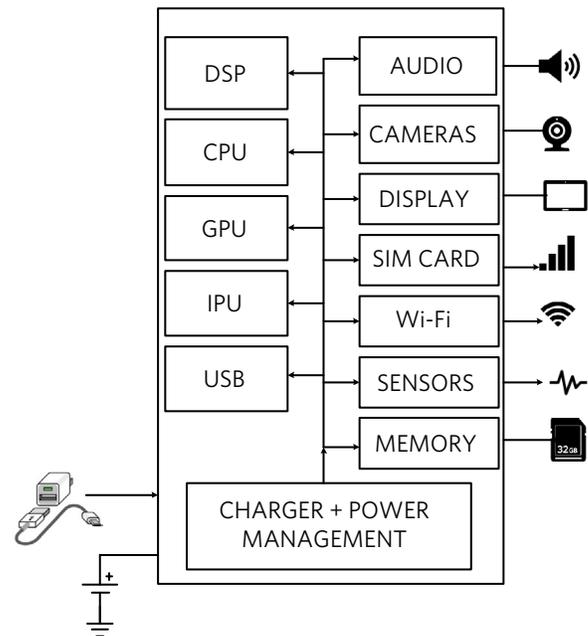

Figure 2. VR Headset Block Diagram

The VR system requires an optimized power management solution to support data processing, communication and sensor functions. The load profiles are dynamic and trend towards lower output voltages, which tightens the load-transient droop requirements. Since the processors are located on devices wrapped around the entire person's head, lower heat dissipation solutions drive power management ICs selection.

Typical AP Power Management Solution

Figure 3 shows a typical VR power management solution along with several auxiliary functions required for successfully running the system. Multiple voltage rails power the CPU, memory, and other necessary functions. A real-time clock (RTC) and a 32kHz highly accurate crystal oscillator (XTAL) enable precise timekeeping. The GPIO expander increases the flexibility of the turn-on and turn-off features, modules, and sensors.

Implementing this complex feature set with discrete ICs can be very challenging on multiple fronts:

1. AP systems require a glitch-free power-up sequence for successful bootup over corner conditions of voltage and temperature. Systems end up overdesigned and bulky.

2. If system or regulator faults are encountered during normal operation, the processor must be alerted to determine the next steps. The priority and sequence of this detection is critical.

3. The resulting large solution footprint and long PCB traces adversely affect regulator efficiency, reducing the runtime of the device and increasing the heat dissipation in the system.

4. Discrete system solution increase component count on the board and are prone to higher failure rates due to assembly issues and inferior signal integrity.

5. Having many ICs in a discrete solution congests the I²C bus and increases delay before the processor can read critical information.
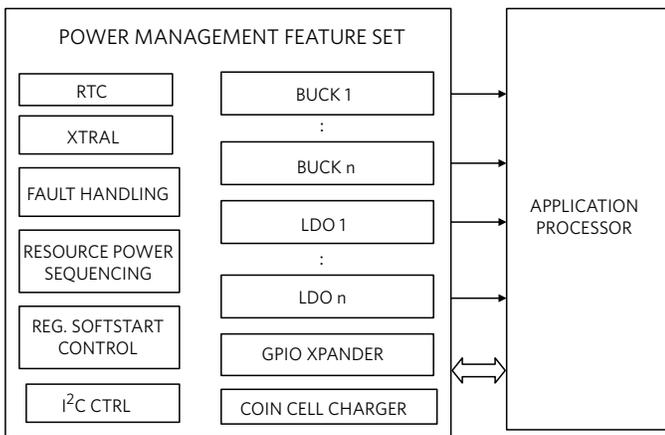

Figure 3. Typical AP Power Management

Integrated Solution

A fully integrated solution can overcome the challenges designers face with a discrete power solution. Figure 4 demonstrates how a single, integrated PMIC powers an AP, reducing PCB size, weight, and volume without compromising performance.

MAX77714 is a complete power management IC for portable devices using system-on-chip (SoC) application processors. Two high-current buck regulators (SD0 and SD1) are optimized for the AP's CPU and GPU rails and feature dynamic voltage scaling (DVS) on the output voltage, which ranges from 0.26V to 1.52V. The output stage $R_{DS(ON)}$ is optimized for superior efficiency as shown in the competitive analysis of Figure 5.

These regulators also support a forced pulse-width modulation control technique to minimize ripple under low-load conditions. Another two buck regulators (SD2 and SD3) are more general purpose with a wider output range. All four switching regulators have internal compensation, minimizing the need for external components.
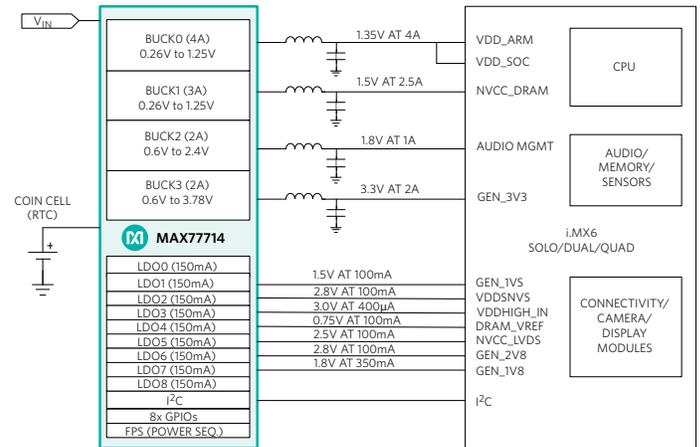

Figure 4. Fully Integrated AP Power Management

This PMIC also has nine highly configurable integrated low-dropout (LDO) linear regulators with current capabilities from 150mA to 450mA for noise sensitive rails in the system. All the LDOs feature two soft-start rates to limit inrush current during startup and support a wide output voltage range. 8x GPIO pins can be configured for alternate mode operation. 4x GPIO pins can be assigned to flexible power sequencing (FPS). 3x GPIO pins can be configured to output 32kHz clock for synchronizing external systems. The 8th GPIO pin can be configured as a system wake-up pin. The real-time clock with an external crystal oscillator provides timekeeping and alarm wake-up functions. If this feature is not used, then an optional, internal silicon oscillator can be used to save BOM cost. A robust on/off controller state machine drives the FPS for power-up/down, fault handling, and power mode control with minimum intervention from the AP. In addition, a watchdog timer is integrated for system monitoring purposes to help overcome AP operation hang-up states.

The PMIC is housed in a 70-bump, 4.1mm x 3.25mm x 0.7mm, 0.4mm pitch wafer-level package (WLP), ideal for space-constrained applications. This, together with high-frequency operation for small passives, yields a PCB area of only 230mm² (Figure 6).

DC-DC EFFICIENCY
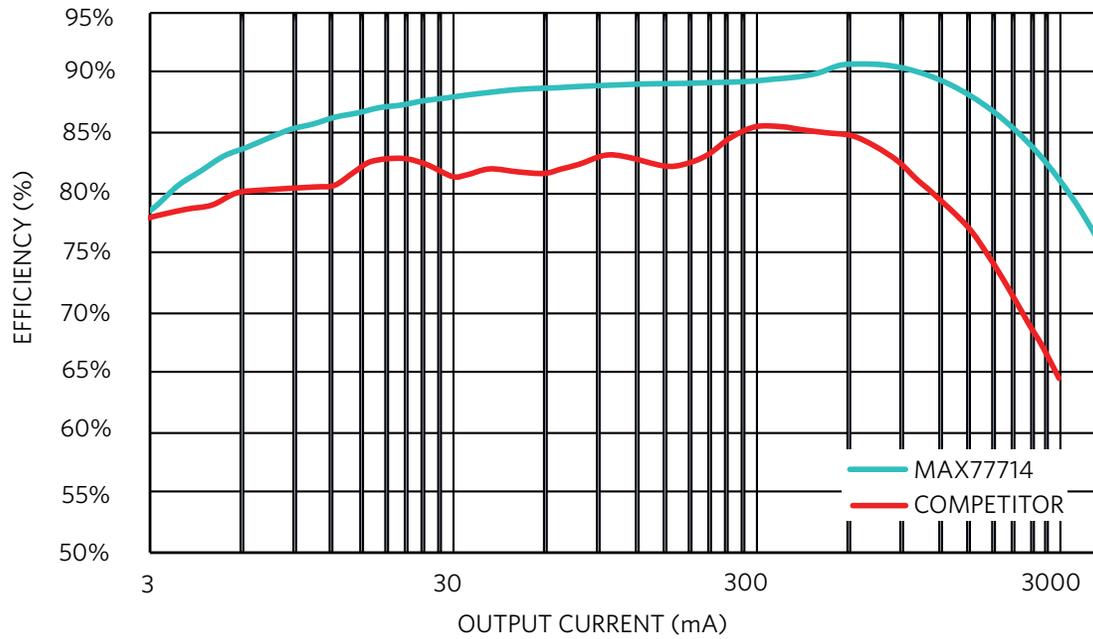### (3.6V$_{IN}$, 0.9V$_{OUT}$)

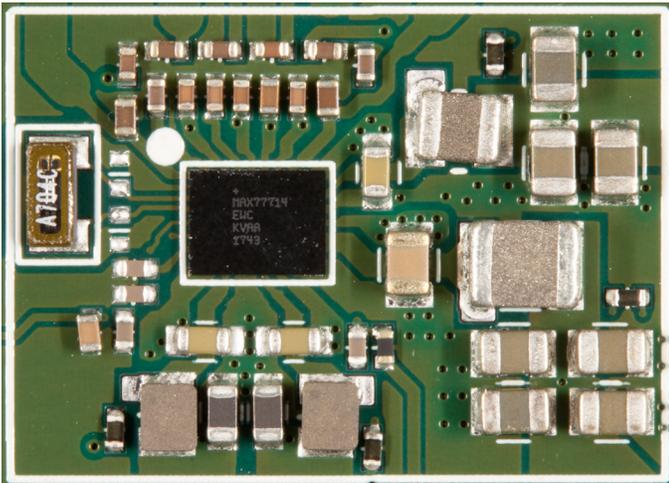
Figure 5. Efficiency Advantage

Figure 6. PCB 230mm^2 (Blank Space Not Subtracted)

The PMIC has multiple configuration registers which can be customized over I^{2}C to be tailored for many applications.

Conclusion

Powering the APs in virtual reality applications presents several design challenges related to flexibility, efficiency, and size. With its high flexibility and high level of integration, a fully integrated PMIC is a good fit for a wide range of space-constrained application processors. Low R$_{DS(ON)}$ integrated FETs yield superior efficiency while high-frequency operation minimizes passives size, further reducing PCB size and cost.

Learn more:

MAX77714 Complete System PMIC, Featuring 13 Regulators, 8 GPIOs, RTC, and Flexible Power Sequencing for Multicore Applications

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