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Returning to the Office with Power Over Ethernet 2

Christopher Gobok, Product Marketing Director

Introduction

IEEE's latest Power over Ethernet (PoE) standard, also known as PoE 2 or 802.3bt (and formerly known as PoE++), just turned 3 years old, but its application is still growing stronger than ever. Despite an increase in remote work due to the coronavirus disease 2019 (COVID-19), the number of powered Ethernet ports deployed each year continues to increase. Employers have been taking advantage of empty desks and upgrading IT infrastructure to future-proof workplaces with the hope that they will eventually return to full occupancy. Creating a smart office involves equipping the office space with multiple IoT devices that are connected to the internet, including meeting room signage, teleconferencing equipment, and various sensors. The benefits of a smart office include energy savings, streamlined business operations, and, perhaps most importantly, increased workplace safety for employees. COVID-19 has only accelerated the need for well-controlled building heating, ventilation, and air conditioning (HVAC) systems and numerous contactless communal items, forcing facility and IT managers to collaborate and deploy PoE-enabled systems. According to the 650 Group market research company, the number of switch/PoE ports shipped in the world is expected to exceed 150 million in 2025.

When PoE 2 was ratified in 2018, it delivered up to 71.3 W to the powered device (PD), nearly tripling the previous standard's 25.5 W. PoE 2 allows power to be sent over the same cabling with gigabit Ethernet, laying the groundwork for many of yesterday's, today's and tomorrow's power and data-hungry applications, including the remote temperature monitoring systems and thermal cameras that are used to screen personnel for COVID-19 at entrances before they enter the work site.

Figure 1 shows a basic PoE block diagram, with a single PD connected to power sourcing equipment (PSE). In past generations of PoE, a single power channel was sufficient to power each PoE port. Fast forward to 802.3bt now, where two power channels per port are required for medium and high power levels, with higher power density per channel to also consider. The global Ethernet market has seen an ever-increasing penetration of PoE-enabled ports. All of these factors have led to a need for IT departments to deploy vast numbers of high power density, high port count systems, all while demanding five nines uptime (99.999%) and reliability. A truly scalable PoE subsystem to ease deployment of high port count, PoE enabled switches has been long overdue.

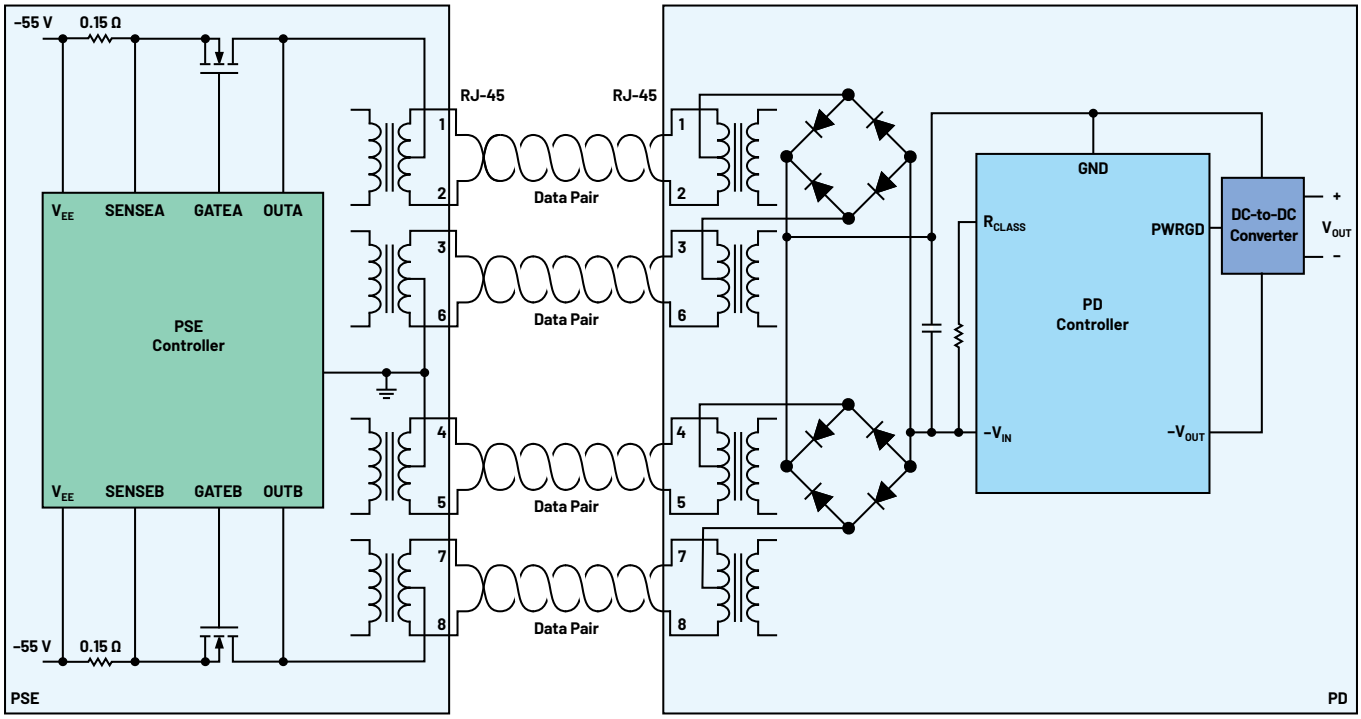

Figure 1. Power over Ethernet block diagram.

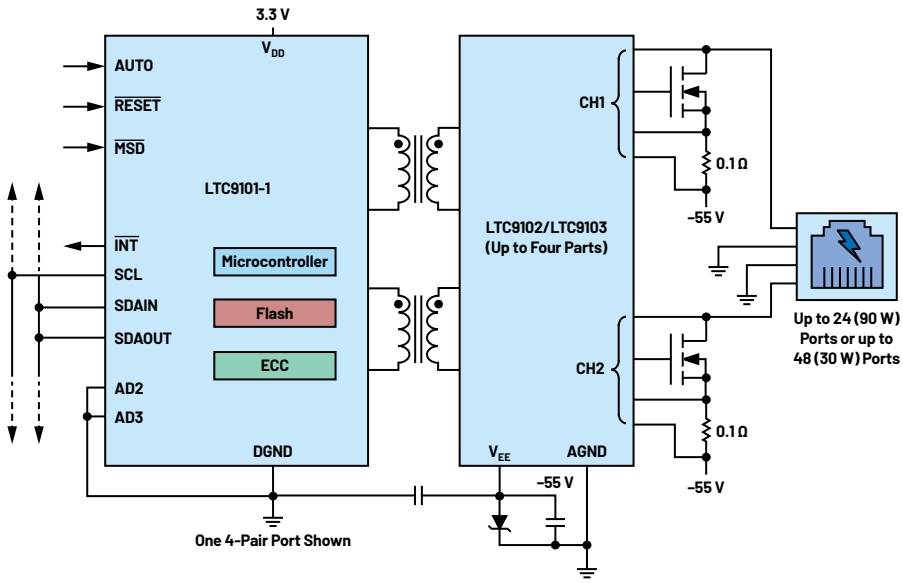

Figure 2. Simplified schematic of the LTC9101/LTC9102/LTC9103 PoE 2 24-port PSE chipset.

As the pioneer of PoE, a member of the IEEE 802.3bt Task Force, and an active participant of the Ethernet Alliance, Analog Devices has a long history of being the premier PSE and PD controller supplier in the industry, contributing to the hundreds of millions of ports deployed in the field today. The just-released ADI LTC9101, LTC9102, and LTC9103 high port count PSE chipset and any of ADI's PoE 2 PD controllers enable developers to offer a complete end-to-end PoE 2 system. Let's take a closer look at what makes this new platform special in today's market.

A Platform-Based Approach to PSE Design

Modern switches are highly complex systems that are commonly exposed to harsh environmental conditions, including surge and cable discharge events, and must deliver high system reliability and uptime. Past approaches to PSE architecture have viewed PSE subsystem design at the component level, focusing on incremental component improvements that did not necessarily optimize collective system performance. Viewing the PSE subsystem at a higher level forced design teams at ADI to rethink the PSE paradigm and to deliver system-level solutions. The LTC9101/LTC9102/LTC9103 and future derivatives will take this system-level approach, combining digital and analog components holistically to solve the PSE challenges facing system integrators, including those listed in Table 1.

Table 1. PSE System-Level Challenges and Solutions

Systems Integrator Challenge	ADI Solution
Surge and cable discharge	Robust port facing pins
System-level isolation requirements	Integrated isolation comms channel
LED lighting support	Dedicated, per-port detect/class resources
802.3bt complexity and standards changes	Custom digital controller with flash memory
Mixed port designs	Software configurable architecture
Diversity of register interfaces	Platform flexibility (coming soon)
Thermal efficiency	Industry lowest power path resistance
Power delivery efficiency	802.3bt-compliant Autoclass

The LTC9101/LTC9102/LTC9103 are part of a self-isolating PSE controller chipset specifically designed from the substrate up for PoE 2 systems. Figure 2 shows a simplified schematic and how one of up to 48 Ethernet ports is powered. The most novel feature of the chipset is its integrated isolation. Hence the chipset architecture, where the LTC9101 provides an isolated digital interface to the PSE host, while multiple LTC9102s and/or LTC9103s provide the high voltage analog Ethernet interface. 802.3 Ethernet specifications require that network segments, including PoE circuitry, be electrically isolated from the chassis ground and the PHY. By placing the LTC9101 on the nonisolated side and the LTC9102 or LTC9103 on the isolated side, up to six expensive optocouplers and an isolated supply are replaced with a single cheaper and more reliable 10/100 Ethernet transformer. This topology results not only in cost savings, but also in a more robust and manufacturable PSE design.

This scalable solution enables the flexible implementation of large PSE systems, anywhere from 4 to 48 ports, depending on how much power is needed for each port. Each design requires at least one LTC9101 digital controller and one or more LTC9102/LTC9103 analog controllers.

- The LTC9102 offers 12 power channels, where each channel energizes two of four pairs of wires in the Ethernet cable, to power anything from twelve 30 W ports (using one power channel per port) to six 90 W ports (using two power channels per port).
- Similarly, the LTC9103 offers eight power channels that can be used to power anything from eight 30 W ports to four 90 W ports.
- A single LTC9101 can manage up to four LTC9102s and/or LTC9103s that can be mixed and matched. For example, one LTC9101, one LTC9102s, and two LTC9103s could be used to implement a 24-port PSE with four 90 W ports and twenty 30 W ports, as shown in Figure 3.

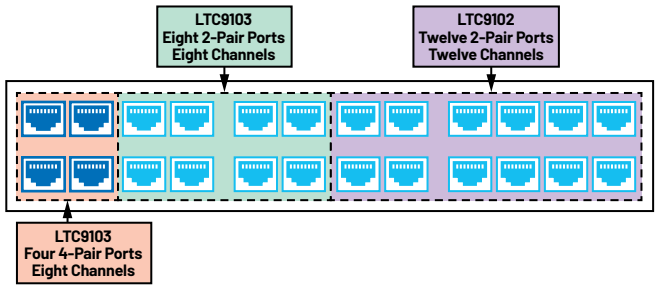

Figure 3. An LTC9102/LTC9103 mix-and-match implementation example: 24-port PSE with four 90 W ports and twenty 30 W ports.

IT and facility managers alike will appreciate the sixth-generation digital features of the LTC9101, including internal eFlash for storage of firmware updates and custom user configura¬tion packages, backward-compatibility with the LTC4291 4-port PoE 2 PSE drivers, and an I²C serial interface. The LTC9101's field-upgradeable firmware images are stored in a dedicated flash partition, where a fully compliant IEEE 802.3at/bt firmware image is preconfigured. Two complete copies of the firmware image are maintained under separate ECC and CRC protections for maximum data protection. After successfully booting up the chipset, users can configure and communicate with the chipset through the LTC9101's I²C interface, where each port can be independently configured to one of four PSE operating modes (auto, semi-auto, manual, or shutdown) and telemetry readings of port current, PoE supply voltage, and port power can be used to manage system power.

While the LTC9101 is the brains of the chipset, the LTC9102/LTC9103 are the brawn that offers high efficiency and ruggedness to the high voltage power path in multiple ways. Each LTC9102/LTC9103 power channel is implemented with dedicated detection and classification hardware. This allows all ports to detect, classify, and power on simultaneously, which drastically reduces the power-on latency across a switch. Other less advanced PSEs are subject to visible delays as PDs; for example, LED lights power on a serial port-by-port basis. The LTC9102/LTC9103 control each power channel using an external MOSFET, allowing users to select low $R_{DS(ON)}$ components, reduce power dissipation, and decouple channel failures. The use of 0.1 Ω sense resistors further helps to reduce power dissipation.

During overcurrent faults or when ports short circuit, the LTC9102/LTC9103 quickly remove power in ~1 µs to protect the PSE, MOSFET, and downstream circuitry. In addition, all port-facing pins can tolerate voltage transient events up to +80 V or down to –20 V without damage. Perhaps most impressive is the chipset's ability to operate through over ±6.5 kV of surge with minimal external components as tested per the IEC 61000-4-5 surge immunity specification (the DC3160 demo board showcases this feature). After any fault, the LTC9102/LTC9103 quickly turn the MOSFET back on in a safe, current-limited manner while minimizing disruption to the PD, which is critical for maximizing network uptime.

PoE 2 Topologies, Detection Schemes, and Power Classes

PoE 2 introduced two different PD signature configurations, single- and dual-signature PDs. A single-signature PD (Figure 4) is a PoE 2 PD that shares the same detection signature and classification signature between both pairsets. A dual-signature PD is a PoE 2 PD with an independent signature on each pairset, allowing each pairset to have fully independent classification and power allocations. Dual-signature PDs are complex solutions costing twice as much as a single-signature PD. It is worth noting that 802.3bt dual-signature PDs are not equivalent to prestandard UPoE devices, despite sharing a common architecture. The LTC9101/LTC9102/LTC9103 support a robust PoE 2 PD detection process that incorporates the new connection check subprocedure to determine which PD signature configuration is attached to the PSE.

In addition to performing a connection check, devices also verify the connected PD is a legal IEEE-compliant PD. While IEEE requires PSEs to detect valid PD signatures (25 kΩ) using either a 2-point voltage or 2-point current detection scheme, the LTC9101/LTC9102/LTC9103 implement a more robust scheme by employing both types of detection schemes. This multipoint (multiple voltages and multiple currents) detection scheme is used to eliminate false positives and avoid damaging network devices that were not designed to tolerate PoE DC voltages.

PoE 2 energizes two pairs of conductors (four wires) to deliver power up to 25.5 W and four pairs of conductors (eight wires) to deliver power up to 71.3 W. Not only are higher power levels enabled, but the use of more conductors provides better efficiency for the older, lower power levels because, with all conductors powered, the power loss in the cable is cut in half. Take, for example, a PoE 1 (PoE+) PSE supplying 30 W to ensure a PoE 1 PD will receive 25.5 W, where 4.5 W is lost over 100 m of CAT5e cable. Four-pair powering the same 25.5 W PD with PoE 2 would reduce the loss to less than 2.25 W, increasing the power delivery efficiency from 85% to 92.5%. When you consider the number of PoE PDs in the world, this translates to a very large reduction in power and, in many use cases, up to a 7.5% lower carbon footprint.

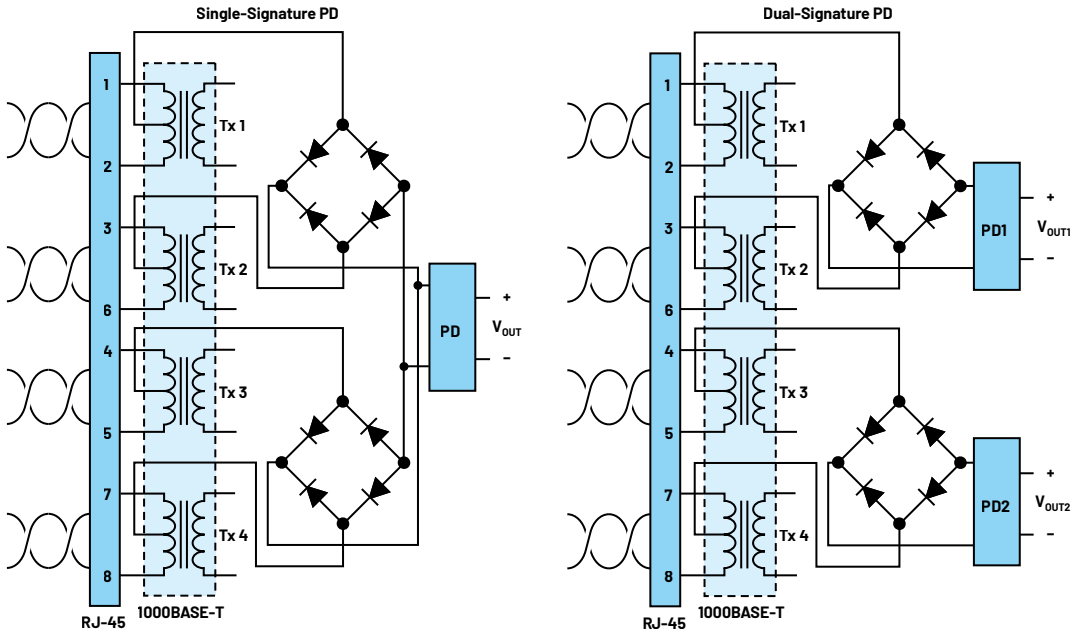

Figure 4. Single-signature vs. dual-signature PD topologies.

PoE 2 introduced four new high power PD classes, bringing the total number of single-signature classes to nine as shown in Table 2. Classes 5 through 8 are new to PoE 2 and translate to PD power levels ranging from 40 W to 71.3 W. PSEs still have their choice of using the physical layer (that is, 5-event classification for 71.3 W) or data link layer (that is, link layer discovery protocol, LLDP) to classify PDs, and PDs still must be able to support both classification schemes to be compliant. Remember, because each pairset operates independently in a dual-signature PD, each pairset can be a different class. For example, a Class 1 (3.84 W) on the first pairset and a Class 2 (6.49 W) on the second pairset would make for a dual-signature Class 1 and Class 2 (10.3 W) PD.

Table 2. PoE 2 PD Classes and Power Levels

Single-Signature PDs		Dual-Signature PDs	
Class	PD Power Available	Class	Pairset PD Power Available
0	13 W		
1	3.84 W	1	3.84 W
2	6.49 W	2	6.49 W
3	13 W	3	13 W
4	25.5 W	4	25.5 W
5	40 W	5	35.5 W
6	51 W		
7	62 W		
8	71 W		

PoE 2 PDs may also implement an optional extension of physical layer classification, known as Autoclass, where a PoE 2 PSE like the LTC9101/LTC9102/LTC9103 chipset measures the actual maximum power draw of a connected PD. By doing so, this handy power management feature allows for the allocation of "leftover" power to other light bulbs if they measure a particular bulb, due to lower brightness settings or a shorter cable, drawing less than its class power.

It goes without saying that PoE 2 is backward compatible with the older 25.5 W and 13 W PoE 1 standards. A lower power PoE 1 PD can connect to a higher power PoE 2 PSE without any issues. And, when the tables are turned and a higher power PoE 2 PD is connected to a lower power PoE 1 PSE, the PD can operate in the negotiated lower power state—this is referred to as demotion. If a PD ignores demotion and operates at its highest power state, the power-hungry PD will cause the PSE to repeatedly turn on, hit its overcurrent, then turn off—in effect, motor boating the PSE. For this reason, demotion is required by both PoE 1 and PoE 2 PDs, but is unfortunately overlooked in some implementations.

The Most Efficient PD

ADI offers a number of unique ICs, including those designed by Maxim Integrated (now part of ADI), to maximize PoE 2 PD performance. Figure 3 shows a simplified block diagram of a high efficiency single-signature PoE 2 PD interface with an auxiliary input. This solution provides an end-to-end (RJ-45 input to PD load) efficiency of greater than 94% and operates within the –40°C to +125°C temperature range.

The LT4321, shown at the RJ-45 interface in Figure 5, is an active diode bridge controller that replaces the required diode bridge rectifiers. The LT4321 uses low loss N-channel MOSFET bridges to simultaneously increase the PD's available power and reduce heat dissipation. PoE 2 requires PDs to accept DC supply voltages of any polarity over their Ethernet inputs, so the LT4321 smoothly rectifies and combines power from both data pairs into a single, polarity-correct supply output. Overall circuit size and cost are reduced as the enhanced power efficiency practically eliminates heat sinking requirements, and power savings of 10× or more enable PDs to stay within classification power budgets or add additional functionality.

The ideal diode bridge controller shown in Figure 5 is the brains of the PD interface—the LT4295 is a PoE 2 PD interface controller that integrates a high efficiency forward or no-opto flyback controller. The LT4295 supports all nine IEEE PD classes with an integrated 25 kΩ signature resistor, up to 5-event classification, and a single-signature topology. Aside from providing more PD power, what gives the LT4295 an edge over traditional PD controllers is its use of an external power MOSFET to, again, drastically reduce overall PD heat dissipation and maximize power efficiency, which becomes more important at PoE 2's higher power levels.

For those PoE 2 PD designs that need to be able to support an auxiliary supply, where the PD can be optionally powered by a power adapter, the LT4320, shown at the top of Figure 3, is a 9 V to 72 V active diode bridge controller that replaces each of the four diodes in a full-wave bridge rectifier with a low loss N-channel MOSFET to significantly reduce the power dissipation and increase available voltage. Power supply and wall wart sizes can be reduced as the enhanced power efficiency eliminates bulky and costly heat sinks. Low voltage applications can also benefit from the extra margin afforded by saving almost two full diode drops (~1.2 V, which is 10% at 12 V) inherent in hot-running diode bridges, increasing the application headroom.

Conclusion

PoE 2 continues to be very relevant in today's growing global Ethernet market, even amidst the ongoing preponderance of remote work. Small, medium, and large businesses that are retrofitting buildings with PoE-enabled scanners, cameras, and other systems to safeguard employees need high port count PSEs more than ever before. ADI's LTC9101/LTC9102/LTC9103 PoE 2 PSE chipset answers the call by enabling switch vendors to efficiently and reliably power up to 48 Ethernet ports, while equipping facility and IT managers with advanced power management capabilities. Meanwhile, at the other end of the cable, PD developers continue to have multiple ADI ICs at their disposal to increase integration, reduce heat, and increase power efficiency.

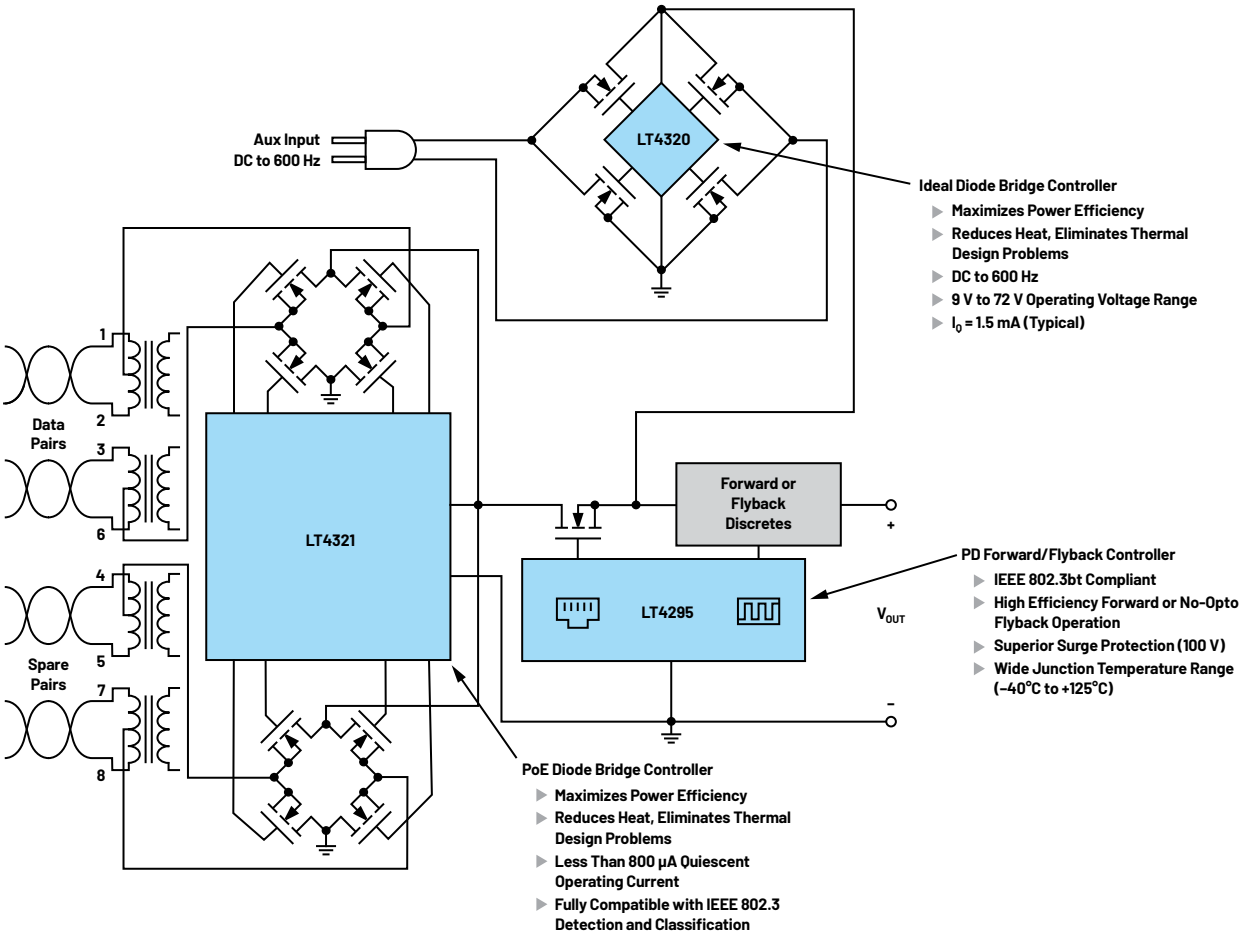

Figure 5. A simplified block diagram of a high efficiency IEEE 802.3bt single-signature PD interface with auxiliary input.

About the Author

Christopher Gobok is a product marketing director for power systems management products at Analog Devices. Chris graduated from San Jose State University with a B.S.E.E., an M.S.E.E., and an M.B.A. His previous industry experience includes working as a PME with optoelectronics and power MOSFETs. He can be reached at christopher.gobok@analog.com.