TECHNICAL ARTICLE



Robert Brennan

Senior Applications

Analog Devices, Inc.

Engineer,

WIDEBAND PHASE-LOCKED LOOPS WITH INTEGRATED VOLTAGE CONTROLLED OSCILLATORS: CAN THEY REPLACE A DISCRETE SOLUTION?

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In virtually every RF and microwave system, a frequency synthesizer is required. The frequency synthesizer creates the local oscillator signal that drives mixers, modulators, demodulators, and many other RF and microwave components. One way of creating a synthesizer, often considered the *heartbeat* of the system, is using a phase-locked loop (PLL) frequency synthesizer.

Traditionally, a simple PLL divided down the voltage controlled oscillator (VCO) output frequency, compared this to a reference signal, and then tweaked the VCO control voltage to tweak its output frequency. For many years, the PLL and VCO have been two separate chips—a discrete solution. The VCO creates the actual output signals; the PLL monitors the output signals and tunes the VCO to lock it relative to a known reference signal.

There are a number of strengths to the discrete solution:

- Each discrete chip can be designed to give its best possible performance.
- The physical distance between the PLL and the VCO reduces cross-coupling effects and minimizes unwanted spurious signals on the output.
- If one chip in the loop is damaged, fewer components need to be replaced.

Discrete solutions dominated the synthesizer industry for a long time but there were also downsides. One major issue is that the discrete solution requires a lot of board space to hold the two chips and all their supporting components. This results in larger end products and a higher cost.

Another major issue with the discrete solution is that traditional VCOs have a narrow output frequency range. A typical VCO bandwidth is 50 MHz to 500 MHz; it's possible to go up around 2 GHz but this requires an op amp-based active filter. This is a major challenge for anyone who wants to implement a system with a wider frequency range. To create a wider frequency range synthesizer, multiple PLLs, VCOs, supporting components, filtering, switches, and power supplies are needed! This exponentially increases the board space and cost of a design. Not only do discrete solutions impact the board design, there is also a huge amount of overhead work in qualifying, creating software for, and inventory controlling each device.

About 10 years ago, there was a breakthrough in the PLL-based synthesizer industry. The first integrated PLL and VCOs (PLL/VCOs) started to appear on the market. This major development meant boards could be smaller, costs could be lower, and the overhead could be dramatically reduced. The integrated solution also meant the VCO architecture could change to create a wideband synthesizer from one component. Let's explore the VCO architecture and how the shift to integrated VCOs opened doors in synthesizer performance.

Traditional VCOs are simple devices—voltage is applied to a tuning pin on the VCO and a certain frequency is output; the voltage is increased and the output frequency increases; the voltage is decreased and the output frequency is decreased. Figure 1 shows an example of the tuning voltage vs. output frequency of a GaAs MMIC VCO—the 13 V tuning range would require an active filter or a PLL with a high voltage charge pump.



Figure 1. Traditional VCO-tuning voltage vs. output frequency.

The integrated PLL/VCO solution uses a different type of VCO architecture that builds on the traditional architecture. The integrated PLL/VCO effectively combines several traditional VCOs side-by-side to create a VCO with a remarkably wide bandwidth. Each individual VCO—created by switching capacitors in and out—are called bands. The fact that the PLL and VCO are integrated onto one chip makes the multiband architecture possible. Every time the user wants to lock to a new frequency, the device initiates a VCO calibration process where the chip quickly sorts through the VCO bands and chooses the optimum one for the required output frequency. Once the VCO band has been selected, the PLL then locks the loop and keeps the output at the desired frequency.

The first generation of these PLL/VCO chips had over 4 GHz of bandwidth! Compare that to the discrete 100 MHz to 300 MHz bandwidth—and this frequency range was possible from a tiny chip relative to the previously required banks of PLLs, VCOs, filters, and switches. Figure 2 shows the tuning voltage vs. output frequency of a multiband PLL/VCO. In this example, the fundamental VCO output range was specified as 2200 MHz to 4400 MHz. This was complemented with a bank of dividers after the VCO output, but internal to the chip, which could divide the signal to as low as 35 MHz; hence the >4 GHz bandwidth—all from one 5 mm \times 5 mm package.



Figure 2. Multiband VCO-tuning voltage vs. output frequency.

While this breakthrough technology was a huge step forward in frequency range, board space, cost, and overhead, there were still drawbacks that stopped the integrated solution completely taking over from the discrete solution. In many applications, the most important performance specification (after frequency range) is phase noise.

Why is phase noise so important? Imagine a system where a signal is transmitted over clear air. Say the signal-to-noise ratio of the transmitted signal is 50 dB at the transmitting antenna. That means, the signal the receiver is supposed to receive is 50 dB more powerful than the noise on either side of the transmitted signal; that is, at nearby higher and lower frequencies. Let's say this signal can travel 10 miles before the signal power is decayed into the noise and the transmission is lost. Now, suppose the phase noise of the synthesizer is improved by 3 dB. This means the signal-to-noise ratio of the transmitted signal is 53 dB. As a result, the transmitted signal power is twice that of the previous, 10 mile range signal, and can therefore travel further before it decays into the noise. Further distance means fewer repeaters/ transmitters are needed and costs can be reduced.

Beyond this communications example, there is an additional drive for phase noise performance from the electronic test and measurement community. Whatever phase noise performance is used by the communications industry, the electronic test and measurement instruments need better phase noise performance so they can measure the communications protocols.

While many solutions were able to move from discrete to integrated saving millions of dollars in the process—the phase noise performance of the first generationPLL/VCOs simply wasn't good enough to replace many of the low phase noise requirement applications. As well as the phase noise performance, the frequency range was still pretty low compared to many of the applications that require a discrete PLL and VCO.

The frequency range issue can be mitigated by frequency doublers and other multipliers, but these are power hungry and add additional cost and board space to the solution.

Fortunately, while these integrated solutions were being rolled out, development was already underway to move to new IC processes that allowed for the much sought after phase noise and frequency range improvements. So, at this point, the stage is set for the second generation of integrated PLL/VCOs. The requirements are:

- Output frequencies greater than 4.4 GHz.
- > Phase noise performance comparable with discrete solutions.
- An integrated PLL and VCO in a single, small package.
- Lower cost than discrete solutions.

Late 2014 saw the start of this second generation of integrated PLL/VCOs. Products started to appear on the market with greater than 10 GHz output frequency range, phase noise comparable to a discrete VCO, 5 mm \times 5 mm packages, and at lower prices than a similar discrete PLL and VCO solution (which would have a much narrower frequency range).

For example, the ADF4355 family from Analog Devices fulfilled all the requirements of this second generation:

- Output frequencies from 50 MHz to 13.6 GHz (≤6.8 GHz from one port, ≥6.8 GHz from another).
- Phase noise:
 - Traditional discrete VCO at 10 GHz: –110 dBc/Hz at 100 kHz offset and –135 dBc/Hz at 1 MHz offset. The discrete VCO trades off frequency range for phase noise performance.
 - ADF4355 family at 10 GHz: -106.5 dBc/Hz at 100 kHz offset and -130 dBc/Hz at 1 MHz offset.
- ▶ 5 mm × 5 mm LFCSP package.
- Prices vary across the family but lower cost than a discrete solution.

Now a user could have all the phase noise performance benefits of a discrete solution, plus all the other benefits of an integrated solution. As an added benefit, PLL technology had also developed over the years so this second generation of PLL/VCO device had an assortment of PLL performance enhancements too.

For the first generation of PLL/VCOs, the PLL blocks had maximum phase frequency detector (PFD) frequencies around 32 MHz and fractional-N divider resolutions of around 12 bits. This combination meant typical channel resolution was in the tens of kilohertz. The second generation of PLLs/VCOs have maximum PFD frequencies greater than 100 MHz and fractional-N divider resolutions of 25 bits or even up to 49 bits. This had two main benefits—the higher PFD frequency allowed for lower PLL phase noise (every doubling of PFD frequency means the N divider can be halved, so the N divider noise contribution drops by 3 dB); and 25 bit or even more resolution allows exact frequency generation and sub-Hz channel spacing.

Spurious Performance

There is an important aspect of the integrated PLL/VC0 that needs to be discussed. One of the benefits of the discrete solution listed above is that the physical isolation between the two chips reduces cross coupling between the PLL and VC0 and therefore reduces the power of unwanted spurious signals. When the PLL and VC0 are integrated, it is inevitable that the spurious performance will degrade. Some parts in the market managed to keep this degradation very low and have surprisingly good spurious performance for a PLL/VC0—for example, the HMC830. Other PLL/VC0 parts need extra applications work to improve the spurious levels for some high performance products.

Varying the PFD Frequency to Eliminate Integer Boundary Spurs

One technique is to vary the PFD frequency of the PLL using a frequency planning algorithm. This can move spurious signals, caused by the PFD block, to a region where they don't have a strong impact and are virtually eliminated. This is detailed in the article "Analyzing, Optimizing, and Eliminating Integer Boundary Spurs in Phase-Locked Loops with VCOs at up to 13.6 GHz."

Isolate the PLL and VCO

As mentioned above, the close proximity of the PLL and VCO circuits can result in unwanted coupling. To mitigate this, it is possible to use two chip solutions to physically separate the PLL and VCO circuits. This gives the discrete advantages of low spurious signals and the integrated advantages of a wide output frequency range.

The HMC704 from Analog Devices discrete fractional-N PLL portfolio is ideal for this task. In this solution, one of the VCO output signals (there are two outputs on all the ADF4355 family) is fed to the HMC704 (an optional 10 dB attenuator on this signal can help reduce spurious levels even further). The ADF4355 PLL is initially used to complete the VCO calibration and lock to the desired frequency. Then, the ADF4355 PLL section can be turned off, by tristating the charge pump and holding the counters in reset thus removing any spurs from the PLL, and the HMC704 will keep the loop locked. There are several benefits to this:

- Using a PLL in a different chip to the VCO reduces the spur power.
- The HMC704 inherently has better spur performance than the ADF4355 PLL—hence, the spurs are reduced even further.
- The HMC704 has a lower normalized phase noise floor than the ADF4355 PLL—hence the noise at the synthesizer output is lower.

To complete the loop, the HMC704 charge pump output is connected to a loop filter. The loop filter output must be connected to the ADF4355 VTUNE pin. When the loop is locked, the HMC704 is operating solely at the PLL and the ADF5355 is operating solely as the VCO. To completely remove spurs from the ADF4355 PLL, it is necessary to ground the ADF4355 reference input pin when the ADF4355 PLL is not in use. Fortunately, the HMC704 offers an easy way to do this. The HMC704 has a general-purpose output (GPO) pin—this pin can be connected directly to the ADF4355 reference input pin. When a reference signal is required by the ADF4355 (which it is for VCO calibration), the HMC704 can route its reference signal out to the GPO pin; when it's necessary to ground the ADF4355 reference input pin, the HMC704 can be programmed to output GND on the GPO pin. Figure 3 shows this circuit.



Figure 3. Locking the ADF4355 with an external HMC704 PLL to improve spurious performance.

Analog Devices has released four keys parts with this second generation PLL/VCO performance, the ADF4355 family. There are four devices in the family; three are very similar except for their frequency range and one is a low power variant.

- ADF4355-2: integrated PLL/VCO outputting 53 MHz to 4400 MHz.
- ADF4355: integrated PLL/VCO outputting 53 MHz to 6800 MHz.
- ADF5355: integrated PLL/VCO outputting 53 MHz to 13,600 MHz.
- ADF4355-3: low power integrated PLL/VCO outputting 51 MHz to 6600 MHz.

All parts are available on *analog.com* with data sheets, samples, evaluation boards, control software, simulation software, user guides, EngineerZone[®] online support community, and much more.

- www.analog.com/adf4355-2
- ▶ www.analog.com/adf4355
- www.analog.com/adf5355
- ▶ www.analog.com/adf4355-3

About the Author

Robert Brennan [*robert.brennan@analog.com*] joined Analog Devices in 2010 after graduating with a bachelor's degree in electrical engineering from the University of Limerick, Ireland. He worked at the Analog Devices Limerick office for several years before relocating to the U.S. He is currently an applications and marketing engineer in the RF and Microwave Group based in Massachusetts. His primary focus is on PLLs, VCOs, and integrated PLL/VCOs.

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Analog Devices, Inc. Worldwide Headquarters

Analog Devices, Inc. One Technology Way P.O. Box 9106 Norwood, MA 02062-9106 U.S.A. Tel: 781.329.4700 (800.262.5643, U.S.A. only) Fax: 781.461.3113

Analog Devices, Inc. Europe Headquarters

Analog Devices, Inc. Wilhelm-Wagenfeld-Str. 6 80807 Munich Germany Tel: 49.89.76903.0 Fax: 49.89.76903.157

Analog Devices, Inc. Japan Headquarters

Analog Devices, KK New Pier Takeshiba South Tower Building 1-16-1 Kaigan, Minato-ku, Tokyo, 105-6891 Japan Tel: 813.5402.8200 Fax: 813.5402.1064

Analog Devices, Inc. Asia Pacific Headquarters

Analog Devices 5F, Sandhill Plaza 2290 Zuchongzhi Road Zhangjiang Hi-Tech Park Pudong New District Shanghai, China 201203 Tel: 86.21.2320.8000 Fax: 86.21.2320.8222 ©2016 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners. Ahead of What's Possible is a trademark of Analog Devices. TA14281-0-4/16

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