**ADuM3220 4A Gate Driver for Synchronous DC/DC Conversion**

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This ADuM3220 was designed to be used as a 4A gate driver in an isolated system for synchronous DC/DC Conversion. Traditional solutions have used 2 isolators and a dual gate driver. As shown in Figure 1 A and Figure 1B, a dual gate driver IC can be mated with two pulse transformers or two optocoupler channels to provide a fairly large solution size. Given that power supply applications require large amounts of power in a small area, the ADuM3220 as shown in Figure 1C is a solution that is more than 50% smaller and is a more integrated solution for lower cost.

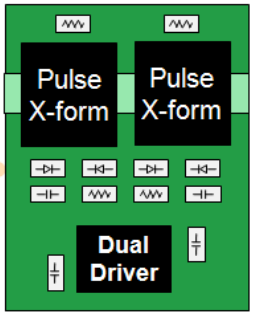


**Figure 1A**

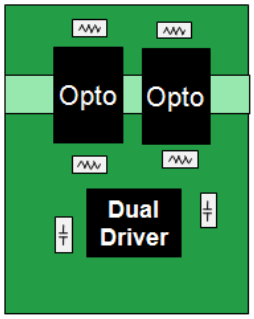


**Figure 1B**

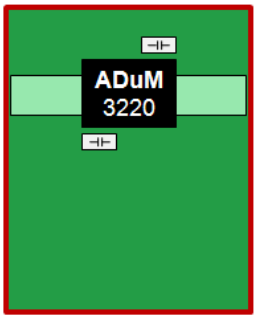


**Figure1C**

Synchronous rectification uses N-channel MOSFETs instead of diodes to reduce the conduction losses and increase efficiency in power supplies where many amperes of current are to be delivered. Implementing the synchronous DC/DC converter architecture requires synchronizing the switching of the secondary MOSFET switches with the primary MOSFET switches. Figure 2 illustrates the ADuM3220 application circuit for an isolated synchronous DC/DC converter with

unregulated output.

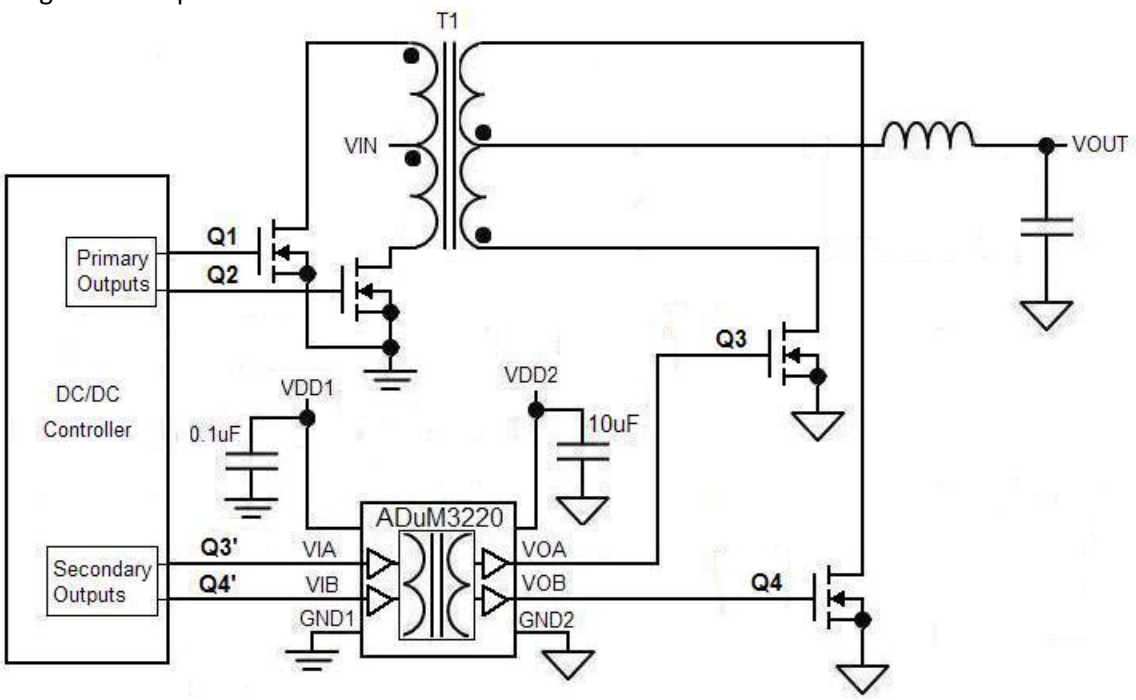


**Figure 2. ADuM3220 application schematic**

The DC/DC controller sends the PWM drive signals to the primary and secondary switches. Primary switches Q1 and Q2 are turned on in a push-pull action with a break before make timing to drive the 2 primary coils of the transformer T1, as shown in Figure 3 timing waveforms. The secondary coil of T1 needs to be switched in sync with the primary coils by switching on Q3 when turning on Q1, and turning on Q4 when turning on Q2. Note, Q3' and Q4' PWM waveforms, if they were shown, would be advanced in time by the known propagation delay of the ADuM3220 so that Q3 and Q4 appear in time as they should. The ADuM3220 has a typical propagation delay of only 45ns, which includes the digital isolator delay and the gate driver delay. By integrating the gate driver with the isolator, the specification of propagation delay is more precise, an advantage over discrete solutions.

ADuM3220 non-overlap signals of Q3, Q4 for unregulated applications

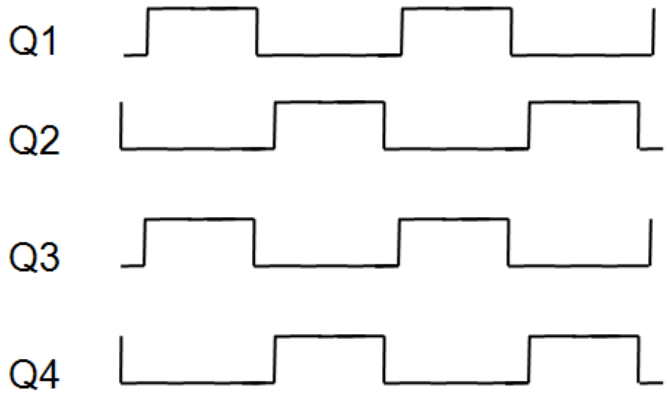

**Figure 3. ADuM3220 PWM timing waveforms**

When PWM switching is performed at a high frequency, the PWM control signals need very tight control. For example, when the PWM frequency is at the ADuM3220 maximum switching frequency of 1MHz and a duty cycle of 50% is used, the pulse width is at a minimum of 500ns. At this small pulse width, the matching between channels of the ADuM3220 needs to be very good to deliver precise switching. The ADuM3220 has a typical channel-to-channel matching of 1ns, with a maximum of 5ns over temperature. This precise matching between channels of the ADuM3220 helps to prevent cross conduction and to protect the MOSFETs from damage.

Next we will consider applications where an isolated feedback is used to tightly control the output voltage, and the duty cycle will not be a fixed 50%, but will vary to control the output voltage. In these applications, during the time that the primary switches are both off, it may be desired to allow the Q3 & Q4 switches to be on at the same time to prevent the body diodes of Q3 & Q4 from conducting, which would be less efficient. The application circuit that is shown in figure 4 would use a 4A gate driver that is just like the ADuM3220 but does not have the non-overlap control logic, allowing Q3 & Q4 to be on at the same time. Unlike the ADuM3220, the timing diagram for the gate driver with regulated output shown in figure 5 can allow the switches Q3 and Q4 to conduct when Q1 and Q2 are both off.

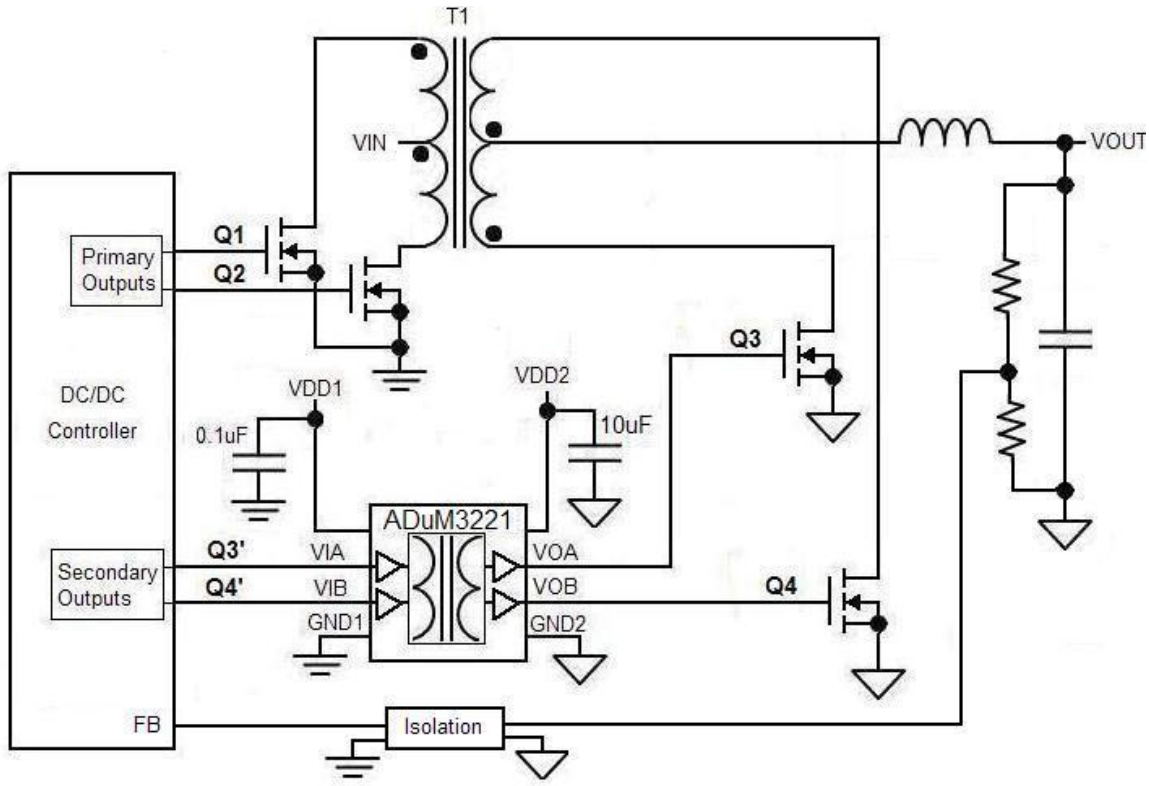


**Figure 4. Application schematic with regulated output**

Overlapping signals for Q3, Q4 for regulated applications

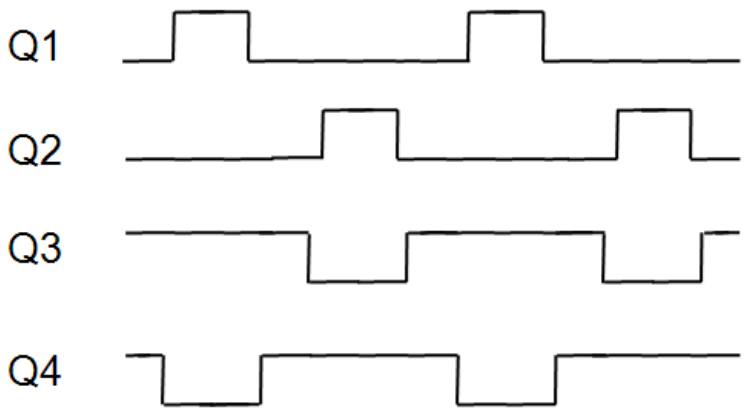


**Figure 5. PWM timing waveforms for regulated output**

In summary, for isolated synchronous DC/DC applications, the ADuM3220 has been shown to reduce the solution size by more than 50%, and provide much improved timing performance over solutions with separate isolators and gate drivers.