Teridian Smart Grid Solutions

78M6612
Hardware Design Guidelines

APPLICATION NOTE

AN_6612_007 **November 2011**

1 Introduction

This application note provides hardware and system design guidelines for those incorporating the 78M6612 system-on-chip (SoC) in their products. These guidelines will help hardware engineers to reduce design cycle times.

The following topics are discussed:

- Non-isolated Configuration
  - Safety Precautions
  - 3.3 VDC Supply (V3P3) and System Connection
  - Line Voltage Resistor Divider Selection
  - Shunt Selection and Connections
- Isolated Configuration
  - Current Transformers
  - Other Connections
  - Voltage Transformers
- Calibration Considerations
- Basic Configuration
  - Reset Circuitry
  - V2P5 Voltage Reference Pin
  - V1 Pin
  - In Circuit Emulator (ICE) Pins
  - Connecting 5 V Devices
  - Driving External Loads
  - Connecting I2C EEPROMs
  - Connecting 3-Wire EEPROMs
  - UART0 (TX/RX)
  - UART1 Interface
  - Power Supply Topologies
- Timing Reference
  - Oscillator Connections and Components Selection
  - PCB Layout Recommendations
  - Other Considerations

A Hardware Design Checklist is provided at the end of this document as a quick summary.

2 Non-isolated Configuration

When using a resistive shunt current sensor, the measurement IC and its power domain are not isolated from the AC mains. In this configuration, the 3.3 VDC supply rail (V3P3) for the 78M6612 must be directly connected to AC-Neutral for precision energy measurement. Isolation components, if required, are added in between the measurement IC and the rest of the system.

The V3P3 connection to AC-Neutral can be eliminated when using current transformers (CT) as the current sensing elements. Refer to the section on Isolated Connections for designing with CTs.

2.1 Safety Precautions

With V3P3 directly connected to NEUTRAL, the 78M6612's Ground signal is -3.3 V below earth ground. Therefore, any external test equipment attached to the 78M6612 will be subject to this -3.3 V ground reference disparity.

External test equipment **must** be floated from earth ground to avoid equipment damage due to this ground reference disparity.

An additional safety issue may arise due to mis-wiring of the AC outlets. If the LINE and NEUTRAL wire connections at the AC plug are reversed between the 78M6612 and the external test equipment, the 78M6612 and external test equipment will see a 120/240 VAC voltage difference rather than -3.3 V. This scenario can occur when the 78M6612 and external test equipment are powered from different wall outlets or power strips, one of which is mis-wired. With proper earth grounding, the external equipment is always referenced to earth ground via their enclosures.

Any systems communication interface (UART, SPI, I^2C) between the 78M6612 and external circuitry must be isolated to accommodate the -3.3 V disparity in their GND pins (or in the event of a LINE reversal).

Refer to the *78M6612 Safety Precautions* document.

2.2 3.3 VDC Supply (V3P3) and System Connection

The 78M6612 requires a single 3.3 VDC supply. The 3.3 VDC (V3P3) also represents the reference potential for the 78M6612. The basic connections for a shunt-based system are represented in Figure 1.

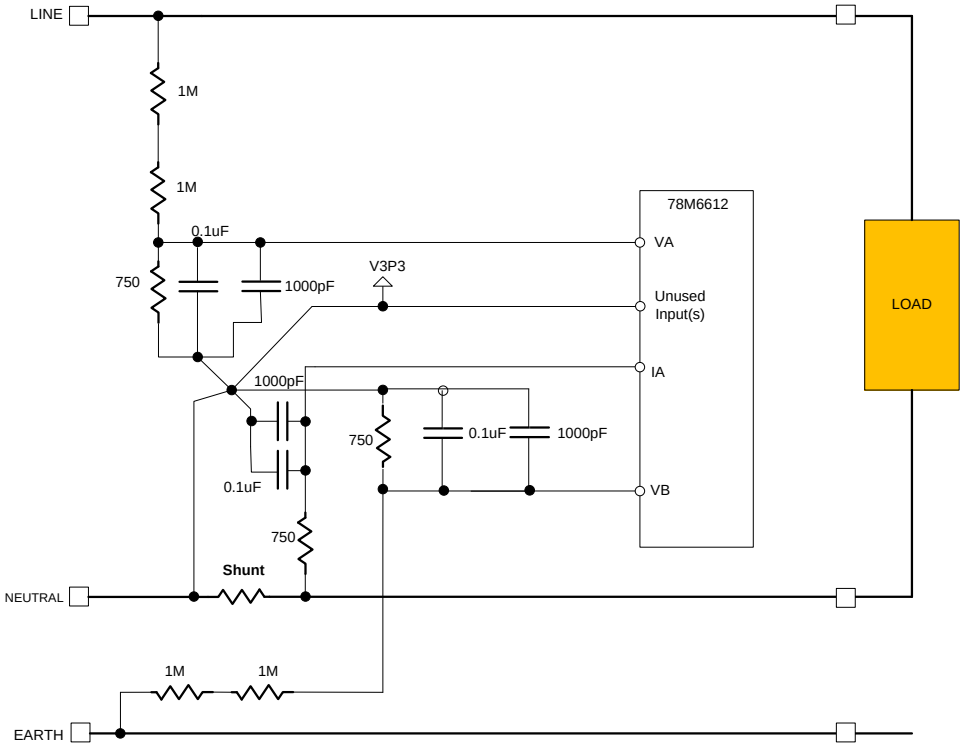


Figure 1: Basic Connection Diagram on Shunt-Based Systems

The analog inputs to the 78M6612 are used as follows:

- VA input is used to measure the line voltage.
- IA input is used to measure the load current.
- VB input is used to flag a Line/Neutral polarity reversal. If this feature is not desired, terminate A2 to V3P3 through a resistor-capacitor filter.
- IB is in this case not used. It is terminated to V3P3 through a resistor-capacitor filter.

Notes:

- The values used for the anti-aliasing filters are 750 Ω and 0.1 µF. The filters have in this case a cutoff frequency of about 2.1 kHz. Since the sample rate of the ADC converter may vary depending on the different firmware configurations, a different value may be required. To tune the filter, it is recommended to keep the 750 Ω resistor unchanged and modify the value of the capacitor.

Do not tie the ground of the 78M6612 directly to earth ground. See the Safety Precautions section.

Effective 3.3 VDC bypassing incorporates the combination of three different capacitor values. A 1000 pF in parallel with a 0.1 µF ceramic capacitor must be placed as close as possible to the 78M6612 V3P3A pin. Place the 1000 pF capacitor should be placed closest to the V3P3A pin of the 78M6612. An additional 22 µF bulk capacitor is placed in the vicinity of the V3P3SYS pin to provide decoupling for the external DIO circuitry. Connect the VBAT pin to the V3P3SYS pin or directly to V3P3. These three capacitor values provide decoupling over a wide frequency spectrum. Do not connect V3P3D to V3P3. V3P3D only requires a 0.1 µF capacitor to ground.

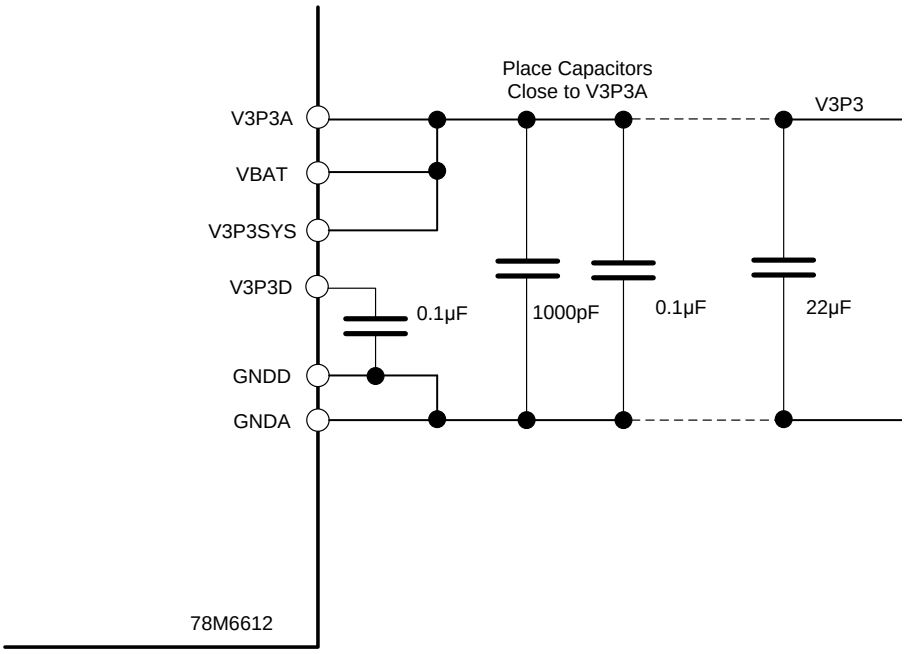


Figure 2: Power Supply Decoupling

2.3 Line Voltage Resistor Divider Selection

The input line voltage must be scaled to match the 78M6612's ADC input signal range of 176.78 mVrms. In the example of Figure 3, the line voltage is scaled as follows:

$$VA = \frac{VLINE * 750}{1M + 1M + 750} = VLINE * 3.7486E - 4$$

The use of two 1 MΩ resistors instead of a single 2 MΩ resistor is required to meet the maximum voltage rating of the resistor package and to provided adequate breakdown and arcing clearance. Typically 1206 series surface mount resistors are recommended.

An important aspect to consider is the accuracy of the resistors in the voltage ladder. Another consideration that can affect the overall measurement accuracy is the resistor temperature coefficient (TCR in Ωppm/°C).

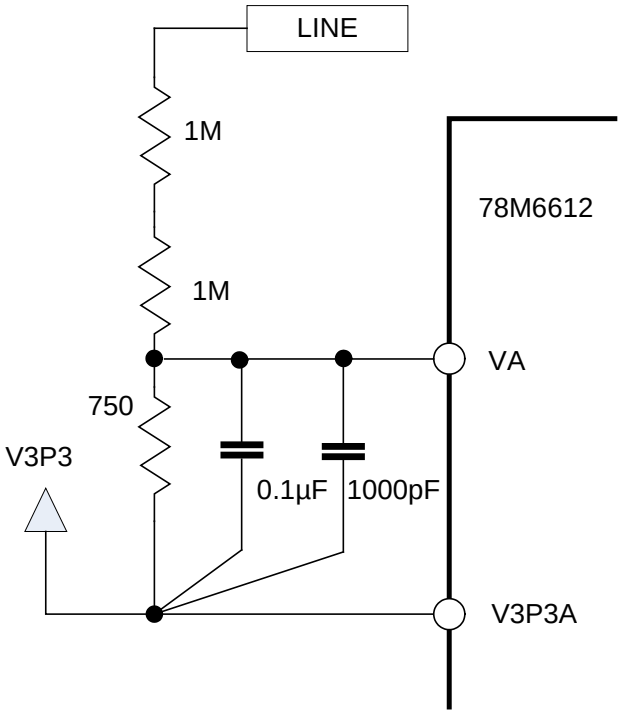


Figure 3: Input Voltage Divider and Filtering

Initial component tolerance can easily be compensated for during calibration. Depending on the system accuracy requirements, the incremental cost of a higher precision resistor (i. e. 0.1% versus 5%) may result in a lower production line calibration cost (shorter calibration time). If 0.1% tolerance resistors are used, a calibration would only need to be done on one system and then the voltage calibration coefficient obtained can be used for all others in production thus saving time through the production line. The variation from board to board would be within the tolerance of the resistors used in the divider.

Additionally, the higher precision resistor will have a smaller temperature coefficient. This eliminates the source of error that can arise from changes in resistance from self heating as the line voltage changes. TCR of 50 ppm/°C or lower (preferably 25 ppm/°C) is recommended.

2.4 Shunt Selection and Connections

The 78M6612 sensor input range is 12.5 µV (8.84 µVrms) to +250 mV (176.78 mVrms). The value of the shunt to be used is usually a tradeoff between a higher shunt value to utilize the full analog sensor input range of the IC and the power loss in the shunt.

Use the maximum rated load power when calculating the value of the shunt resistor for best utilization of the ADC's input range (±250 mVpp). Also, use the lowest operating LINE voltage (for example 90 VAC for 120 VAC rated systems) for this calculation. The maximum input current is then:

$$IInmax(rms) = \frac{PInmax}{VACIn\,min}$$

For example, if the maximum input power is 1.0 kW, the maximum input current is 11.12 A rms.

The resultant peak-to-peak current is calculated to be:

$$IInmax(pk-pk) = 2 * \sqrt{2} * IInmax(rms)$$

In the example above, the peak to peak value is 31.4 A.

$$Rshunt = \frac{Vmax}{IInmax} = \frac{176.78\,mVrms}{11.12\,Arms} = 15\,m\Omega$$

A 15 mΩ shunt value fully utilizes the ADC input range. This shunt value produces a dissipated power of 1.85 W at maximum load current. In order to ensure more ADC signal margin due to transients and to lower the power dissipation in the shunt resistor, a lower value shunt of 8 mΩ is recommended. In this case, the shunt's power dissipation reduces to 0.99 W at the maximum load current.

The next steps involved in the shunt resistor selection include considerations for power dissipation, initial tolerance and the device's temperature coefficient. In the case selected above, the power dissipated in the shunt at maximum load current is 0.99 W. A 2 W rated device package is recommended for good long-term reliability. The initial tolerance can be compensated during calibration. However, the temperature coefficient plays a role in the overall accuracy and cannot be easily compensated. For example, a temperature coefficient of 100 ppm/°C causes a resistance variation of 1% over the 100 °C operating temperature environment.

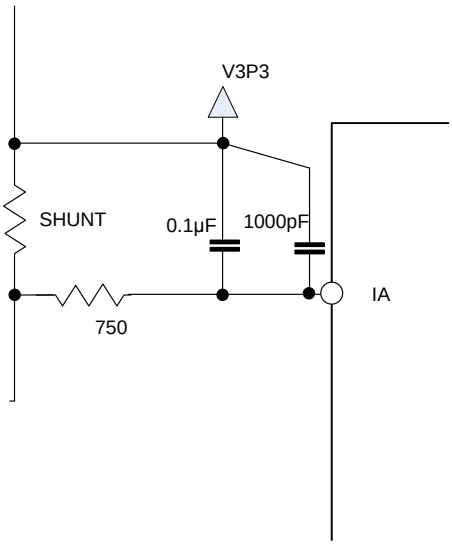


Figure 4: Shunt Connections and Filtering

3 Isolated Configuration

Alternatively, the 78M6612 can sense the load current using a current transformer (CT) for an isolated configuration. In this configuration, the 3.3 VDC supply rail (V3P3) for the 78M6612 is not directly tied to AC mains. The analog inputs to the 78M6612 are used as follows:

- The A0 and A2 inputs are used to measure the line voltage differentially.
- The A1-A3 inputs are used to measure the load currents.
- The IB input is not used and is tied to V3P3. It can be used to measure the load current to a second outlet and in this case would use similar topology as the IA input.

3.1 Current Transformers

The selection of a current transformer with respect for the desired measurement accuracy includes factors such as line frequency, measured current range and the CT's turns ratio. Also, subjecting a current transformer to load currents above the manufacturer's rated current specification may saturate the CT and cause winding failures due to excessive temperature rise. On the other hand, a current transformer that is rated much higher than the target load current might be restrictively too large and expensive for its purpose.

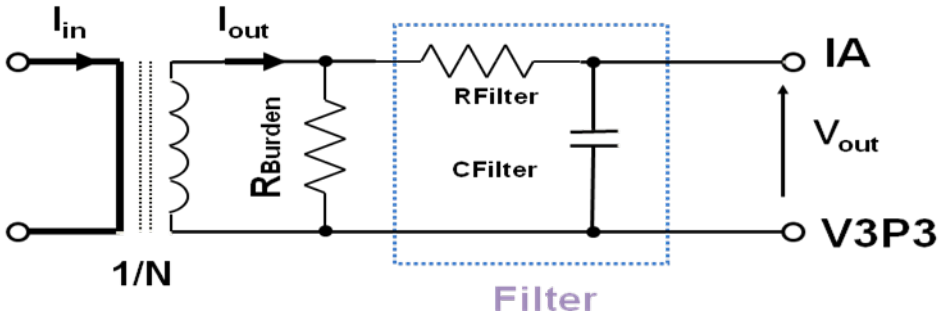


Figure 5: Current Transformer (CT) Basic Connections

Usually, current transformers have turns ratios ranging from 10:1 to 2500:1. The higher the turns ratio (TurnRatio = Nsecondary/Nprimary), the higher the resolution of the current measurement. A too high turns ratio increases distributed capacitance and leakage inductance. These characteristics may decrease the CT's accuracy and capability to operate at higher frequencies. However, if the number of turns is too low, the output signal may distort or "droop" (for positively sloped unipolar input signals). Such distortion may cause measurement inaccuracies. We recommend a minimum turns ratio of 1000:1.

The next step towards selecting a current transformer is the calculation of the burden resistor's value (RBurden). The 78M6612 signal input range is 176.78 mVrms (250 mVpk). Therefore, the CT's secondary output voltage (Vout) must operate within this range. Assuming the maximum load current is 20 A rms (28.284A pk), a 1000:1 ratio current transformer will produce a secondary current of 20 mA rms (28.284 mA pk). Per Figure 5, the burden resistor's value is calculated as follows:

$$RBurden = \frac{Vout}{Iout}$$

Using the values in the above example, the value of the burden resistor is:

$$RBurden = \frac{0.250}{0.028284} = 8.85\ \Omega$$

A standard value 8.2 Ω resistor is recommended.

Figure 6 shows a basic connection diagram of a CT-based system.

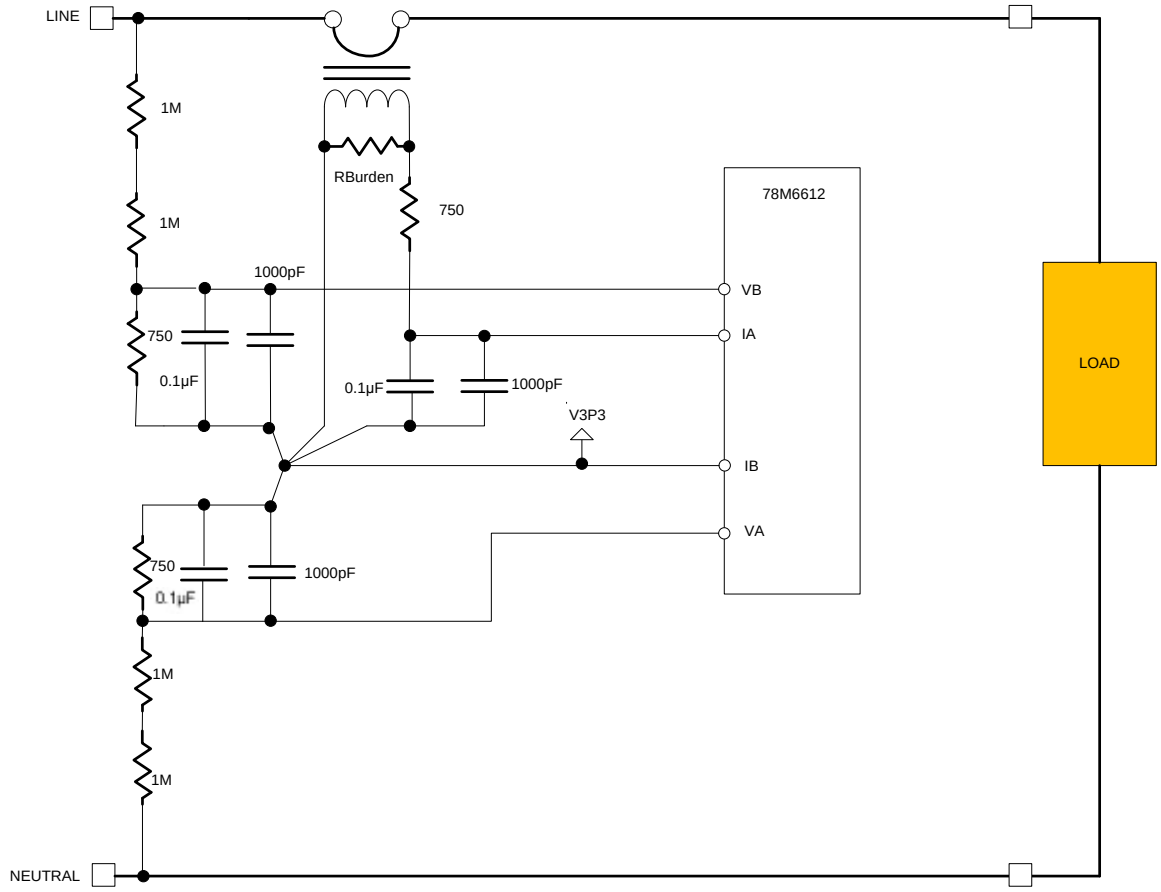


Figure 6: Basic Connection Diagram of a CT-Based System

The use of a CT allows for the 78M6612's V3P3 to be isolated from the plant NEUTRAL wiring. This topology eliminates the safety issues stated earlier regarding shunt-based current sensing. Figure 6 shows a 2 MΩ isolation from the LINE voltage via the voltage divider network. In this topology, the line voltage is a pseudo-differential measurement of VB-VA.

The V3P3 reference point critical to multi-shunt measurement performance is not an issue with CTs. The output currents generated by the CT's secondary winding is small enough that the sheet resistance of the 1 oz. copper plating does not present measurement errors from adjacent CTs. Shield the CTs secondary pins, burden resistor and filter components with top and bottom printed circuit board layer V3P3 plane surfaces. Insert multiple V3P3 vias to interconnect the top and bottom V3P3 structures for a low impedance shield. Refer to the *78M6612 Printed Circuit Board Layout Guidelines* application note for additional layout design recommendations.

See *Using Current Transformers with the 78M661x* for additional information.

3.2 Other Connections

The same power supply decoupling circuit from Section 2.2 can be used for an isolated configuration. The 78M6612 supply and ground connections, however, can be shared with other (isolated) components in the system when V3P3 is not tied to AC Neutral.

Line voltage sensor recommendations for a non-isolated sensor configuration (resistor divider) can also be used in a isolated configuration due to the high impedance connections between high voltage AC and the 78M6612. Alternatively, a voltage transformer (VT) can be used for fully isolated voltage sensing.

3.3 Voltage Transformers

The pseudo-differential voltage measurement circuit of VB-VA shown in Figure 6 can be replaced with a voltage transformer (VT). The VT replaces the two 2 MΩ resistor divider networks and requires use of only V. Use of a CT with a VT provides complete galvanic isolation from the plant wiring. A good quality VT provides accurate linear measurements from 100VAC to 240VAC.

The basic connection of a VT to the 78M6612 is similar to Figure 5. The VT's secondary output voltage range in conjunction with the manufacturer's recommended burden resistor value must meet the 78M6612's signal input range of ±176.78 mVrms (±250 mVpk). Higher output VT secondary voltages can be accommodated using a resistor divider between the VT and the 78M6612.

Use only good quality VTs which introduce minimal phase shift between the primary to secondary winding. The CT phase calibration routine can be used to compensate for any VT phase delay.

Figure 7 shows a basic connection diagram of a CT and VT based system.

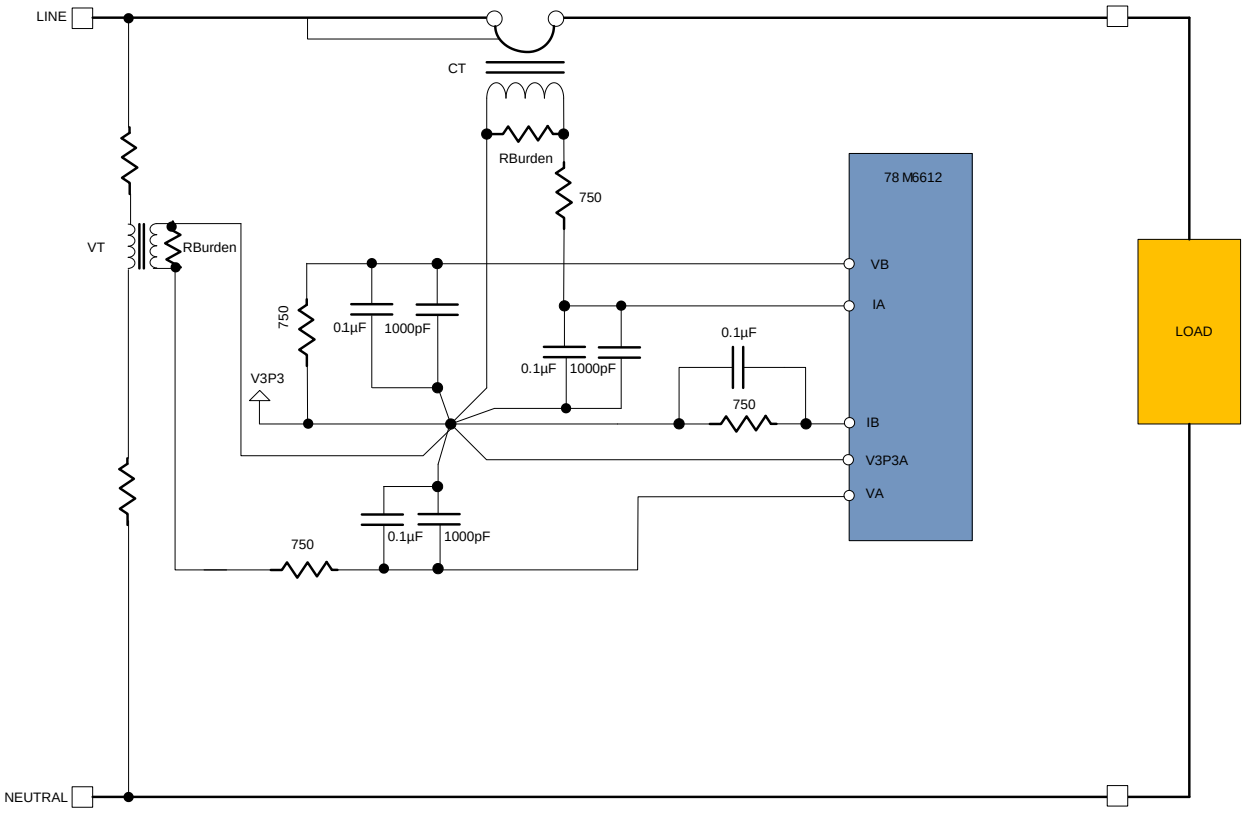


Figure 7: Basic Connection Diagram of a CT and VT Based System

4 Calibration Considerations

All power measurement ICs must employ in-system calibration to achieve higher accuracy. In-system calibration compensates for the PCB trace lengths, LINE input voltage divider resistor network, current sensor tolerances, and 78M6612 IC tolerances. Using tighter tolerance components can help reduce or even eliminate in-system calibration depending on the required measurement accuracy.

As an example, the following table shows different levels of accuracies that can be achieved with different levels of calibration. The Current Only Calibration compensates for only the current sensing resistor tolerance and utilizes 0.1% tolerance resistors for the voltage sensor. The Full Calibration compensates for both the voltage divider plus the current sensor tolerances.

If the system does not require a high level of accuracy relative to the initial tolerance of the voltage divider and current sensor components, predetermined coefficients can also be hard coded into the firmware to eliminate production line calibration and maximize cost savings. Invoke the requisite CLI temperature calibration command for all systems. See the applicable 78M6612 Firmware Description Document for more information on the firmware interface.

Calibration Type	**Time**	**Accuracy**
Full Calibration	< 15s	< 0.5%
Current Only Calibration [1]	< 7.5s	< 1%
No Calibration (fixed coeff.) [1 2]	0	< 2.5

Notes:

1. Use 0.1% tolerance resistors voltage divider.
2. Use 1% tolerance shunt resistor or burden resistor when using a current transformer.

Refer to the *78M661x Calibration Procedure* for additional information.

5 Basic Configuration

This section describes the configuration of the remaining hardware interfaces found on the 78M6612.

5.1 Reset Circuitry

The 78M6612 employs an active high Reset input pin. Figure 7 shows the external circuit configuration using a pushbutton switch to generate the reset signal. If an external reset is not required, connect the Reset pin to GND (GNDD). An external reset is recommended only during the development phase of a project. It is recommended that the RESET pin be grounded for the production version of the PCB.

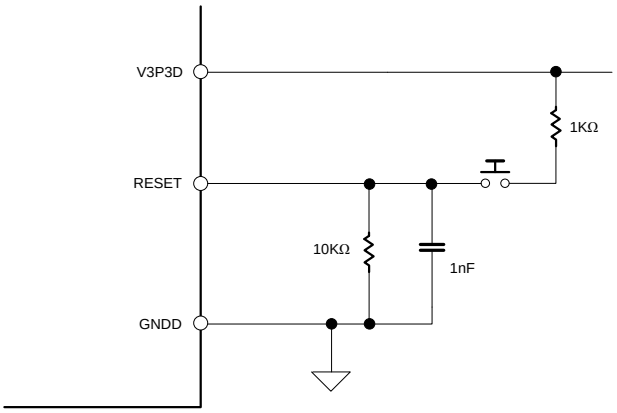


Figure 8: Reset Circuitry

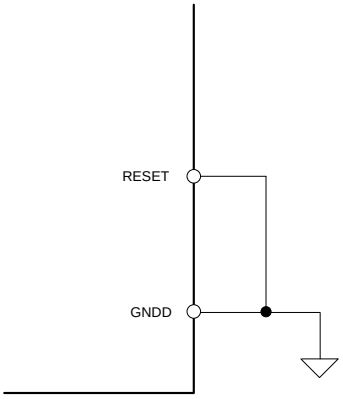


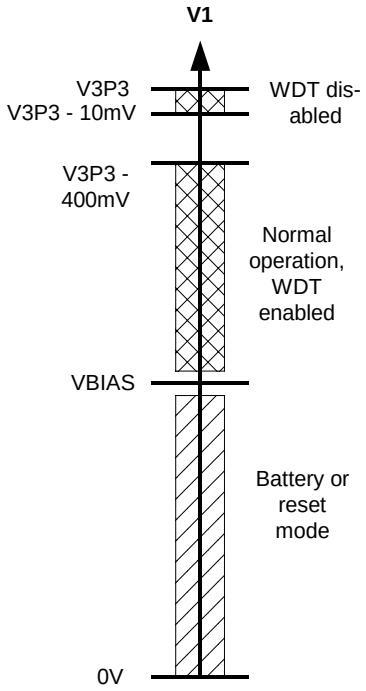
Figure 9: Connection for Unused Reset Pin

5.2 V2P5 Voltage Reference Pin

The V2P5 pin is connected to an internal 2.5 VDC reference voltage. Do not attach external circuitry to this pin. This pin must be left unconnected.

5.3 V1 Pin

The V1 pin is connected to an internal power-fail comparator. The V1 input voltage is compared to an internal reference voltage of 1.6 V (VBIAS). If the V1 voltage is above VBIAS, the comparator output is high (1) signaling normal operation. If the V1 voltage is below VBIAS, the comparator output is low (0) signaling battery mode operation (via an external battery attached to the VBAT pin). Connect the voltage divider shown in Figure 9 to the V1 pin to enable normal (WDT enabled) 78M6612 operation. The watchdog may be disabled for debugging by raising the V1 pin above 2.9 V.



R3 is used to provide hysteresis to the comparator.
The input pin V1 sinks 1 µA when V1< VBIAS and 0 µA when V1 ≥ VBIAS.
Therefore the thresholds are:

$$V3P3 \leq \frac{R1+R2}{R2} VBIAS$$ (High to Low transition, VBIAS = 1.6 VDC)

$$V3P3 > \frac{R1+R2}{R2} (VBIAS + R3 * 1E-6A)$$ (Low to High transition, VBIAS = 1.6 VDC)

C1 provides additional filtering to the V1 input to prevent spurious commutations of the V1 comparator.

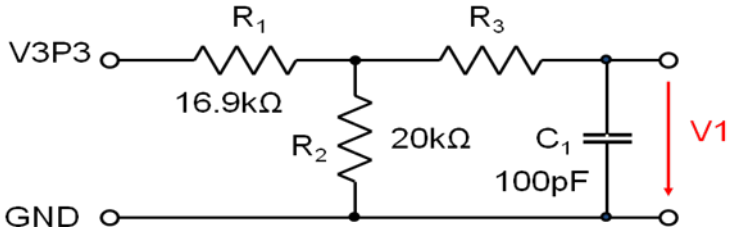


Figure 10: Voltage Divider

5.4 In Circuit Emulator (ICE) Pins

The 78M6612 evaluation boards employ a reduced component ICE interface. This circuit design is sufficient when short ICE cables (less than 12 inches) are used or large RF fields are not present. If either case is not true, the following recommendations are to be utilized.

If the ICE pins are used to drive LCD segments, attach 22 pF capacitors from the ICE signals to GND for EMI protection. If the trace length of the ICE signals exceeds 2 inches, add 22 pF capacitors across the ICE signals to GND for EMI protection. If the external ICE cables exceed 12 inches, insert the series resistors to control signal reflections.

Connect the ICE_EN pin to GND on production boards using pre-programmed 78M6612 devices. Otherwise, provide a strong pull-down resistor (recommend 330 Ω value) along with a filter capacitor of 1000 pF on ICE_EN to allow in-circuit programming.

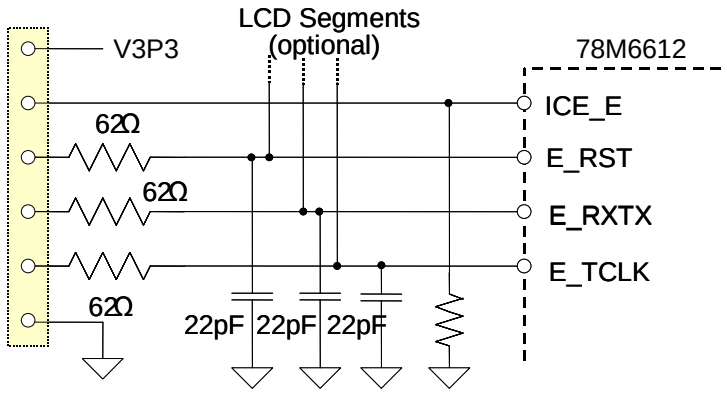


Figure 11: ICE Pin Used to Drive LCD Segments

5.5 Connecting 5 V Devices

All digital input pins (DIO pins) of the 78M6612 are 5 V compatible allowing connection to external 5 V devices. I/O pins configured as inputs do not require current-limiting resistors when they are connected to external 5 V devices.

5.6 Driving External Loads

Connect external loads to the digital outputs (DIO pins) as shown in Figure 11.

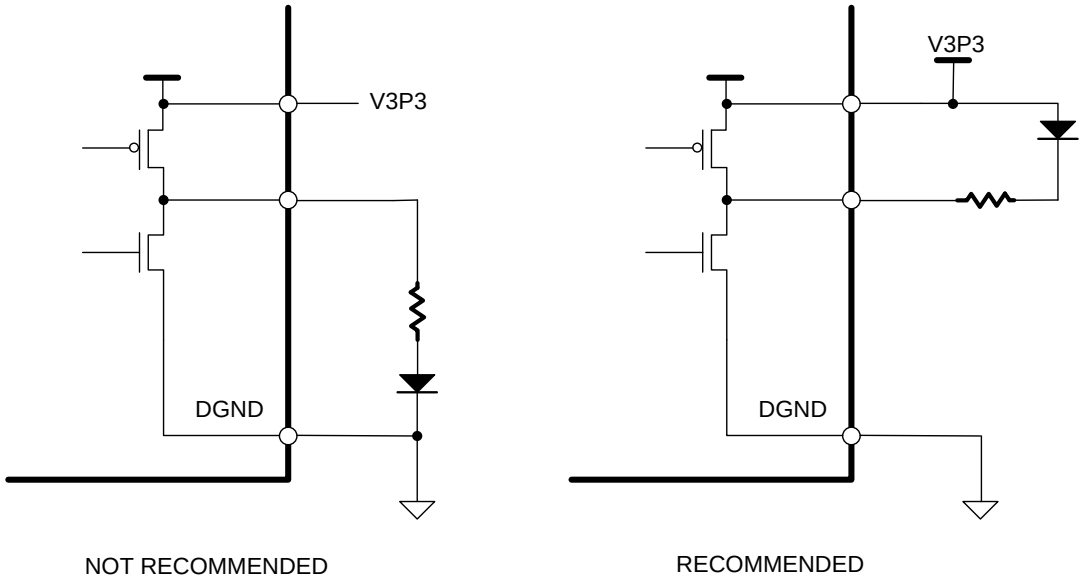


Figure 12: Connecting an External Load to a Digital Output

5.7 Connecting I²C EEPROMs

Connect I²C EEPROMs or other I²C compatible devices to DIO pins DIO4 and DIO5 as shown in Figure 12. Add pull-up resistors of roughly 10 kΩ to V3P3 for both the SCL and SDA signals. The I/O RAM register *DIO_EEX* must be set to 01 to convert the DIO pins DIO4 and DIO5 to SCL and SDA I²C operational mode.

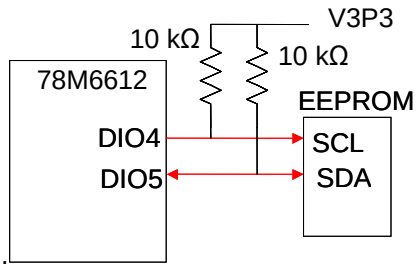


Figure 13: I²C EEPROM Connection

5.8 Connecting 3-Wire EEPROMs

Connect MICROWIRE® EEPROMs and other compatible devices to DIO pins DIO4 and DIO5 as shown in Figure 13. Connect DIO5 to both the DI and DO pins of the three-wire device. Connect the CS pin to a vacant 78M6612 DIO pin. Add a pull-up resistor of roughly 10 kΩ to V3P3 to the DI/DO signals. Add a pull-down resistor to the CS pin to prevent that the 3-wire device from being enabled on power-up before the 78M6612 can establish a stable signal for CS. The I/O RAM register *DIO_EEX* must be set to 10 in order to convert the DIO pins DIO4 and DIO5 to μWire operational mode pins.

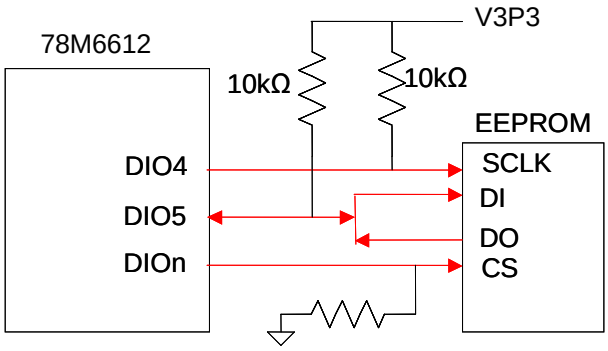


Figure 14: 3-Wire EEPROM Connection

5.9 UART0 (TX/RX)

Attach a 10 kΩ pull-down resistor to the RX input pin. Additionally, include a 100 pF ceramic capacitor for EMI protection as shown in Figure 14.

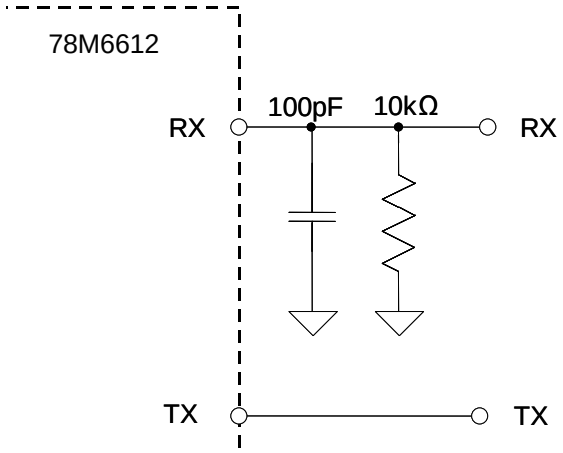


Figure 15: Connections for the RX Pin

5.10 UART1 Interface

The TX1 and RX1 (UART1) pins can be used as a regular serial UART interface, e.g. by connecting a RS-232 transceiver.

Alternatively, they can directly interface to optical components, e.g. an infrared diode and phototransistor implementing a FLAG interface. Contact Maxim's Teridian™ applications support for more information at www.maxim-ic.com/support.

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Teridian is a trademark of Maxim Integrated Products, Inc.

5.11 Power Supply Topologies

Several power supply topologies are presented for consideration as a dedicated source of V3P3 power in non-isolated configurations.

5.11.1 Capacitive

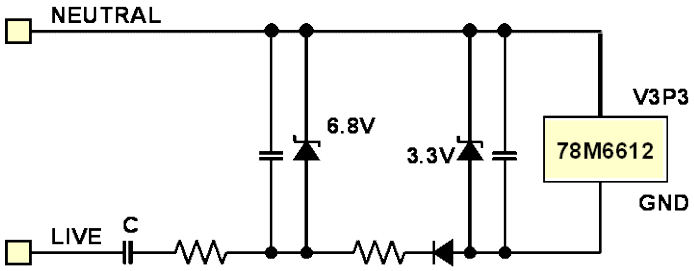

Figure 16: Simple Circuit Design for Low-Power Applications

5.11.2 Transformer

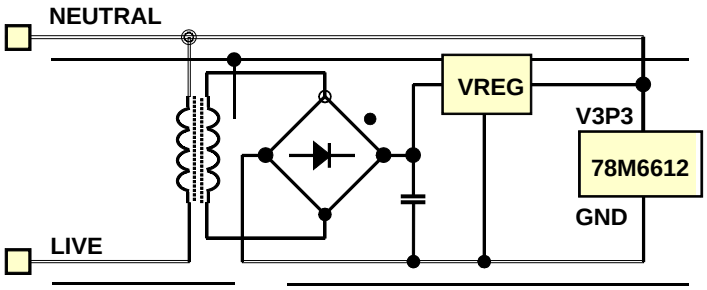

Figure 17: No High-Voltage Components for Higher Power Applications

5.11.3 Half-Wave Rectification with Switch-Mode Power Supply or Regulator

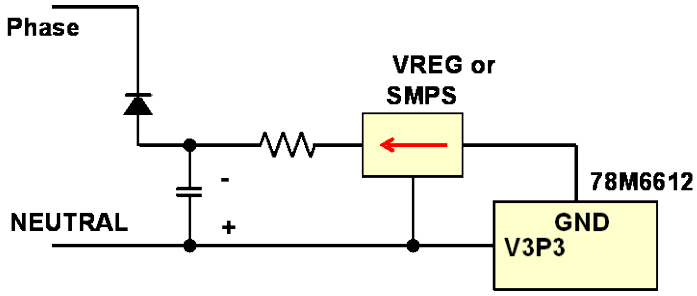

Figure 18: High Efficiency for Higher Power Applications

6 Timing Reference

This section is both a design and troubleshooting guide for using the low-power crystal oscillator interface on the 78M6612.

The 78M6612 typically uses a crystal oscillator as the clock source. Another option is to use an external canned oscillator. The main advantages of a crystal oscillator are frequency accuracy, stability, low cost, high reliability, and low power consumption.

To avoid common problems with crystal oscillators and to achieve high reliability, it is important to pay attention to the components and their values, and the layout. This section shows how these elements affect such factors as stability, temperature variation, start-up time, and noise immunity. It also contains suggestions for solving problems in these areas.

6.1 Oscillator Connections and Components Selection

Figure 18 shows the recommended connection of the crystal oscillator.

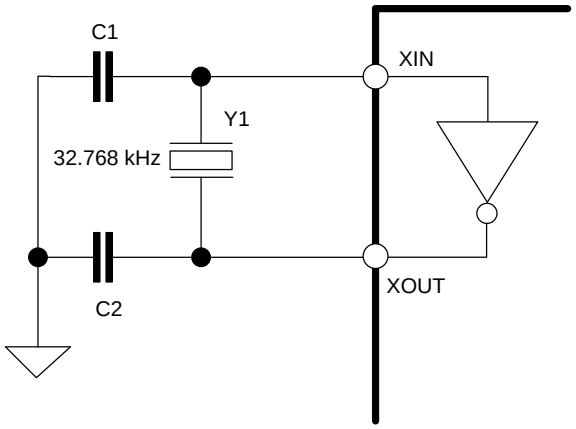

Figure 19: 78M6612 Crystal Oscillator Connection

Typical values for C1 and C2 are 27 pF for a crystal load capacitance value of 12.5 pF.

The crystal output (XOUT) driver strength is internally limited to reduce the power dissipation.

6.2 PCB Layout Recommendations

6.2.1 Power Supply Noise and Electromagnetic Noise

Supply noise and electromagnetic noise are common causes of crystal oscillator failures. The oscillator gain, and the slow rise and fall times (the signal is near sinusoidal), are typical characteristics of a low-power and low-frequency oscillator. Because of these characteristics, the 32-kHz oscillator is sensitive to power supply noise and to electromagnetic coupling.

Do not locate power magnetic components near the crystal oscillator components. Select a PCB layout topology that places the crystal components on the opposite PCB side from the power magnetic components and resulting magnetic fields.

6.2.2 Component Placement

To minimize noise sensitivity to spurious coupling or parasitic antenna phenomena on the PCB, the connections of the crystal to oscillator input and output and to other components must be as short as possible. The best practice is to place the crystal and phasing capacitors as close as possible to the 78M6612. This helps to minimize the length of the connections.

The currents flowing through the two load capacitors (C1 and C2) are in opposition. The best practice is to connect the two capacitors before connecting to the ground reference. At that time, the current back to the ground is significantly reduced. The connections must be as short as possible and of identical lengths. Avoid long connections from these capacitors that make a large loop on the PCB, which behaves like an antenna and can collect surrounding high-frequency radiation.

6.2.3 Layout

The reference ground of the oscillator must be as quiet as possible; otherwise, high-frequency noise is transmitted directly to the oscillator input and output, resulting in degradation of the oscillator performance.

To prevent cross-coupling to fast signals with high-level harmonic content, do not route signal traces through the crystal area. Both oscillator pin connections are critical.

Vias in the oscillator circuit should only be used for connections to the ground plane. Do not share ground connections; instead, make a separate connection to ground for each component that requires grounding. If possible, place multiple vias in parallel for each connection to the ground plane.

The use of high-quality components in the oscillator circuit is equally important to achieve correct and reliable operation. Capacitors should be high-quality capacitors with very low ESR, designed for use in high-frequency applications (i.e., NP0 and COG).

Figure 20, Figure 21, and Figure 22 show layout examples for the crystal oscillator. Figure 20 and Figure 21 show the placement and layout of the crystal oscillator components on the opposite side of the PCB from the 78M6612. The 32.768 kHz crystal and its two 27 pF capacitors are placed on the GND layer. This allows the crystal and the two capacitors to be surrounded with a ground shield. Place the XIN and XOUT vias as close as possible to the 78M6612 pins. Shield the XIN and XOUT signal vias with a Ground plane flood sectioned out of the V3P3 layer.

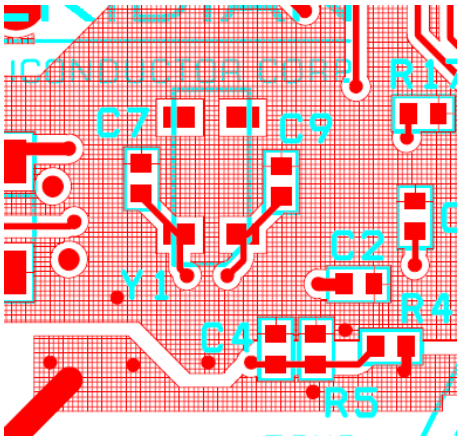

Figure 20: Crystal Y1 and Capacitors C7/C9

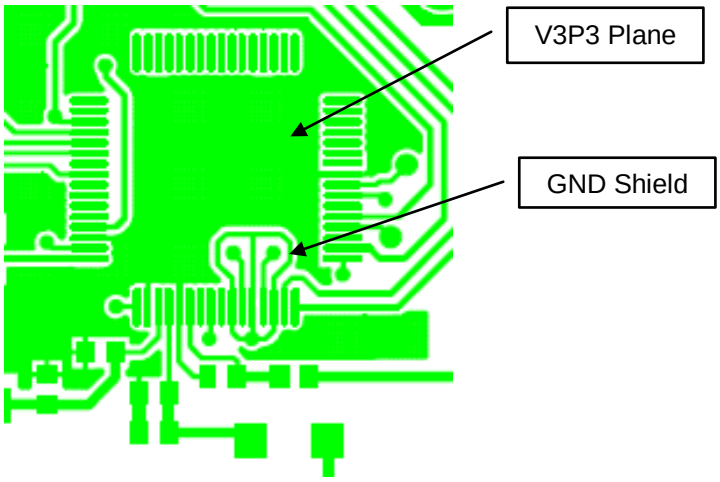

Figure 21: GND Shield Surrounds Crystal Traces

Figure 21 shows the placement and layout of the crystal oscillator components on the same side of the PCB with the integrated circuit (a 78M6613 is used in the example). There is a ground guard-ring surrounding the crystal oscillator. One way to accomplish this is by surrounding the circuit with a wide grounded trace. For this to work, the grounded trace must have zero current flowing through it. In this example, there is a “floating ground” with no connections other than the oscillator’s VSS.

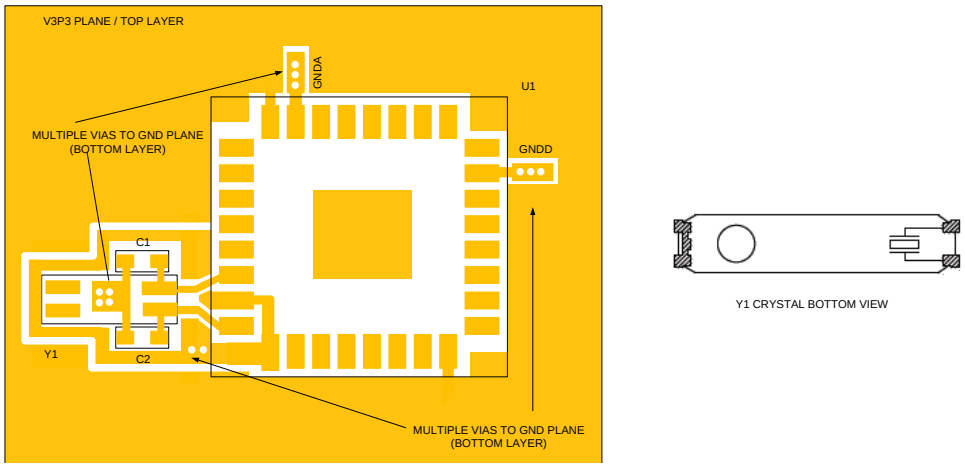

Figure 22: Crystal Oscillator Components on the Same Side

6.3 Other Considerations

6.3.1 Solder Flux, Condensation and Other Conducting Materials

A common cause of crystal oscillator malfunction is the buildup of contaminants on the PCB. PCB contaminants such as flux, humidity, finger prints etc. can create a high-impedance path from one of the oscillator pins to GND or the V3P3 supply preventing oscillator startup. To overcome this problem, check for contaminant accumulation between the crystal leads and beneath the 78M6612 package. Board cleanliness is most critical when using water soluble solder paste.

6.3.2 QFN Substrate Pad

The 789M6612 does not dissipate much heat. Therefore, the size of the underside substrate PCB pad does not have to be equal to the package pad dimensions. A PCB pad dimension of 50% of the package pad dimension minimizes flux residue under the device and eliminates solder shorts due to excessive solder paste from a large pad surface.

6.3.3 Soldering Process

An inappropriate soldering profile can cause excessive stress on the components. Improper handling of the crystal may cause the fracture of the hermetic seal. This would allow moisture and other contaminants to infiltrate the case, causing sporadic operation or complete failure. Excessive temperatures or excessive exposure time to high temperatures due to an inappropriate soldering profile can also damage the crystal.

6.3.4 Oscillator Start-up Time

In general, the startup time for a low-frequency crystal oscillator is longer than for at high-frequency crystal. For a 32.768 kHz crystal, startup should be within the range of 200 – 400 ms. Startup time exceeding 700 milliseconds is most likely an indicator that the crystal is having trouble starting at all, and that the value chosen for the capacitors C1 and C2 does not meet the crystal manufacturer's requirements or there other causes such as contaminants (solder flux etc.).

Crystals require a certain amount of power to start into a stable oscillation pattern. Since the power supplied to the crystal is going to be a function of the power supply, oscillator start-up times are going to be strongly affected by the rise time of the power supply. Another factor is that a power supply with very sharp rise times will act like an impulse to the crystal, causing it to start faster when compared to using a power supply with a very slow rise time. Some crystal characteristics that affect startup time:

- High Q-factor crystal oscillators typically start slower than crystal oscillators with higher frequency tolerance.
- Crystal with low load capacitance typically start faster than crystals requiring high load capacitance.
- Crystals with low ESR start more quickly than high ESR crystals.
- Oscillators with high OA (Oscillation Allowance) start faster than low OA crystal oscillators.

To increase the drive strength and obtain a shorter startup time, it is possible to place a resistor between XOUT and the V3P3 supply. The value of the resistor should be 2.5 MΩ or higher, as shown in Figure 23.

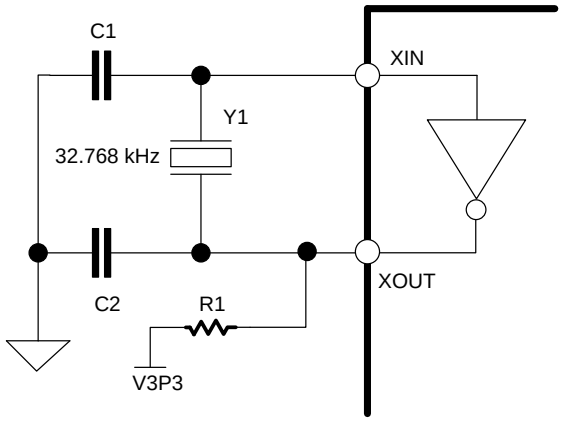

Figure 23: Crystal Oscillator with Pull-up to Reduce Startup Time

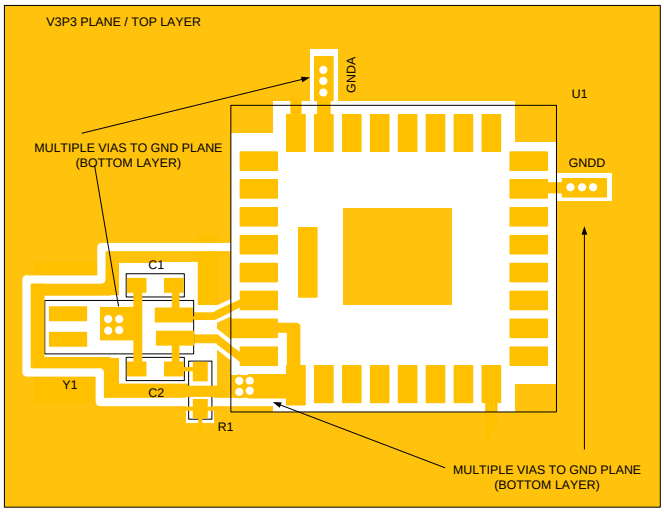

Figure 24: Example of Layout of Crystal Oscillator with Pull-up Resistor

6.3.5 Temperature and Voltage Issues

The crystal oscillator should be tested over the entire temperature and voltage range in which it is expected to operate. The most critical corner is at the highest temperature and lowest supply voltage. This condition leads to minimum loop gain and could result in a slow or no start-up.

To minimize undesirable temperature effects, use capacitors with a low temperature coefficient, such as NP0 or COG types. Verify that all components are specified to work for the entire temperature and voltage range, the crystal in particular.

6.3.6 Use with External Canned Oscillators

The 78M6612 oscillator may be driven from an external 32.768 kHz clock source. The clock source can be derived from a canned oscillator or a divided down system clock. The external clock signal must be attenuated using the resistor divided shown in Figure 25.

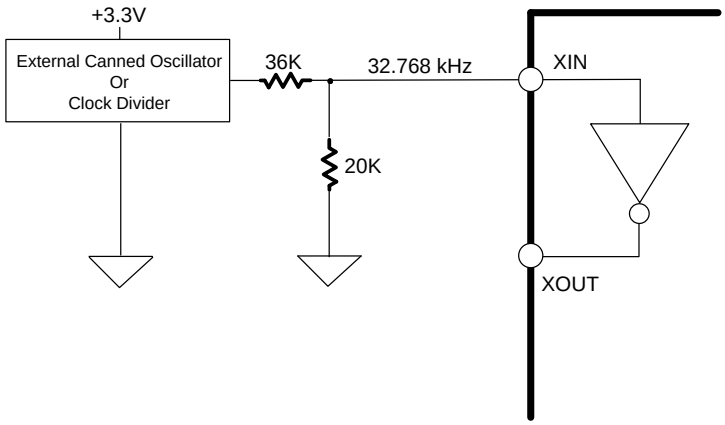

Figure 25: 78M6612 with External Canned Oscillator

7 Hardware Design Checklist

Verified	Item	Notes
	Non-isolated Configuration	3.3 VDC supply rail (V3P3) for the 78M6612 must be directly connected to AC-Neutral.
	Non-isolated Configuration	Isolation components, if required, are added in between the measurement IC and the rest of the system.
	Safety Precautions	External test equipment must be floated from earth ground to avoid equipment damage.
	Safety Precautions	AC outlets must be properly wired.
	Crystal Capacitor's Value	Capacitance value is 27 pF for 32.768 kHz crystal. No resistor across XTAL.
	Shunt Value	Calculate value based on maximum load current. Not to exceed ±250 mVpp.
	Shunt Power Rating	Optimize shunt value at maximum load current for required power dissipation.
	Line Voltage Resistor Divider Selection	Calculate value based on maximum input LINE voltage. Not to exceed ±250 mVpp.
	Line Voltage Divider Resistor Rating	Select package based on its maximum voltage rating and isolation clearance requirements.
	CT Turns Ratio and Power Rating	Select configuration based on maximum load current.
	CT Burden Resistor Value Calculation	Calculate value based on maximum load current and CT turns ratio. Not to exceed ±250 mVpp.
	V3P3 Decoupling Capacitor Value and Placement	1000 pF and 0.1 µF ceramic capacitors placed as close as possible to the 78M6612 V3P3A pin. Add a 22 µF bulk capacitor.
	V1 Pin	Calculate for V1 pin voltage to be between 1.6 V and 2.9 V for normal operation.
	Reset Circuitry	Active high. Connect to GND or pull low.
	In Circuit Emulator (ICE) Pins	Connect ICE_EN pin to GND or pull low.
	Driving External Loads	Connect external loads to the DIO pins.
	Connecting I2C EEPROMs	Connect I^2C EEPROMS or µWire EEPROMS to DIO pins.
	UART0 (TX/RX)	Attach a 10 kΩ pull-down resistor to the RX pin. Include a 100 pF ceramic capacitor for EMI protection.
	Power Supply Topologies	Select a source of V3P3 power.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION
1.0	3/23/2010	First publication.
1.1	8/30/2010	Added the Timing Reference section; fixed VB connection in Figure 1.
1.2	10/29/2010	Added “The V3P3 connection to AC-Neutral can be eliminated when using current transformers (CT) as the current sensing elements. Refer to the section on Isolated Connections for designing with CTs.” to Section 2. In Section 2.2, added a note about the values used for the anti-aliasing filters. Added Section 3.3, Voltage Transformers.
2	11/2/2011	Corrected Figure 7.