

Evaluating the **ADAR1000** 8 GHz to 16 GHz, 4-Channel, X Band and Ku Band Beamformer

FEATURES

Based on the **ADAR1000** 4-channel beamformer
 Controllable through SPI
 Multiple forms of digital interface (3.3 V and 1.8 V logic)
 On-board logic level translators with 1.8 V low dropout regulator for supply
 Software control from a Windows-based PC through USB

ADDITIONAL EQUIPMENT

PC running Windows XP or a more recent software version
SDP-S or **SDP-B** USB interface board
 Network analyzer
 Power supplies: 3.3 V, -5.0 V

DOCUMENTS NEEDED

ADAR1000 data sheet

REQUIRED SOFTWARE

ADAR1000-EVALZ evaluation software

GENERAL DESCRIPTION

The ADAR1000-EVALZ is designed for evaluating the performance of the **ADAR1000** 4-channel, X band and Ku band beamformer for radar systems. All radio frequency (RF) input/output channels and detector inputs are brought out to Subminiature Version A (SMA) connectors. On-board logic level translators convert the on-chip 1.8 V logic signals to 3.3 V for interfacing to external controllers running on 3.3 V. Two identical, 20-pin, dual row, rectangular headers provide the digital interface signals to allow daisy-chaining up to four ADAR1000-EVALZ boards together. A 24-pin connector provides control and bias outputs to interface to four external transmit and receive modules with each ADAR1000-EVALZ.

The ADAR1000-EVALZ can be used with an Analog Devices, Inc., system demonstration platform (SDP) **SDP-S** or **SDP-B** board (supplied separately), which allows connection to a Microsoft Windows®-based PC through the USB for controlling all **ADAR1000** device functions.

For full details on the **ADAR1000**, see the **ADAR1000** data sheet, which must be consulted in conjunction with this user guide when using the ADAR1000-EVALZ.

EVALUATION BOARD PHOTOGRAPH

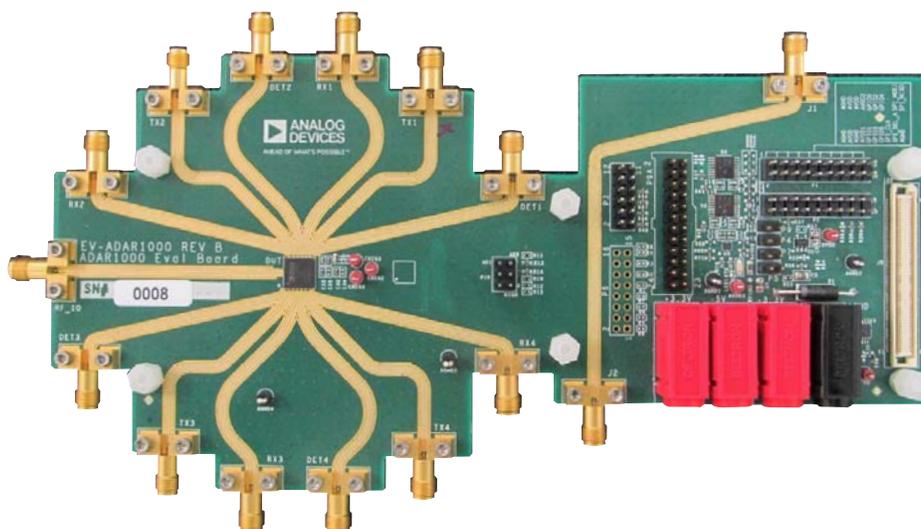


Figure 1.

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REVISION HISTORY

8/2019—Rev. 0 to Rev. A

Changes to Required Software Section and General
Description Section..... 1

Changes to Figure 3 and Table 3..... 4

Change to Peripheral Module-Compatible Interface Section 5

Added Transmit and Receive Startup Using the GUI Section,
Resetting the Registers, Changing to a 4-Wire SPI, and Setting
the LDO Voltage Section, Figure 6, Transmit Startup Section,
Bypassing the RAM Section, Figure 7, Enabling Transmit
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Added Setting Transmit Bias Currents Section, SPI Control and
Enabling Transmit Mode Section, Transmit Gain Control
Section, Transmit Phase Control Section, Figure 9, Figure 10,
Figure 11, and Figure 12 9

Added Transmit Load Override Section, Receive Startup
Section, Bypassing the RAM Section, Enabling Receive
Channels Section, Setting Receive Bias Currents Section,
Figure 13, Figure 14, Figure 15, and Figure 16 10

Added SPI Control, Enabling Receive, and Receive Mode
Section, Receive Gain Control Section, Receive Phase Control
Section, Receive Load Section, Control Using the Manual
Register Write Section, Figure 17, Figure 18, Figure 19,
and Figure 20..... 11

Added Figure 21, Figure 22, and Figure 23..... 12

Changes to Quick Test Procedure Section 13

Added Figure 26 13

Changes to Detailed Software Description section 14

Changes to Transmit and Receive Control Tab Section..... 17

Changes to MISC Tab Section 18

Changes to Beam Sequencer Tab Section and
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6/2018—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

Figure 1 shows the ADAR1000-EVALZ, with 13 high frequency connectors for the four transmit outputs, four receive inputs, four detector inputs, and a common RF input and output. Four on-board banana jacks provide power supply connections and a connector for an SDP adapter board that interfaces with the USB on a Windows-based PC. Dual row, square pin headers allow connections to four transmit and receive modules, as well as the daisy-chaining of up to four ADAR1000-EVALZ boards together.

The ADAR1000-EVALZ requires an [SDP-S](#) or [SDP-B](#) adapter board to program the device. The ADAR1000-EVALZ evaluation software and the examples provided in this user guide both make use of this SDP connection. The SDP adapters are not included with the ADAR1000-EVALZ, but these adapters are available through local Analog Devices distributors, as well as on the [SDP](#) product page.

The interface signals on the [ADAR1000](#) core chip, plus additional digital interface circuitry, are made available on the ADAR1000-EVALZ, as shown in Figure 2.

POWER SUPPLY REQUIREMENTS

The ADAR1000-EVALZ is powered via two external supplies (see Table 1). Connections to the ADAR1000-EVALZ are described in the Quick Test Procedure section. Note that the -3.3 V banana jack has no function and therefore is not populated.

Table 1. External Supply Details

Pin Supply	Board Label	Capacity
AVDD3	+3.3	3.3 V (600 mA)
AVDD1	-5V	-5.0 V (50 mA)

RADIO FREQUENCY INPUT AND OUTPUT SIGNALS

The ADAR1000-EVALZ has 13 edge mounted SMA connectors for RF inputs and outputs (see Table 2).

Table 2. SMA Connectors

Connector	Description
RF_IO	Common RF output connector in receive mode and common RF input connector for transmit mode
RX1 to RX4	Receive channel inputs to connect to antennas or low noise amplifiers (LNAs)
TX1 to TX4	Transmit channel outputs to connect to antennas or power amplifiers (PAs)
DET1 to DET4	Detector inputs designed for measuring the sampled level of each RF output channel

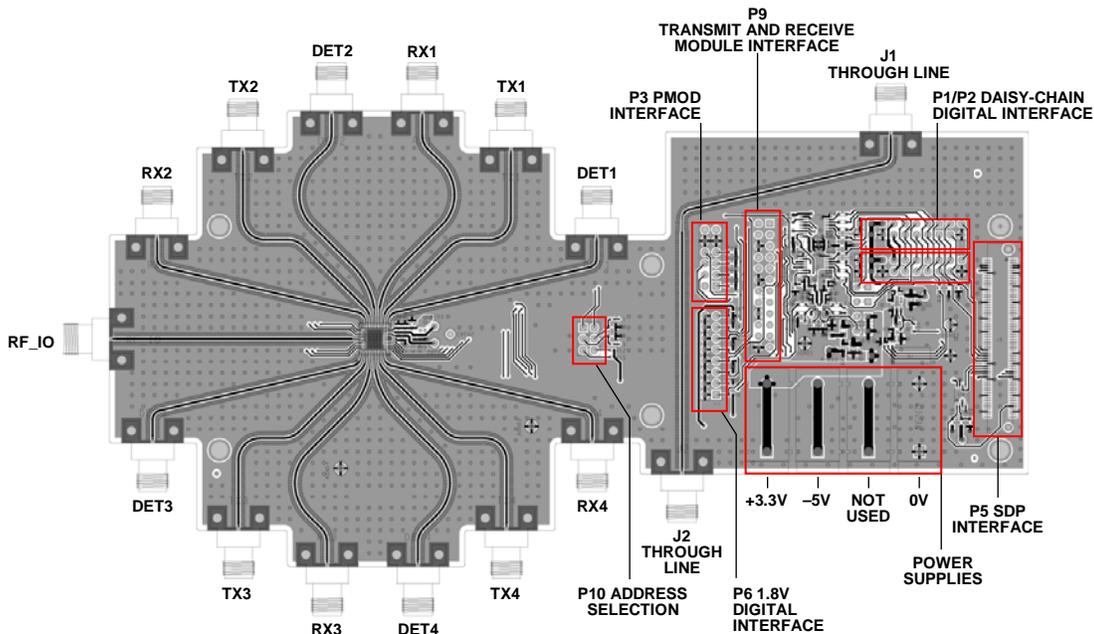


Figure 2. ADAR1000-EVALZ Evaluation Board Connections

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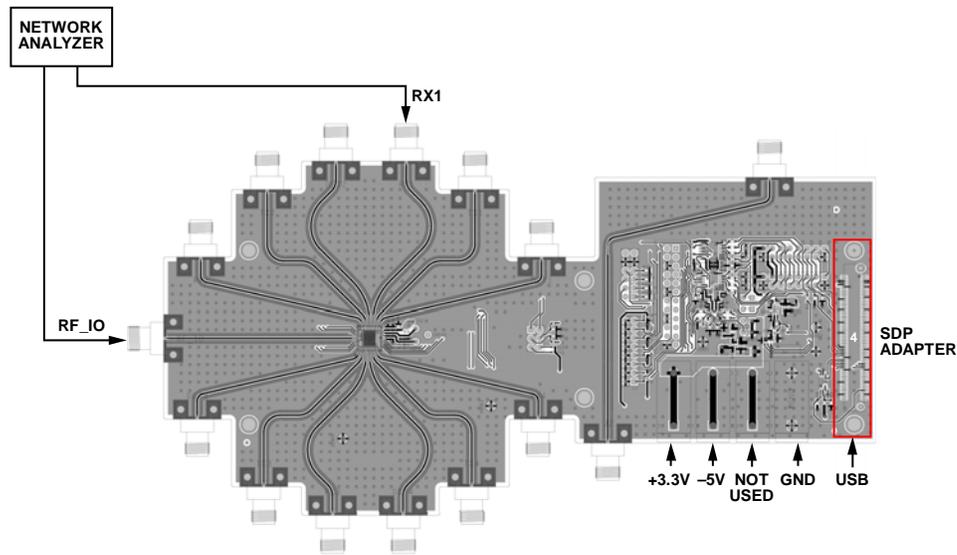


Figure 3. Typical Evaluation Board Setup

DIGITAL INPUT AND OUTPUTS

SDP Connector

The J5 connector interfaces to the SDP adapter that connects to a Windows-based PC. A detailed description of the SDP adapter is found in the [SDP-S Controller Board](#) user guide. All internal registers and control functions of the ADAR1000-EVALZ are driven from the PC using the ADAR1000-EVALZ evaluation software.

Daisy-Chain Interface Connectors

The 20-pin connectors (P1 and P2) also carry the digital signals for controlling the [ADAR1000](#). The two connectors have identical pinouts and the connectors daisy-chain up to four ADAR1000-EVALZ boards controlled through a single USB interface. All signals on these connectors except Pin 15 operate at 3.3 V logic levels, and these signals pass through 3.3 V to 1.8 V logic translators before connecting to the digital pins on the [ADAR1000](#), which operate at 1.8 V logic levels. The serial data output (SDO) pin from each [ADAR1000](#), with the 1.8 V logic levels, can be tied together through the daisy chain (Pin 15 on P1 and P2) by installing a 0 Ω resistor jumper (R36). The pinout of P1 and P2 is shown in Table 3.

The TR, TX_LOAD, RX_LOAD, and PA_ON pins on the [ADAR1000](#) are also controlled by software via general-purpose input output (GPIO) lines on the SDP connector and 3.3 V to 1.8 V level shifters.

Table 3. Digital Interface—Connectors P1 and P2 Pinout

Pin ¹	Signal Name	Function
1	AGND	Analog ground
2	AGND	Analog ground
3	AVDD	3.3 V supply
4	AVDD	3.3 V supply
5	AVDD	3.3 V supply
6	AGND	Analog ground
7	AVDD1	–5 V supply
8	No connect	Not used
9	GPIO0	RX_LOAD input
10	GPIO1	TX_LOAD input
11	GPIO2	ADDR0 (chip Address 0) input
12	GPIO3	ADDR1 (chip Address 1) input
13	GPIO4	TR input
14	GPIO5	PA_ON input
15	SDO	Device serial data output (1.8 V logic)
16	SPI_CLK	Serial clock input
17	SPI_MOSI	Serial data input
18	SPI_SEL_A	Serial enable input, active low
19	SPI_MISO	Serial data output
20	AGND	Analog ground

¹ 3.3 V logic, unless noted otherwise.

Device Interface with 1.8 V Logic Levels

Logic signals on the [ADAR1000](#) are brought to an optional connector, P6, to allow direct interface to the device using 1.8 V logic signals. To operate in this mode, the logic level translators (U2, U4, and U5) must be disabled using the J4, J5, J7, and J9 jumpers. The pinout for connector P6 is shown in Table 4.

Table 4. 1.8 V Logic Connector P6 Pinout

Pin	Signal Name	Function
1	CSB	Serial port enable input (active low)
2	AGND	Analog ground
3	SDIO	Serial data input and output
4	AGND	Analog ground
5	SDO	Serial data output
6	AGND	Analog ground
7	SCLK	Serial clock input
8	AGND	Analog ground
9	TR	Transmit and receive switching input
10	AGND	Analog ground
11	TX_LOAD	Load transmit configurations input
12	AGND	Analog ground
13	RX_LOAD	Load receive configurations input
14	AGND	Analog ground
15	PA_ON	PA bias enable input
16	AGND	Analog ground

Board Address Selection

The ADAR1000 supports up to four devices on the same serial peripheral interface (SPI) connection, with each device identified by the corresponding ADDR0 and ADDR1 pin logic values and addressed by the SPI bits (AD1 and AD0). See the ADAR1000 datasheet for more details. Jumper Block P10 allows the user to determine whether the ADDR0 and ADDR1 pin values are high or low, as shown in Table 5. Note that P10 is labeled AD0 and AD1 on the ADAR1000-EVALZ, which corresponds to the ADDR0 and ADDR1 pins, respectively.

Table 5. Jumper Block P10 Selections

Jumper Connection	Function
Position 1 to Position 3	AD1 is controlled by SDP GPIO2
Position 3 to Position 5	AD1 = high
Position 3 (Not Connected)	AD1 = low
Position 2 to Position 4	AD0 is controlled by SDP GPIO3
Position 4 to Position 6	AD0 = high
Position 4 (Not Connected)	AD0 = low

Peripheral Module-Compatible Interface

The 3.3 V digital interface signals are also repeated on Connector P3, arranged to be compatible with the peripheral module interface connector available on many field programmable gate array (FPGA) evaluation kits or modules. Appropriate FPGA programming is required to use this function. The pinout of the P3 connector is shown in Table 6.

Table 6. Peripheral Module-Compatible Interface (P3)

Pin	Signal
1	GPIO0 (RX_LOAD)
2	SPI_SEL_A
3	GPIO1 (TX_LOAD)
4	SPI_MOSI
5	GPIO4 (TR)
6	SPI_MISO
7	GPIO5 (PA_ON)
8	SPI_CLK
9	AGND
10	AGND
11	No connect
12	No connect

TRANSMIT AND RECEIVE MODULE CONTROL SIGNALS

The ADAR1000 controls the operation of four transmit and receive modules, which typically contain an LNA, a PA, a transmit and receive selection switch, and possibly a polarization selection switch. The 24-pin header, P9, contains signals in groups of six to control the four transmit and receive modules. The pinout of P9 is shown in Table 7.

Table 7. Transmit and Receive Module Interface Connector P9 Pinout

Pin	Signal
1	TR_SW_NEG
2	LNA_BIAS
3	TR_SW_POS
4	TR_POL
5	PA_BIAS4
6	AGND
7	TR_SW_NEG
8	LNA_BIAS
9	TR_SW_POS
10	TR_POL
11	PA_BIAS3
12	AGND
13	TR_SW_NEG
14	LNA_BIAS
15	TR_SW_POS
16	TR_POL
17	PA_BIAS2
18	AGND
19	TR_SW_NEG
20	LNA_BIAS
21	TR_SW_POS
22	TR_POL
23	PA_BIAS1
24	AGND

The ADAR1000-EVALZ has eight signals for driving switches and biasing amplifiers on transmit and receive modules available on Connector P9 (see Table 8). Switch driver outputs as well as

LNA bias outputs are common to all four channels, whereas each PA has an individual corresponding own bias output.

Table 8. Transmit and Receive Module Interface Signal Descriptions

Signal	Description
TR_SW_NEG	0 V to –5 V output to drive an external transmit and receive switch
TR_SW_POS	0 V to 3.3 V output to drive an external transmit and receive switch
TR_POL	0 V to –5 V output to drive an external antenna polarization switch
LNA_BIAS	Provides a common bias control voltage (0 V to –4.8 V) for external LNAs
PA1_BIAS to PA4_BIAS	Provide individual bias control voltage (0 V to –4.8 V) for each of the four PAs

EVALUATION BOARD SOFTWARE INSTALLATION

To install the ADAR1000-EVALZ evaluation software, take the following steps:

1. The ADAR1000-EVALZ evaluation software zip file is available for download on the [ADAR1000](#) product page.
2. Save the **adar1000_eb_sw_2p1p0.zip** to the **Downloads** folder or any other convenient location (see Figure 4). Navigate to that location using the **File Manager** and double click the file name to open it.

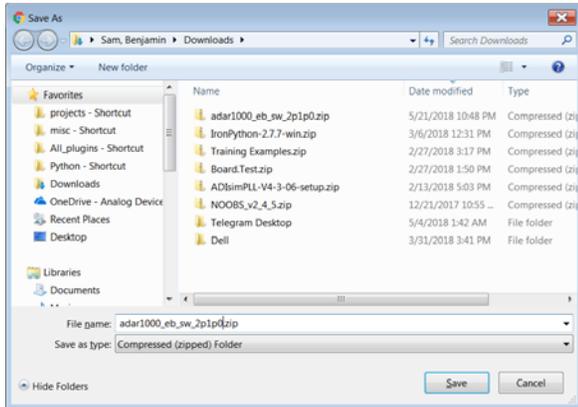


Figure 4. Saving Downloaded Control Software Zip File

3. The **File Manager** shows the content of the zip file, as shown in Figure 5.

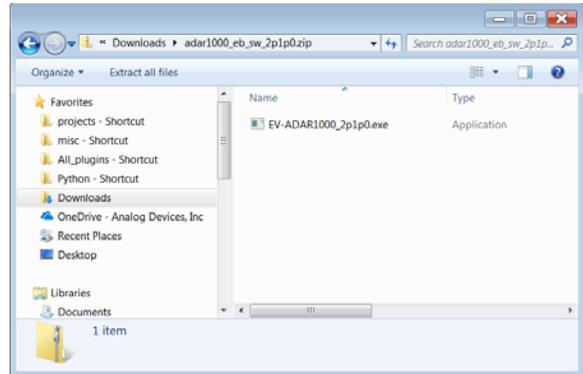


Figure 5. Unpacking Software Zip File

4. Double click the **EV-ADAR1000_2p1p0.exe** file to start the installation. Click **Yes** when asked to allow the program to make modifications to the PC. Administrator privileges may be required to complete the step.
5. When the application is installed, **ADAR1000** is available in the **Start** menu under the **Analog Devices** folder.

TRANSMIT AND RECEIVE STARTUP USING THE GUI

The ADAR1000-EVALZ evaluation software can be used in one of the following ways:

- Operation of the graphical user interface (GUI) to control the device settings and perform register writes. This method includes all GUI tabs except for the **Manual Register Write** tab and the **ReadBack** tab.
- Use the **Manual Register Write** tab and the **ReadBack** tab to write to a single register, read from a single register, or write to multiple registers at once using a .txt file that contains specific registers and data. This method is user defined and created.

The following sections describe how to operate the ADAR1000-EVALZ from power-on using the GUI or using .txt files for quick writes to the necessary registers.

RESETTING THE REGISTERS, CHANGING TO A 4-WIRE SPI, AND SETTING THE LDO VOLTAGE

Perform a soft reset of the device before working with the **ADAR1000** to ensure that the device is in a known state. To perform a soft reset, write 0x81 to Register 0x000. Next, write 0x18 to Register 0x000 to activate the SDO pin and place the device in 4-wire SPI mode and read back from the device via the SPI_MISO line. To write to the LDO regulator trim register to trim the LDO regulator to approximately 1.8 V, write 0x55 to Register 0x400.

These commands can only be given in the **Manual Register Write** tab, either all at once in the **Load and Write** section or individually in the **Values to write** section (see Figure 6).

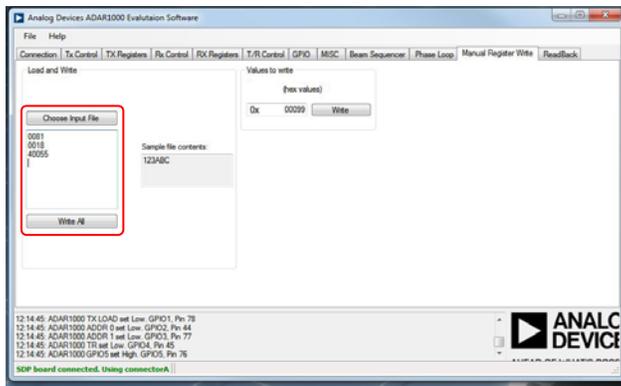


Figure 6. Using the Load and Write Feature to Perform Several Writes

When all values are loaded via a .txt file or typed manually, click **Write All** to write the data to the device.

TRANSMIT STARTUP

When powering up the device or after performing a soft reset, the **ADAR1000** sources the gain, phase, and bias data from the on-chip random access memory (RAM), which is accessed via Register Address 0x1000 through Register Address 0x1FFF. When operating the device for the first time, use the control registers (Register 0x0000 to Register 0x0FFF) to set the gain,

phase, and bias. The following procedures bypass the RAM, enable transmit subcircuits, set SPI control (vs. TR pin control), place the device in transmit mode, and set transmit Channel 1 to maximum gain and 45° phase.

Bypassing the RAM

To bypass the on-chip RAM and source the gain and phase data from the configuration registers, take the following steps:

1. Click the **MISC** tab (see Figure 7).
2. Select the **BEAM RAM BYPASS** check box and the **BIAS RAM BYPASS** check box.
3. Click **Write Value**.

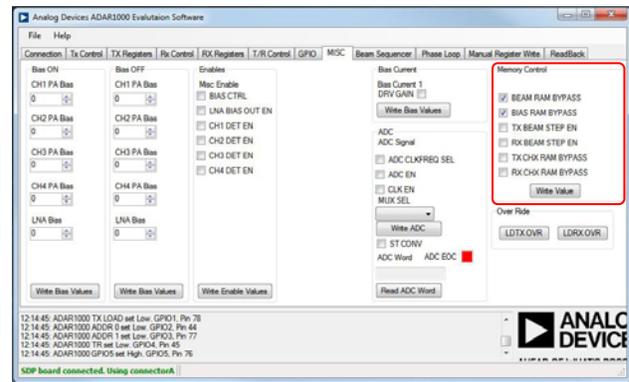


Figure 7. Placing the Device in RAM Bypass Mode

Enabling Transmit Channels

To enable the transmit channels and associated circuits, take the following steps:

1. Click the **T/R Control** tab (see Figure 8).
2. Select all check boxes in the **Tx Enable** section to enable all four transmit channels and the corresponding subcircuits.
3. Click **Write Enable Values**.

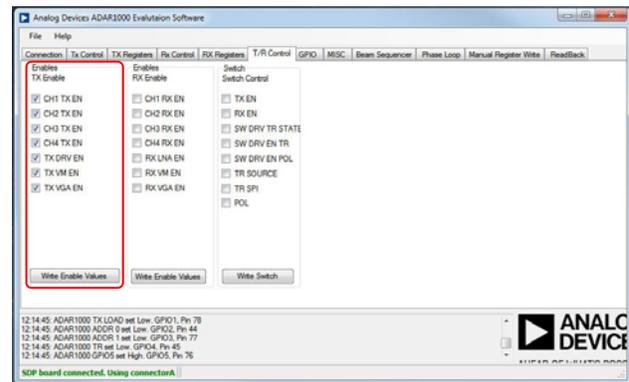


Figure 8. Enabling Transmit Channels

Setting Transmit Bias Currents

To set the nominal bias currents for the transmit variable gain amplifiers (VGAs), vector modulators, and drivers, take the following steps:

1. Click the **TX Registers** tab (see Figure 9).
2. In the **Bias Current** section, set **TX VGA BIAS** to 2, set **TX VM BIAS** to 6, and set **TX DRV BIAS** to 6.
3. Click **Write Bias Values**.

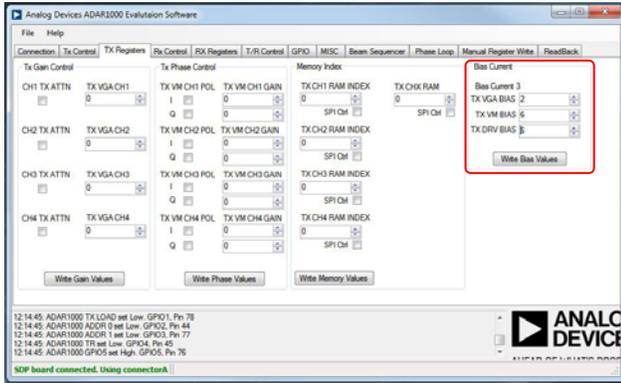


Figure 9. Setting Transmit Bias Currents

SPI Control and Enabling Transmit Mode

To operate in transmit mode, take the following steps:

1. Click the **T/R Control** tab (see Figure 10).
2. Select the **TX EN** check box to enable transmit subcircuits in SPI control. Note that the TX_EN bit is AND'ed together with the transmit enable bits in Register 0x02F such that the transmit paths and subcircuits do not enable until the TX_EN bit is asserted high.
3. Select the **TR SPI** check box to place the device in transmit mode.
4. Click **Write Switch**.

Note that leaving the **TR SOURCE** check box cleared places the device in SPI control mode, which is the default mode.

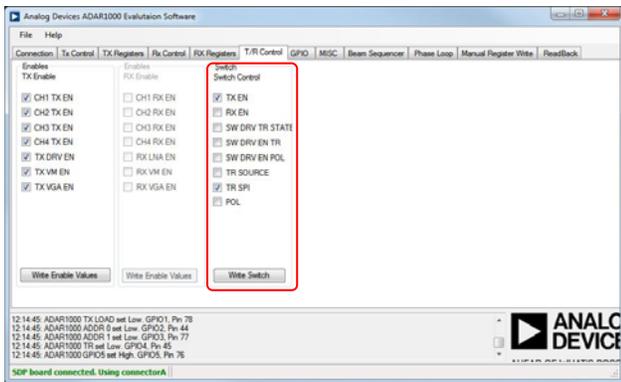


Figure 10. SPI Control, Transmit Enable, and Transmit Mode

Transmit Gain Control

To set the transmit Channel 1 gain to maximum, take the following steps:

1. Click the **TX Registers** tab (see Figure 11).
2. Select the **CH1 TX ATTN** check box to bypass the attenuator on Channel 1.
3. Set the **TX VGA CH1** value to 127 to set the VGA to maximum gain on Channel 1.
4. Click **Write Gain Values**.

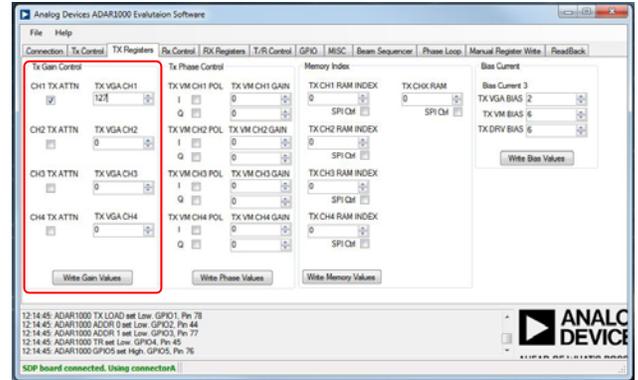


Figure 11. Setting Transmit Channel 1 to Maximum Gain in Transmit Gain Control with All Other Channels at Minimum Gain

Transmit Phase Control

To set transmit Channel 1 to 45° phase, take the following steps:

1. Click the **TX Registers** tab (see Figure 12).
2. Select the **I** and **Q** check boxes under **TX VM CH1 POL** to set the polarity bits so that the vector is in the first quadrant.
3. Set the **I** and **Q** values under **TX VM CH1 GAIN** to 22 for a resulting vector of 45° phase.
4. Click **Write Phase Values**.

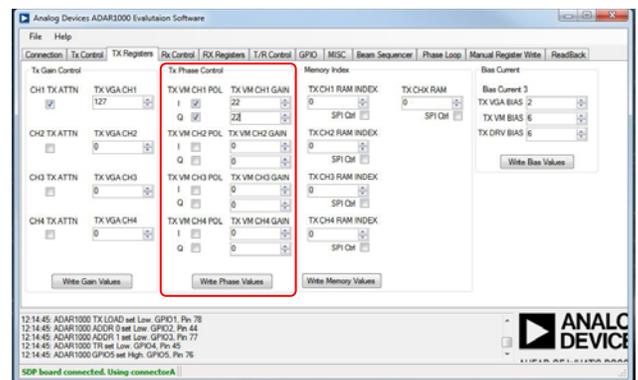


Figure 12. Setting Transmit Channel 1 to 45° in Transmit Phase Control with All Other Channels at 0°

Transmit Load Override

For the gain and phase changes to take effect, a load transmit override command must be given. To give this command, take the following steps:

1. Click the **MISC** tab (see Figure 13).
2. In the **Over Ride** section, click **LDTX OVR**.

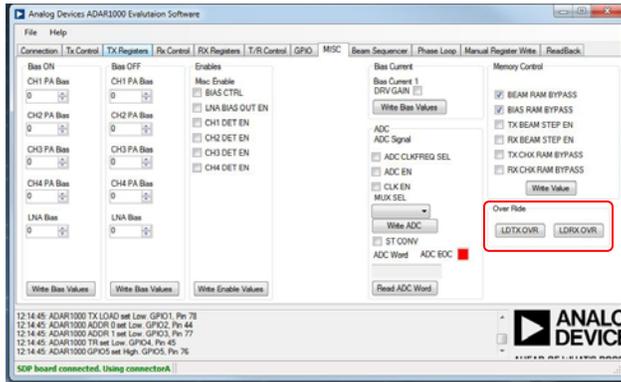


Figure 13. Load Transmit Override

RECEIVE STARTUP

The following procedures bypass the RAM, enable receive subcircuits, set the device to SPI control, place the device in receive mode, and set Receive Channel 1 to maximum gain and 45° phase.

Bypassing the RAM

To bypass the on-chip RAM and source the gain and phase data from the configuration register, take the following steps:

1. Click the **MISC** tab (see Figure 14).
2. Select the **BEAM RAM BYPASS** check box and the **BIAS RAM BYPASS** check box.
3. Click **Write Value**.

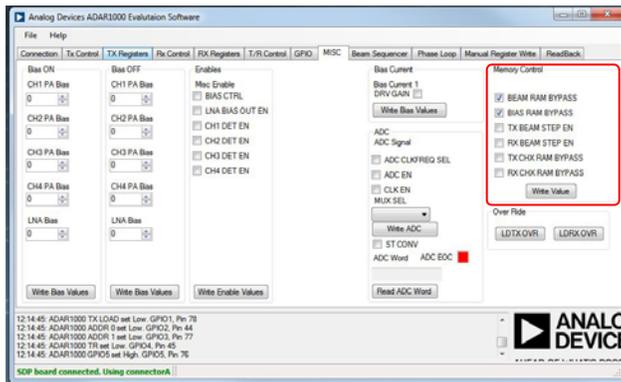


Figure 14. Placing the Device in RAM Bypass Mode

Enabling Receive Channels

To enable the receive channels and associated circuits, take the following steps:

1. Click the **T/R Control** tab (see Figure 15).
2. Select all check boxes in the **Rx Enable** section to enable all four receive channels and the corresponding subcircuits.
3. Click **Write Enable Values**.

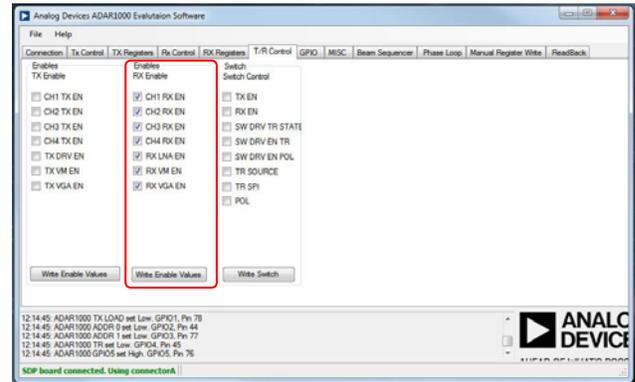


Figure 15. Enabling Receive Channels

Setting Receive Bias Currents

To set the nominal bias currents for the receive VGAs, vector modulators, and drivers, take the following steps:

1. Click the **RX Registers** tab (see Figure 16).
2. In the **Bias Current** section, set **RX VGA BIAS** to 2, set **RX VM BIAS** to 6, and set **LNA BIAS** to 8.
3. Click **Write Bias Values**.

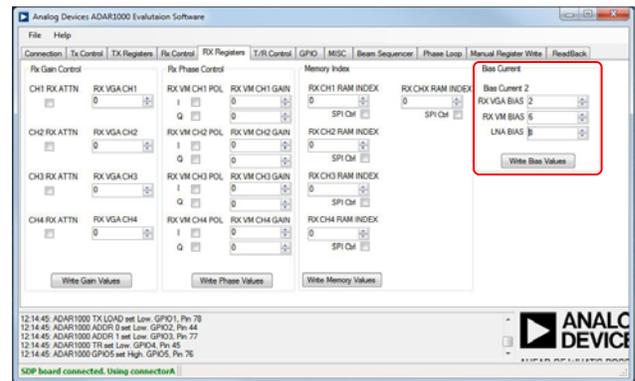


Figure 16. Setting Receive Bias Currents

SPI Control, Enabling Receive, and Receive Mode

To operate in receive mode, take the following steps:

1. Click the **T/R Control** tab (see Figure 17).
2. Select the **RX EN** check box to enable the receive subcircuits in SPI control. Note that the RX_EN bit is AND'ed together with the receive enable bits in Register 0x2E such that the receive paths and subcircuits do not enable until the RX_EN bit is asserted high.
3. Leave the **TR SPI** check box cleared to place the device in receive mode.
4. Click **Write Switch**.

Note that leaving the **TR SOURCE** check box cleared places the device in SPI control mode, which is the default mode.

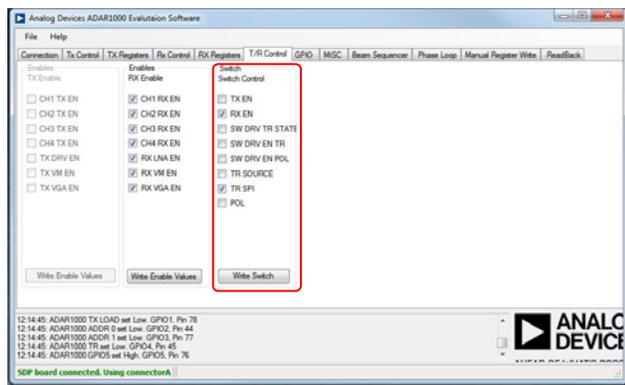


Figure 17. SPI Control, Receive Enable, and Receive Mode

Receive Gain Control

To set Receive Channel 1 to maximum gain, take the following steps:

1. Click the **RX Registers** tab (see Figure 18).
2. Select the **CH1 RX ATTN** check box to bypass the attenuator on Channel 1.
3. Set the **RX VGA CH1** value to 127 to set the VGA to maximum gain on Channel 1.
4. Click **Write Gain Values**.

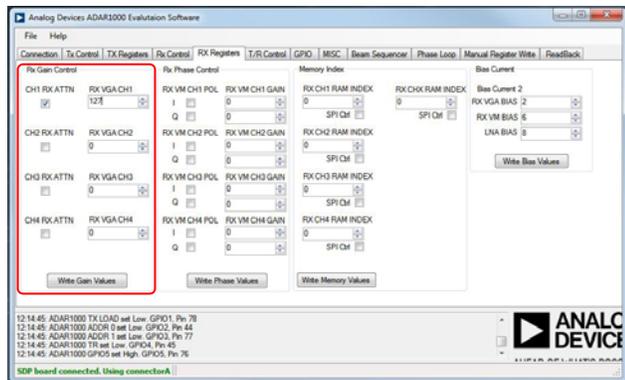


Figure 18. Setting Receive Channel 1 to Maximum Gain in Receive Gain Control with All Other Channels at Minimum Gain

Receive Phase Control

To set Receive Channel 1 to 45°, take the following steps:

1. Click the **RX Registers** tab (see Figure 19).
2. Select the inphase (**I**) and quadrature phase (**Q**) check boxes under **RX VM CH1 POL** to set the polarity bits so that the vector is in the first quadrant.
3. Set the **I** and **Q** values under **RX VM CH1 GAIN** to 22 for a resulting vector of 45°.
4. Click **Write Phase Values**.

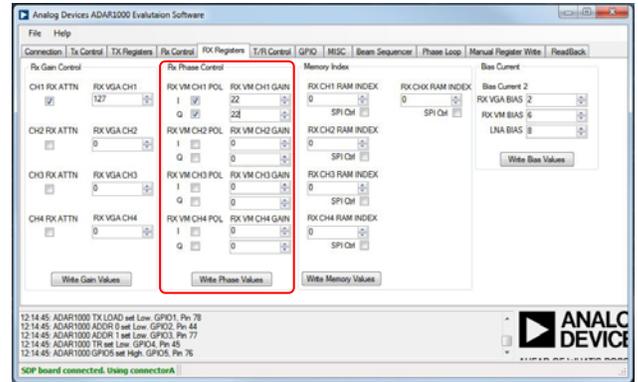


Figure 19. Setting Receive Channel 1 to Maximum Gain in Receive Phase Control with All Other Channels at Minimum Gain

Receive Load

For the gain and phase changes to take effect, a load receive override command must be given. To give this command, take the following steps:

1. Click the **MISC** tab (see Figure 20).
2. In the **Over Ride** section, click **LDRX OVR**.

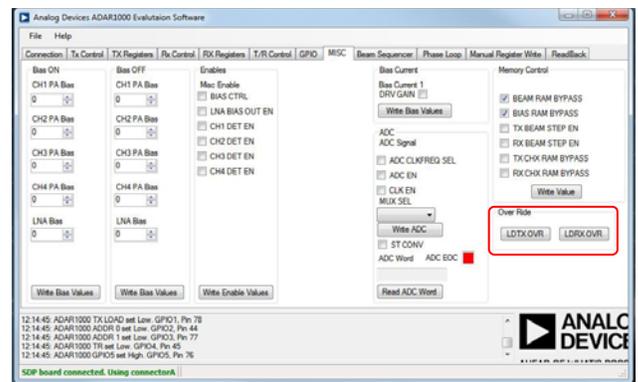


Figure 20. Load Receive Override

CONTROL USING THE MANUAL REGISTER WRITE

The ADAR1000 GUI allows several registers of data to be loaded quickly and efficiently in the **Load and Write** section under the **Manual Register Write** tab. When the user becomes familiar with the ADAR1000, this method of writing to the device saves a significant amount of time. The provided maximum gain and switch bias settings .txt files can be used, or the user can generate files containing user defined settings to control the ADAR1000.

To perform several writes that are stored in a .txt file, take the following steps:

1. Click the **Manual Register Write** tab (see Figure 21).
2. Click **Choose Input File**.
3. Navigate to where the settings files are located (see Figure 22).
4. Open the desired file (**Tx1_MaxG_45.txt**, for example).
5. The values in the file appear in the larger text box on the left side of the window, as shown in Figure 23.
6. Click **Write All** to load all values via the SPI.

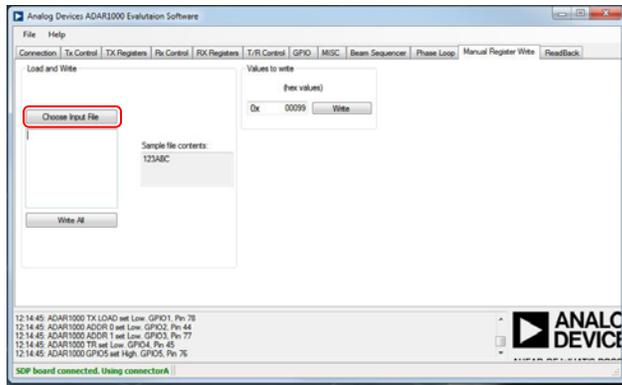


Figure 21. Manual Register Write Tab

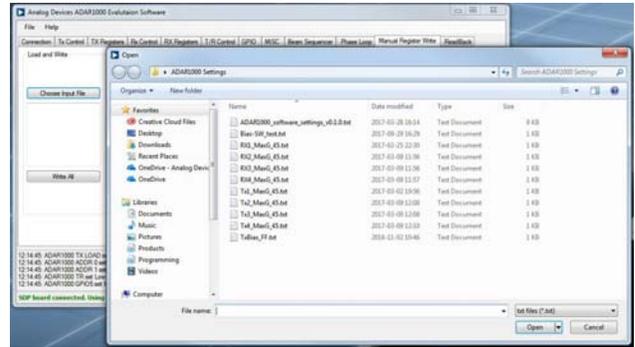


Figure 22. Choose Settings File

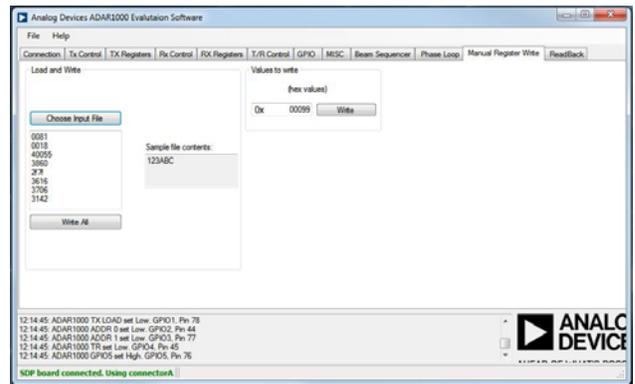


Figure 23. Values to Write

QUICK TEST PROCEDURE

To use the ADAR1000-EVALZ to test and evaluate the [ADAR1000](#), take the following steps:

1. Plug the SDP adapter into the P5 connector on the ADAR1000-EVALZ.
2. Connect the 3.3 V and -5 V power supplies to the corresponding banana jacks on the ADAR1000-EVALZ.
3. Use a USB cable to connect the SDP adapter to the PC that has the ADAR1000-EVALZ evaluation software downloaded.
4. Connect one port of the network analyzer to the RF_IO connector and another port to the RX1 input connector.
5. Use the **Start** menu to run the ADAR1000-EVALZ evaluation software (see the Evaluation Board Software Installation section for more information), as shown in Figure 24.

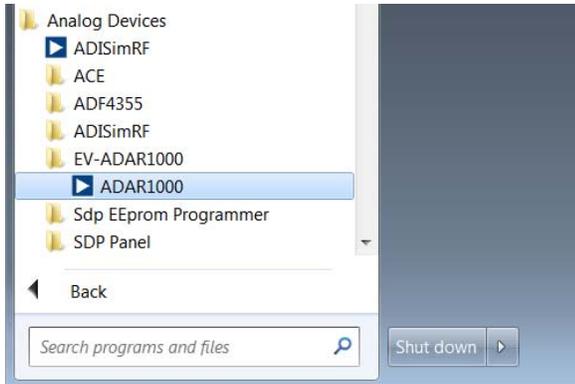


Figure 24. Run Control Software from the **Start** Menu

6. After the ADAR1000-EVALZ evaluation software starts up, click the **Connection** tab and then click **Connect** (see Figure 27).
7. Ensure that **SDP board connected** appears on the status bar.
8. For receive mode operation, click the **Manual Register Write** tab (see Figure 21) and click **Choose Input File** to choose the **RX1_MaxG_45.txt** file for the register values. Note that this file (and the similar settings files) does not change any of the GUI settings. The file only writes data to the [ADAR1000](#).
9. Click **Write All** to send the register values to the [ADAR1000](#). Receive Channel 1 is now turned on at full gain.
10. Measure the gain and return loss on the network analyzer. A typical response is shown in Figure 25.

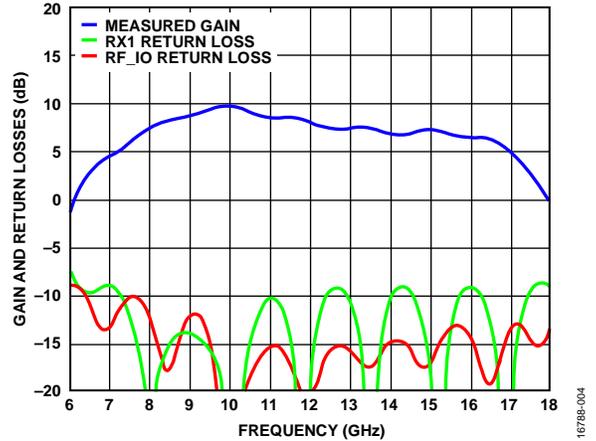


Figure 25. Receive Mode Gain and Return Loss Measurement Results

11. For transmit mode operation, disconnect the RX1 port and connect to the TX1 output connector.
12. Click **Choose Input File** to choose the **TX1_MaxG_45.txt** file for the register values.
13. Click **Write All** to send the register values to the [ADAR1000](#). Transmit Channel 1 is now turned on at full gain.
14. Measure the gain and return loss on the network analyzer. A typical response is shown in Figure 26.

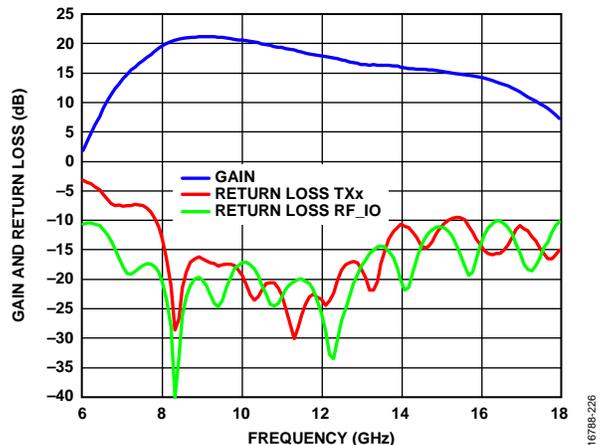


Figure 26. Transmit Mode Gain and Return Loss

DETAILED SOFTWARE DESCRIPTION

The ADAR1000-EVALZ evaluation software is organized as a number of tabs. Each tab contains a different set of functions to control the ADAR1000-EVALZ. Beneath the content area of the current tab, a log of each hardware control instruction that the software sends to the ADAR1000-EVALZ is shown near the bottom of the window. The last line of the window displays the status of the connection between the ADAR1000-EVALZ evaluation software and the ADAR1000-EVALZ hardware.

CONNECTION TAB

The **Connection** tab displays the two different SDP adapters that can be used to provide the USB interface to the ADAR1000-EVALZ (see Figure 27).

Click the **Connect** button to initialize communication between the ADAR1000-EVALZ evaluation software and the ADAR1000-EVALZ. When communication is established, the **SDP board connected** message displays on the status line at the bottom of the window.

The **ADDR0** and **ADDR1** check boxes in Figure 27 allow the setting or clearing of the two corresponding address bits, AD0 and AD1, on the **ADAR1000** device. These two bits determine which of the four ADAR1000-EVALZ boards on the same serial bus responds to programming information from the bus.

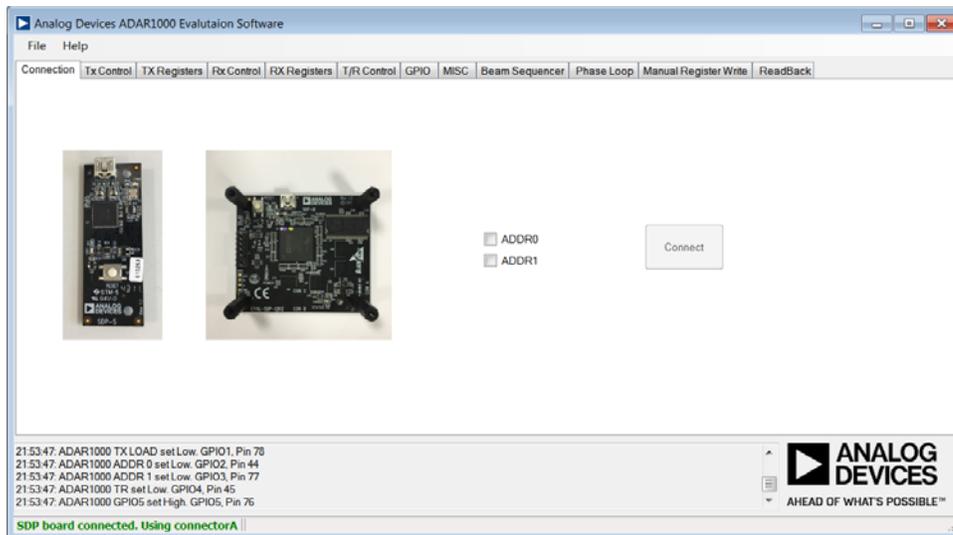


Figure 27. **Connection** Tab

Tx CONTROL TAB

The Tx Control tab (see Figure 28) allows the user to set the gain and phase of each of the four transmit channels.

To use the Tx Control tab, take the following steps:

1. Click **Tx Initialise**.
2. Select the **Attenuation** check box for each channel to add or remove the 15 dB step attenuation.
3. Adjust the **Gain Index** and **Phase Angle** (°) settings of each channel using the corresponding dropdown menus.
4. When adjustments are made, click **Load All** to write the settings to the device registers.

TX REGISTERS TAB

The TX Registers tab provides control for all transmit function registers in the device (see Figure 29).

In the Tx Gain Control section, set the gain register for each transmit channel.

In the Tx Phase Control section, set the I and Q gain registers, as well as polarity bits for each channel in the corresponding vector modulator (VM).

In the Memory Index section, if the SPI Ctrl check box is selected, the beam position settings for the corresponding channel are recalled from memory into the channel work registers, according to the value (the memory address) in the TX CH1 RAM INDEX to TX CH4 RAM INDEX fields for each channel. If the SPI Ctrl check box under TX CHX RAM INDEX is selected, data for all four channels are pulled according to the value in the TX CHX RAM INDEX field.

In the Bias Current section, choose a bias setting for each of the three transmit stages (the settings are common to all four transmit channels).

Click **Write Gain Values**, **Write Phase Values**, and **Write Memory Values** to send the corresponding bias register setting to the ADAR1000-EVALZ.

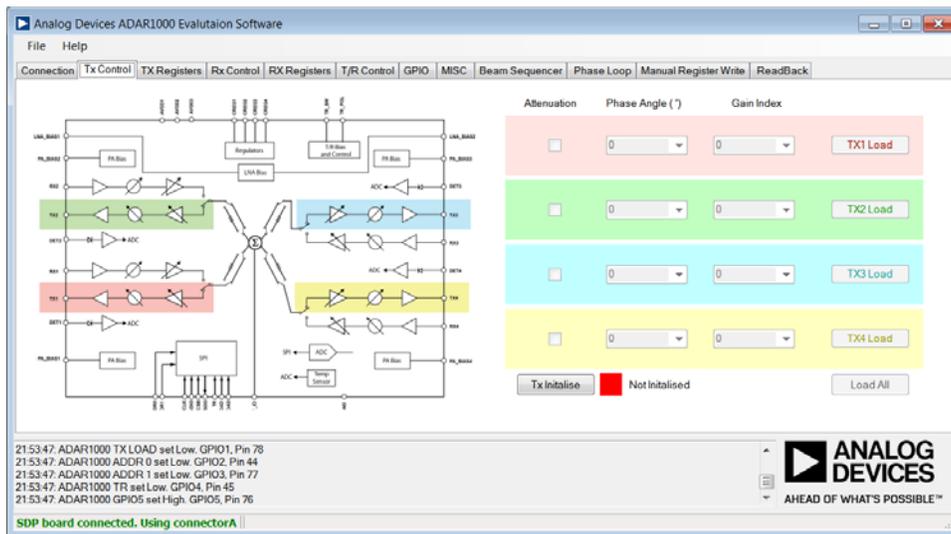


Figure 28. Tx Control Tab

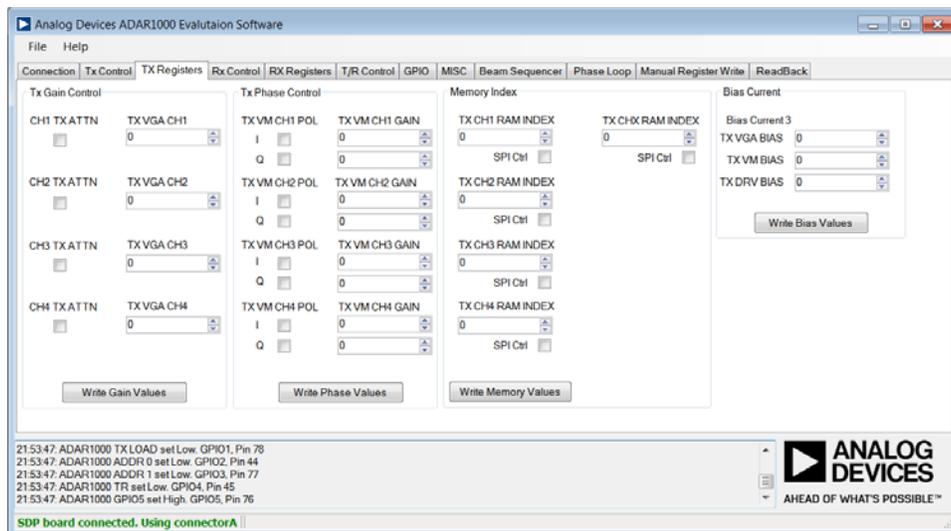


Figure 29. TX Registers Tab

Rx CONTROL TAB

The **Rx Control** tab (see Figure 30) allows setting the gain and phase of each of the four receive channels.

To use the **Rx Control** tab, take the following steps:

1. Click **Rx Initialise**.
2. Select the **Attenuation** check box for each channel to add or remove the 15 dB step attenuation.
3. Adjust the **Gain Index** and **Phase Angle (°)** settings of each channel using the corresponding dropdown menus.
4. When adjustments are made, click **Load All** to write the settings to the device registers.

RX REGISTERS TAB

The **RX Registers** tab provides control for all receive function registers in the device (see Figure 31).

In the **Rx Gain Control** section, set the gain register for each receive channel.

In the **Rx Phase Control** section, set the **I** and **Q** gain registers for each channel in the corresponding VM.

In the **Memory Index** section, if the **SPI Ctrl** check box is selected, the beam position settings for the corresponding channel are recalled from memory into the channel work registers according to the value (the memory address) in the **RX CH1 RAM INDEX** to **RX CH4 RAM INDEX** field for each channel. If the **SPI Ctrl** check box under **RX CHX RAM INDEX** is selected, data for all four channels are pulled according to the value in the **RX CHX RAM INDEX** field.

In the **Bias Current** section, choose a bias setting for each of the three receive stages (the settings are common to all four receive channels).

Click **Write Gain Values**, **Write Phase Values**, and **Write Memory Values** to send the corresponding register setting to the ADAR1000-EVALZ.

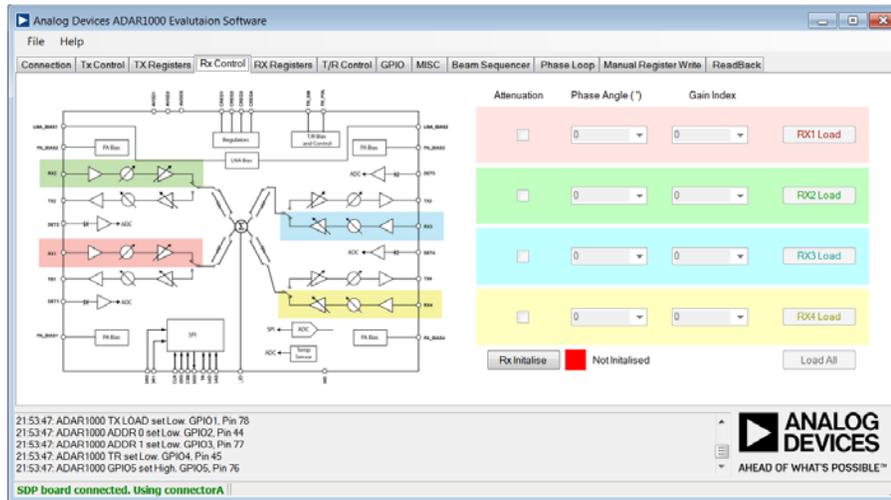


Figure 30. Rx Control Tab

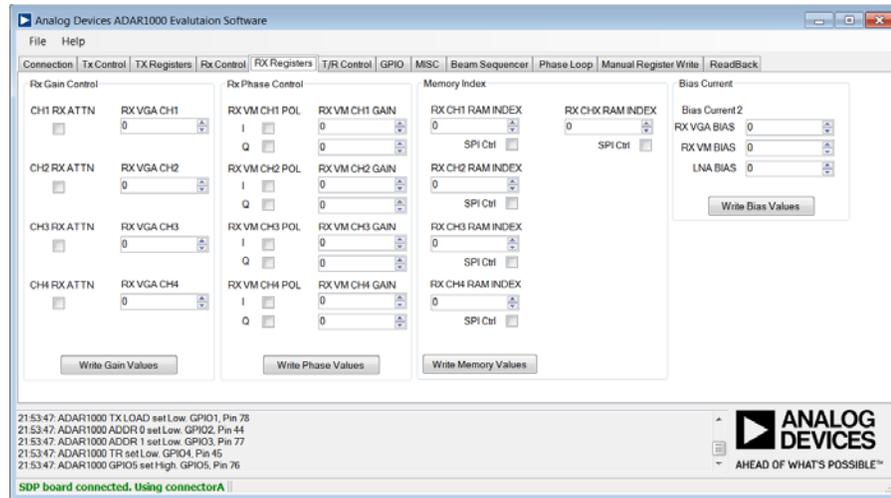


Figure 31. RX Registers Tab

T/R CONTROL TAB

The **T/R Control** tab controls the enabling of the transmit and receive channels (see Figure 32).

If the **TX EN** check box (under **Switch Control**) is selected, the transmit enable functions are enabled and the receive enable functions are disabled.

If the **RX EN** check box (under **Switch Control**) is selected, the receive enable functions are enabled and the transmit enable functions are disabled.

When the check boxes are selected or cleared, click **Write Enable Values** or **Write Switch Values** in each section to write the register settings to the ADAR1000-EVALZ.

GPIO TAB

In the **GPIO** tab (see Figure 33), select the correct check boxes to set the corresponding digital control signals on the ADAR1000-EVALZ to Logic 1 (selected) or Logic 0 (cleared).

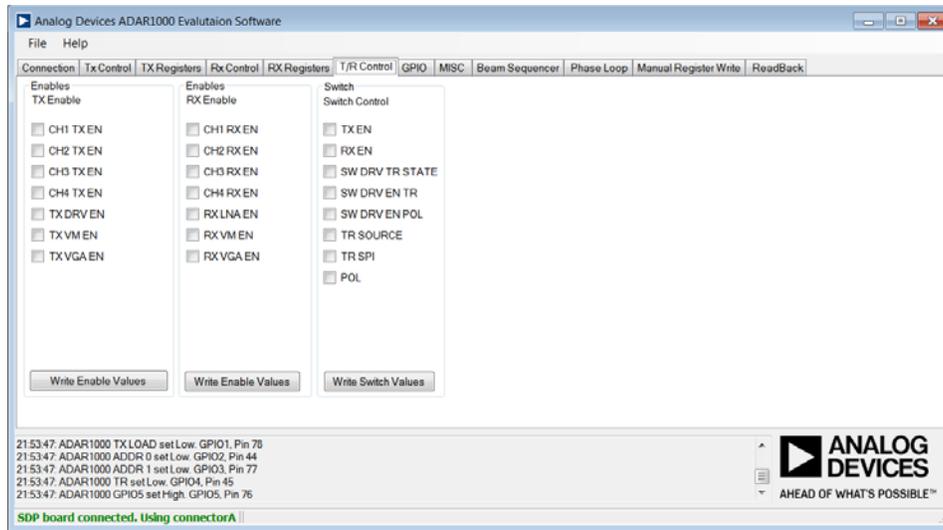


Figure 32. T/R Control Tab

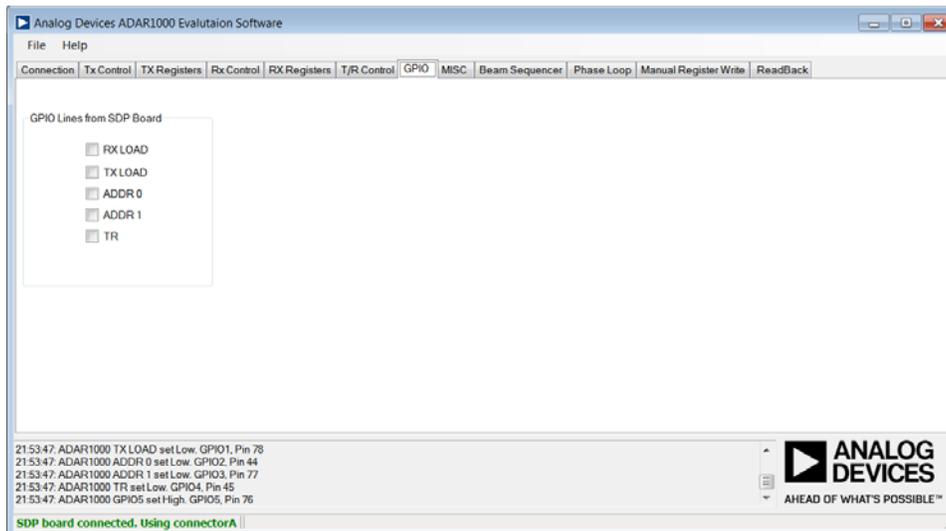


Figure 33. GPIO Tab

MISC TAB

In the **MISC** tab, configuration of miscellaneous functions is available (see Figure 34).

Two sets of registers are on the **ADAR1000** device to control the LNA and PA bias outputs and to set the DACs when the corresponding bias outputs are in the on and off states. The register values can be entered in the **Bias ON** and **Bias OFF** sections. Each set of register values is transferred to the ADAR1000-EVALZ when the respective **Write Bias Values** buttons are clicked.

Under the **Enables** section, if the **BIAS CTRL** check box is cleared, the bias digital-to-analog converter (DAC) outputs use the **Bias ON** register values only.

If the **BIAS CTRL** check box is selected while the device is in receive mode, the PA DACs use the **Bias OFF** register values,

and the LNA DAC uses the **Bias ON** register value. If the check box is selected while the device is in transmit mode, the opposite is true, and the PA DACs use the **Bias ON** register values, and the LNA DAC uses the **Bias OFF** register values.

In the **ADC** section, use the **MUX SEL** dropdown menu to choose the temperature sensor or the power detector, one through four, for analog to digital conversion.

Select **ADC EN**, **CLK EN**, and **ST CONV** and then click **Write ADC Values** to initiate analog to digital conversion.

Click **Read ADC Word** to access the conversion result.

The **Memory Control** section allows setting or clearing the corresponding bits in Register 0x038 for various memory control functions.

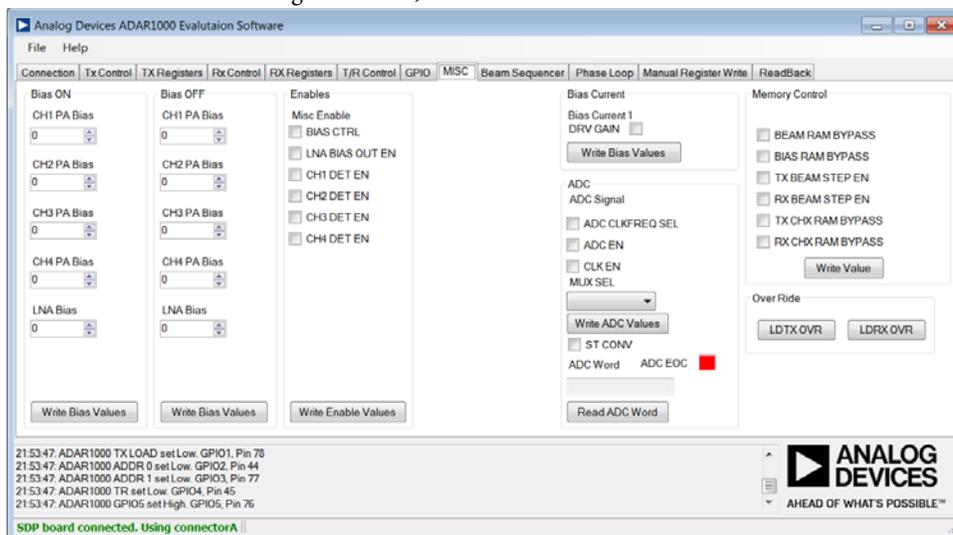


Figure 34. **MISC** Tab

BEAM SEQUENCER TAB

The **Beam Sequencer** tab (see Figure 35) contains a script to automatically step through a range of memory locations, each of which contains the gain and phase setting of all four transmit or receive channels in the device.

Click **Select File** to choose a user file containing a list of memory locations and values, and click **Load File** to load values into beam memory. Each line of the beam position file contains two values separated by a comma. The first value is the decimal equivalent value, and the second value is the hexadecimal value. For the hexadecimal value string, the memory address is the four most significant digits, and the data for each memory location is the two least significant digits. Typical entries in a beam position file include the following:

- 1573119, 0x1800FF
- 1573174, 0x180136
- 1573429, 0x180235

The starting and ending memory locations (**Start Point** and **End Point**, respectively), as well as the time delay between steps (**Time Delay (ms)**), is entered into the corresponding fields. The stepping operation is controlled by **Start** and **Stop**.

PHASE LOOP TAB

The **Phase Loop** tab (see Figure 36) provides control to increase the phase setting of a channel with a predefined step size (**Phase Step**) while dwelling at each step for a specified time (**Dwell Time (ms)**).

The **ADI Logo Loop** section moves the phase in a triangular manner around the circle of a polar plot.

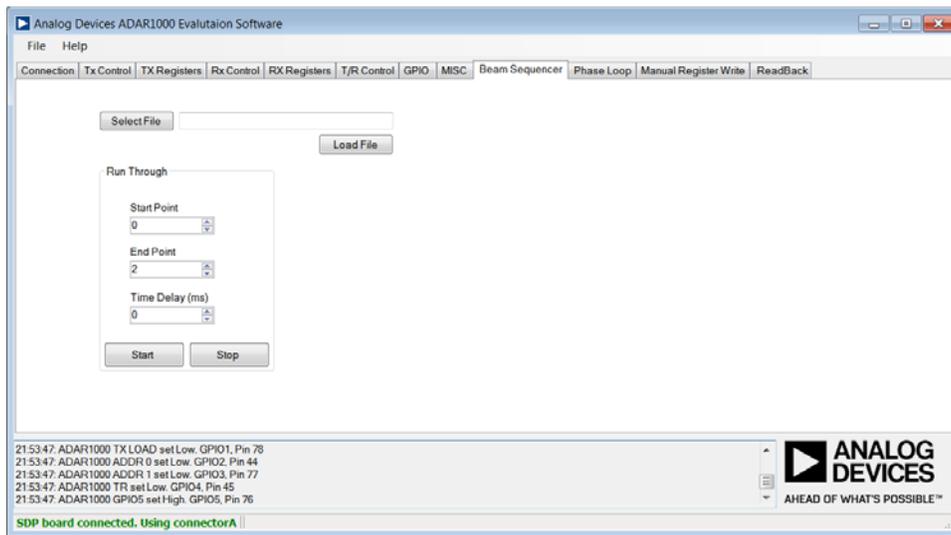


Figure 35. Beam Sequencer Tab

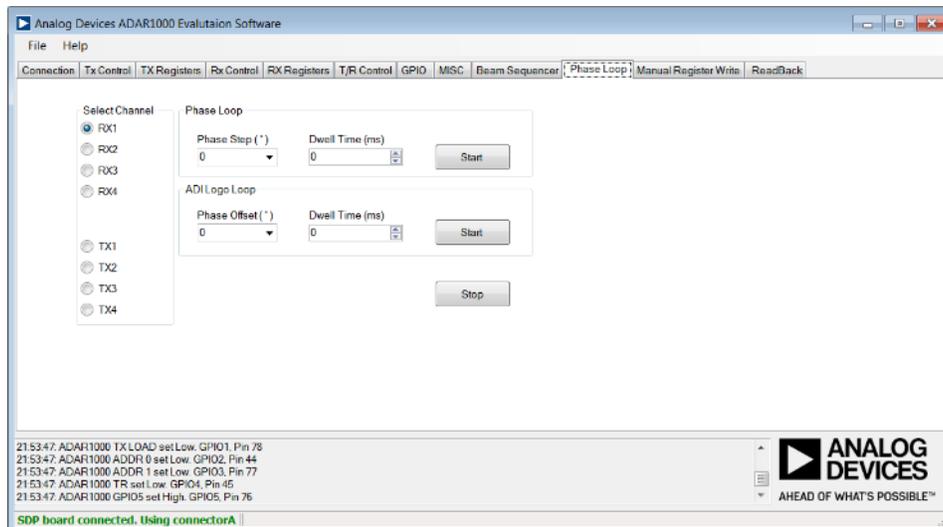


Figure 36. Phase Loop Tab

MANUAL REGISTER WRITE TAB

The **Manual Register Write** tab (see Figure 37) allows manual writes to the **ADAR1000** registers, either individually (**Values to write**) or grouped (**Load and Write**). In the **Load and Write** section, click **Choose Input File** to load a list of register writes from a file or paste one into the field directly. Click **Write All** to send the list to the ADAR1000-EVALZ.

When the device is initially powered up, enter 00099 into the **Values to write** section. Entering 00099 performs a full register reset and enables the 4-wire SPI SDO function.

READBACK TAB

The **ReadBack** tab allows direct writing and reading of the content of a register (see Figure 38).

Click **Manual Write** to write a string of hexadecimal digits containing the address and data of a register into the register.

Enter the register address in the **Register** field and click **Manual Read** for the content of the register to display in the **Data** field.

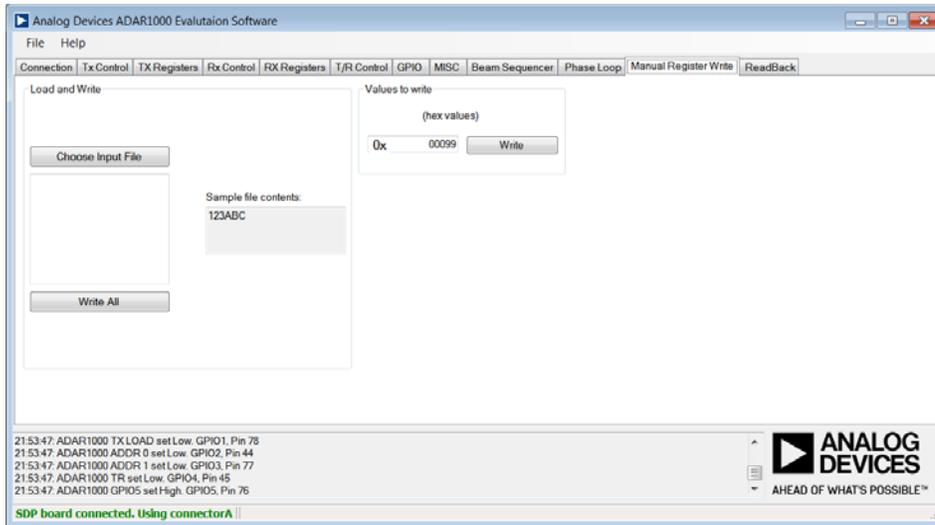


Figure 37. Manual Register Write Tab

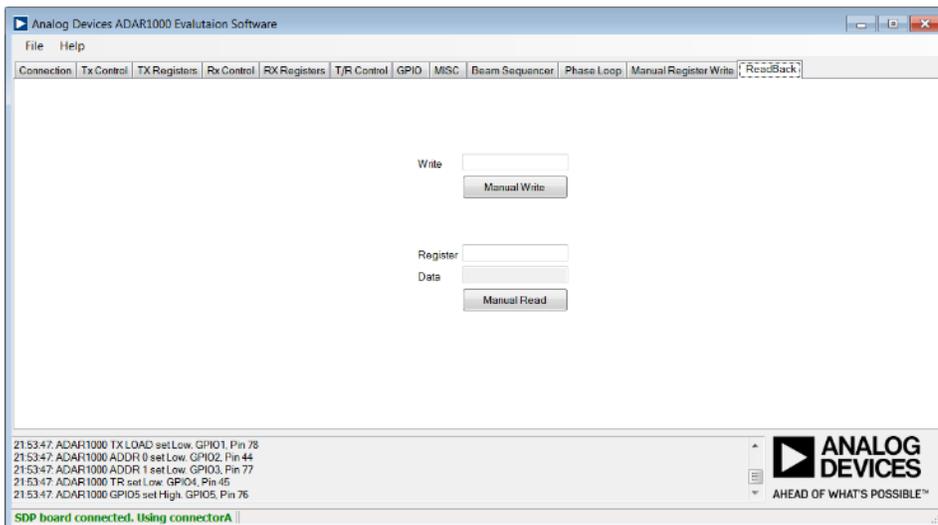
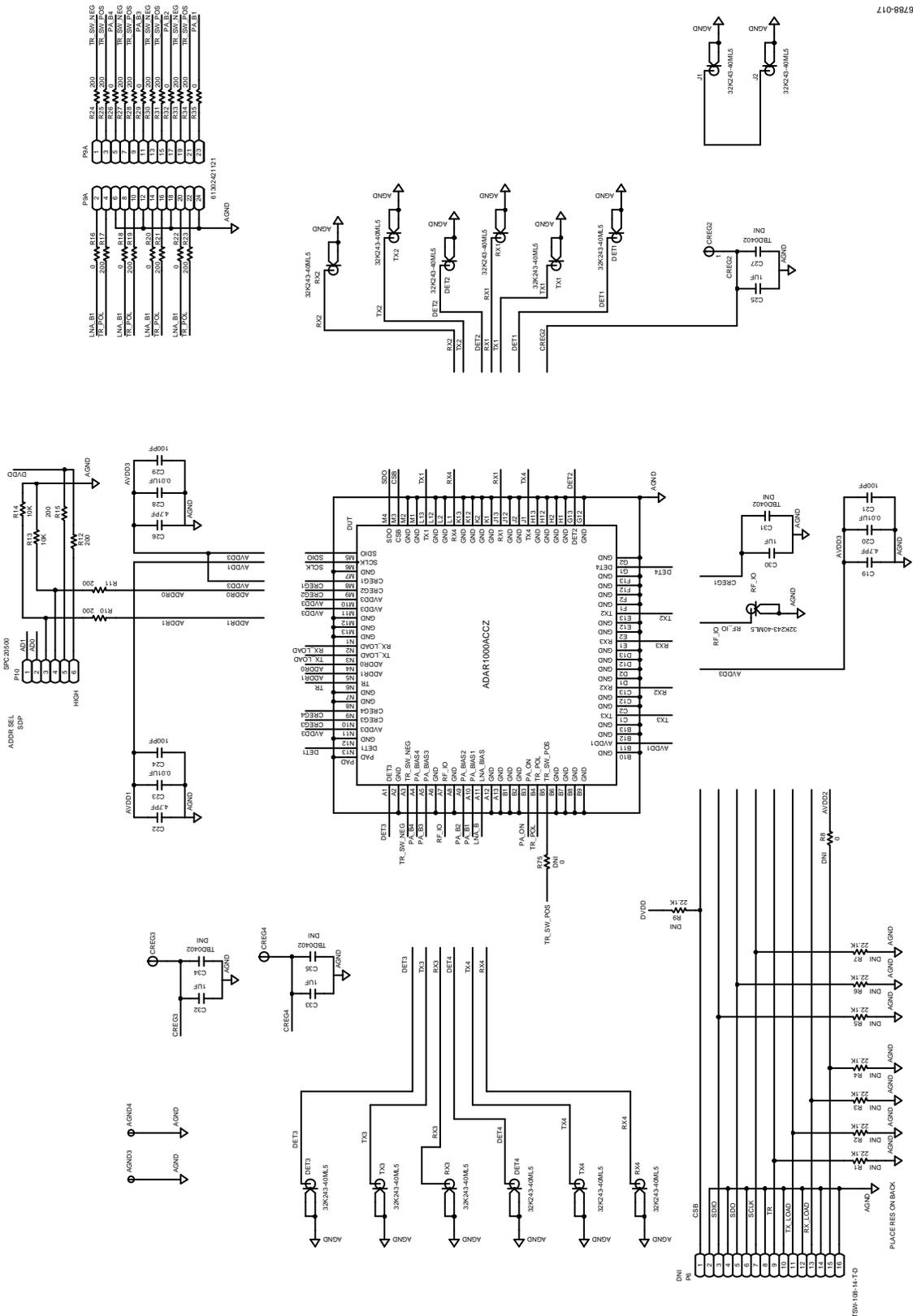


Figure 38. ReadBack Tab

EVALUATION BOARD SCHEMATICS AND ARTWORK



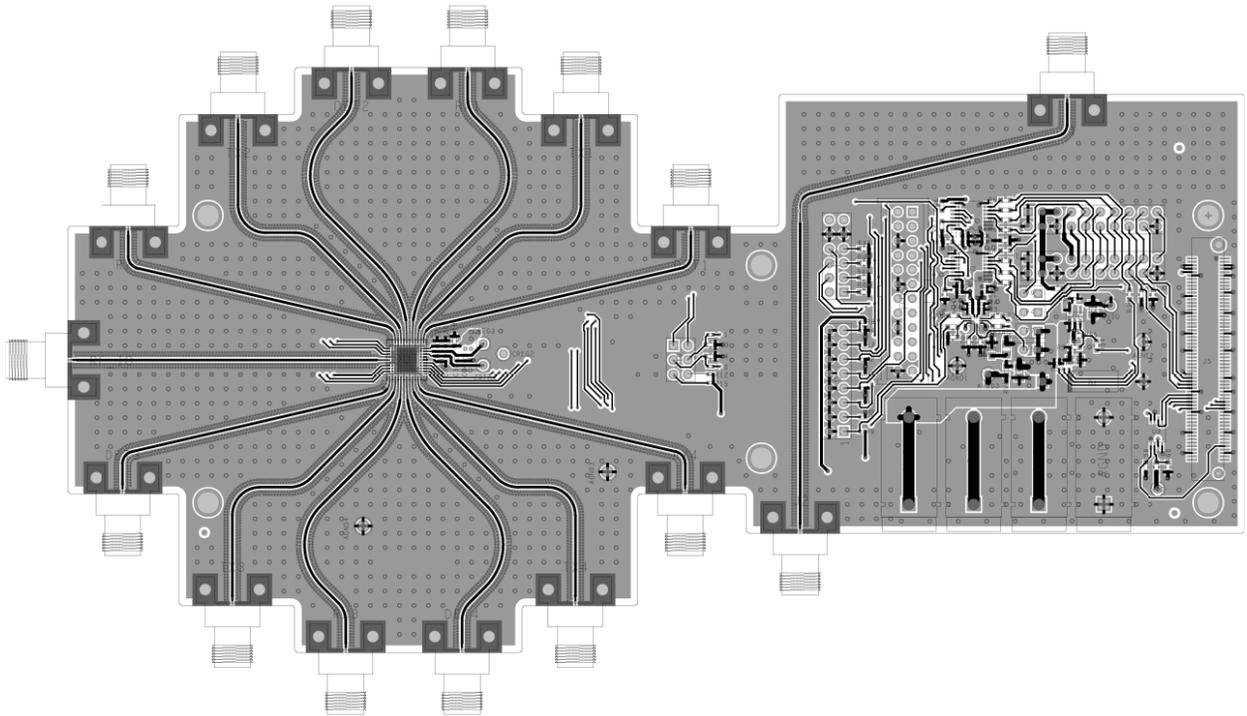


Figure 41. Layer 1 (Component Side)

16788-019

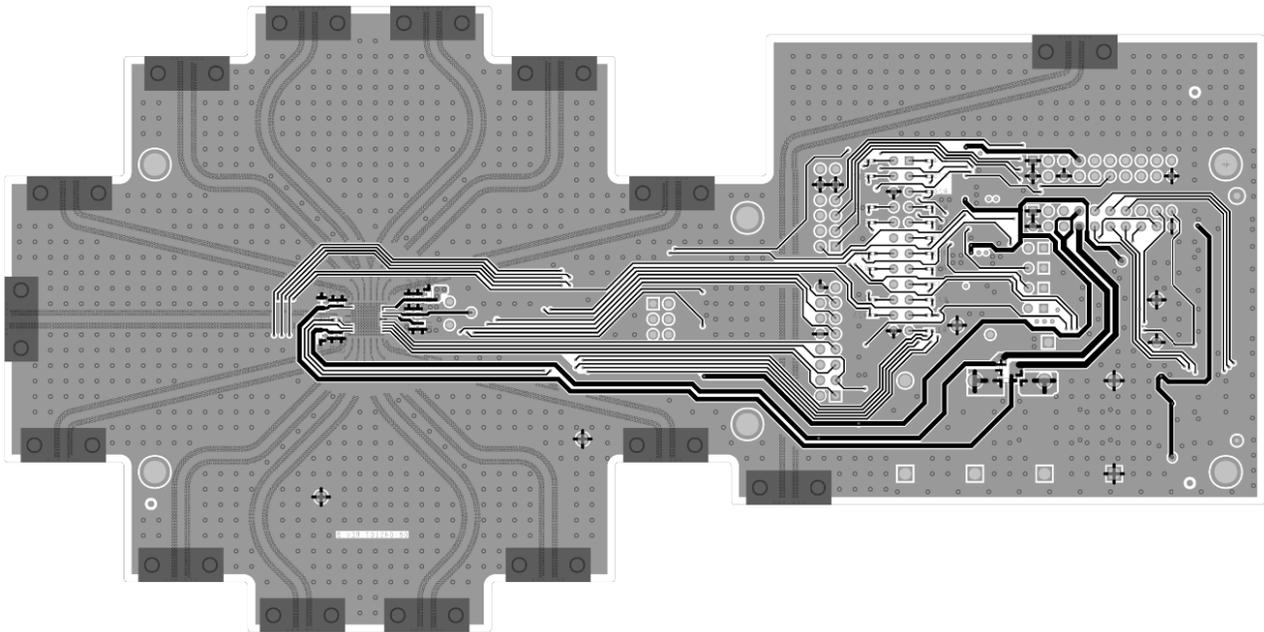


Figure 42. Layer 4 (Bottom Side)

16788-020

NOTES

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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