

## Evaluation Board for the **AD5232** Digital Potentiometer

### FEATURES

- Full featured evaluation board used in conjunction with low voltage digiPOT motherboard (EVAL-MB-LV-SDZ)
- Multiple test circuits
- Multiple ac/dc input signals
- PC control via a separately purchased system demonstration platform (SDP-B or SDP-S)
- PC software for control

### EVALUATION KIT CONTENTS

- EVAL-AD5232DBZ** evaluation board
- EVAL-MB-LV-SDZ motherboard
- CD that includes
  - Self-installing software that allows users to control the board and exercise all functions of the device
  - Electronic version of the **AD5232** data sheet
  - Electronic version of the **EVAL-AD5232DBZ** user guide

### GENERAL DESCRIPTION

This user guide describes the evaluation boards for evaluating the **AD5232**, a single-channel, 256-position, SPI-compatible digital potentiometer.

The **AD5232** supports single-supply 2.7 V to 5.5 V operation, making the device suitable for battery-powered applications and many applications requiring superior low temperature coefficient performance.

In addition, the **AD5232** uses a versatile SPI-compatible serial interface that operates in fast mode, allowing speeds of up to 50 MHz. This interface can be used to read back the wiper register.

The **EVAL-AD5232DBZ** daughter board and the EVAL-MB-LV-SDZ motherboard can operate in single-supply mode and incorporate an internal power supply from the USB.

Complete specifications for the **AD5232** can be found in the **AD5232** data sheet, which is available from [www.analog.com](http://www.analog.com) and should be consulted in conjunction with this user guide when using the evaluation board.

### PHOTOGRAPH OF **EVAL-AD5232DBZ** WITH MOTHERBOARD AND SDP-B

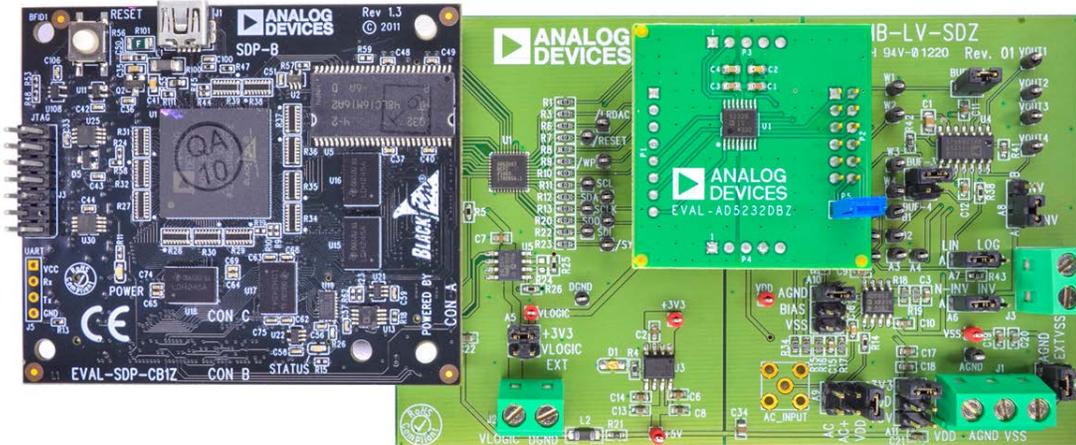


Figure 1. Digital Picture of Evaluation Board with Low Voltage DigiPOT Motherboard and System Demonstration Platform

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**REVISION HISTORY**

5/14—Revision 0: Initial Version

## EVALUATION BOARD HARDWARE

### POWER SUPPLIES

The EVAL-MB-LV-SDZ supports using single power supplies.

The evaluation board can be powered either from the SDP port or externally by the J1 and J2 connectors, as described in Table 1.

All supplies are decoupled to ground using 10  $\mu$ F tantalum and 0.1  $\mu$ F ceramic capacitors.

### LINK OPTIONS

Several link and switch options are incorporated on the EVAL-MB-LV-SDZ and [EVAL-AD5232DBZ](#) boards and must be set up before using the evaluation system. The functions of these link options are described in detail in Table 2 through Table 5. By default, the evaluation system is set up to be controlled by a PC via the SDP board.

**Table 1. Connector Functions**

| Connector No. | Label  | Description                            | Voltage |          |
|---------------|--------|--|---------|----------|
|               |        |  | Min     | Max      |
| J1-1          | VDD    | Analog positive power supply, $V_{DD}$ | 2.7V    | 5.5V     |
| J1-2          | AGND   | Analog ground                          |         |          |
| J2-1          | VLOGIC | Digital supply                         | 2.7V    | $V_{DD}$ |
| J2-2          | DGND   | Digital ground                         |         |          |

**Table 2. Link Functions**

| Link No. | Power Supply | Options  | Default Position |
|----------|--------------|--|------------------|
| A5       | $V_{LOGIC}$  | Digital supply select options:<br>3.3 V (from the SDP board)<br>VLOGIC EXT (external supply from the J2 connector)                             | 3.3 V            |
| A11      | $V_{DD}$     | Positive power supply select options:<br>5 V (from the SDP board)<br>3.3 V (from the SDP board)<br>VDD (external supply from the J1 connector) | 3.3 V            |
| A12      | GND          | AGND   | AGND             |

**TEST CIRCUITS**

The EVAL-AD5232DBZ and EVAL-MB-LV-SDZ incorporate several test circuits to evaluate the performance of the AD5232.

**DAC**

The RDAC can be operated as a digital-to-analog converter (DAC), as shown in Figure 2.

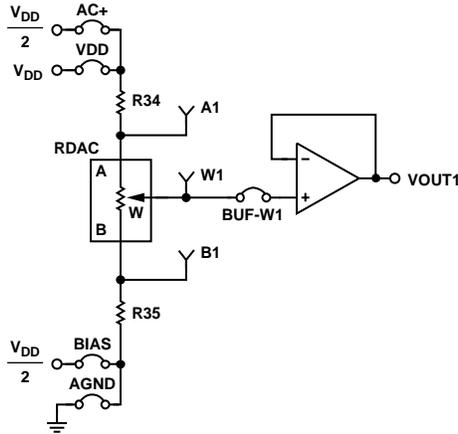


Figure 2. DAC

Table 4 shows the options available for the voltage references.

The output voltage is defined in Equation 1.

$$V_{OUT} = (V_A - V_B) \times \frac{RDAC}{256} \tag{1}$$

where:

- RDAC is the code loaded in the RDAC register.
- V<sub>A</sub> is the voltage applied to the A terminal (A9 link).
- V<sub>B</sub> is the voltage applied to the B terminal (A10 link).

However, by using the R34 and R35 external resistors, you can reduce the voltage of the voltage references. In this case, use the A1 and B1 test points to measure the voltage applied to the A and B terminals and recalculate V<sub>A</sub> and V<sub>B</sub> in Equation 1.

**AC Signal Attenuation**

The RDAC can be used to attenuate an ac signal, which must be provided externally using the AC\_INPUT connector, as shown in Figure 3.

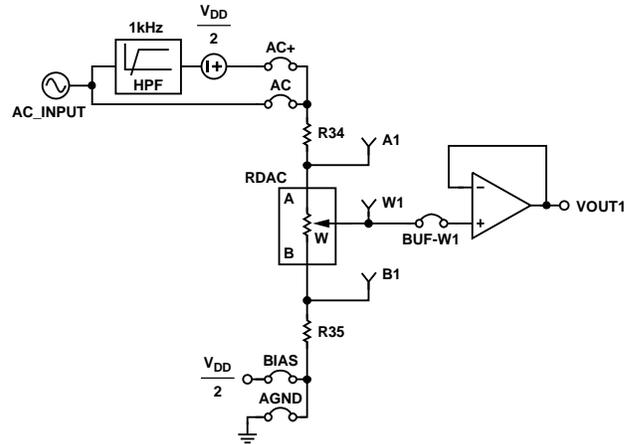


Figure 3. AC Signal Attenuator

Depending on the voltage supply rails and the dc offset voltage of the ac signal, various configurations can be used, as described in Table 3.

**Table 3. AC Signal Attenuation Link Options**

| Link | Options      | Conditions   |
|------|--------------|--|
| A9   | AC+          | No dc offset voltage.<br>AC signal is outside the voltage supply rails due to the dc offset voltage.<br>DC offset voltage ≠ V <sub>DD</sub> /2. <sup>1</sup> |
|      | AC           | All other conditions.  |
| A10  | BIAS<br>AGND | Use in conjunction with AC+ link. <sup>1</sup><br>All other conditions.  |

<sup>1</sup> Recommended to ensure optimal total harmonic distortion (THD) performance.

The signal attenuation is defined in Equation 2.

$$Attenuation \text{ (dB)} = 20 \times \log \left( \frac{R_{WB} + R_W}{R_{END-TO-END}} \right) \tag{2}$$

where:

- R<sub>WB</sub> is the resistance between the W and B terminals.
- R<sub>W</sub> is the wiper resistance.
- R<sub>END-TO-END</sub> is the end-to-end resistance value.

**Table 4. DAC Voltage References**

| Terminal | Link Settings                        |                                      | Description   |
|----------|--------------------------------------|--------------------------------------|---|
|          | Daughter Board                       | Motherboard                          |   |
| A1       | Hardwired to RDAC1 of daughter board | A9: AC+ position<br>A9: VDD position | Connects Terminal A1 to V <sub>DD</sub> /2<br>Connects Terminal A1 to V <sub>DD</sub> |
| W1       | Hardwired to RDAC1 of daughter board | BUF-W1: inserted                     | Connects Terminal W1 to an output buffer  |
| B1       | Hardwired to RDAC1 of daughter board | A10: BIAS position                   | Connects Terminal B1 to V <sub>DD</sub> /2  |
|          |                                      | A10: AGND position                   | Connects Terminal B1 to analog ground   |
|          | P5: inserted                         |                                      | Closes the feedback loop of the second op amp in the AD8618                           |

**Signal Amplifier**

The RDAC can be operated as an inverting or noninverting signal amplifier and can support linear or pseudologarithmic gain. Table 5 shows the available configurations.

The noninverting amplifier with linear gain is shown in Figure 4, and the gain is defined in Equation 3.

$$G = 1 + \frac{R_{WB}}{R_{38}} \tag{3}$$

where  $R_{WB}$  is the resistance between the W and B terminals.

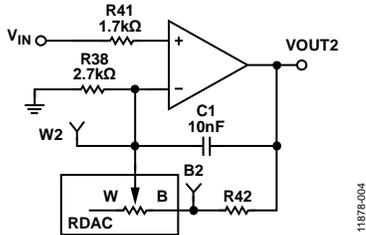


Figure 4. Noninverting Amplifier with Linear Gain

The noninverting amplifier with pseudologarithmic gain is shown in Figure 5, and the gain is defined in Equation 4.

$$G = 1 + \frac{R_{WB}}{R_{AW}} \tag{4}$$

where:

$R_{WB}$  is the resistance between the W and B terminals.  
 $R_{AW}$  is the resistance between the A and W terminals.

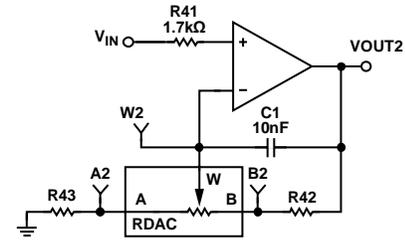


Figure 5. Noninverting Amplifier with Pseudologarithmic Gain

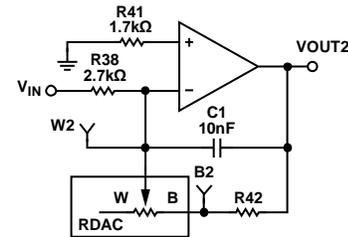
$R_{43}$  and  $R_{42}$  can be used to set the maximum and minimum gain limits.

The inverting amplifier with linear gain is shown in Figure 6, and the gain is defined in Equation 5.

$$G = -\frac{R_{WB}}{R_{38}} \tag{5}$$

where  $R_{WB}$  is the resistance between the W and B terminals.

Note that the input signal,  $V_{IN}$ , must be negative.



NOTES  
 1. THE INPUT SIGNAL,  $V_{IN}$ , MUST BE NEGATIVE.

Figure 6. Inverting Amplifier with Linear Gain

**Table 5. Amplifier Selection Link Settings**

| Amplifier    | Gain              | Link Settings   |  | $V_{IN}$ Range   |
|--------------|-------------------|---|--|------------------|
|              |                   | Daughter Board  | Motherboard  |                  |
| Noninverting | Linear            | Hardwired to RDAC2 of daughter board,<br>P5: not inserted | A7: LIN position,<br>A6: N-INV position,<br>A8: N-INV position | 0 V to $V_{DD}$  |
|              | Pseudologarithmic | Hardwired to RDAC2 of daughter board,<br>P5: not inserted | A7: LOG position,<br>A6: N-INV position,<br>A8: N-INV position | 0 V to $V_{DD}$  |
| Inverting    | Linear            | Hardwired to RDAC2 of daughter board,<br>P5: not inserted | A7: LIN position,<br>A6: INV position,<br>A8: INV position     | $-V_{DD}$ to 0 V |

## EVALUATION BOARD SOFTWARE

### INSTALLING THE SOFTWARE

The [EVAL-AD5232DBZ](#) kit includes evaluation board software provided on a CD. The software is compatible with Windows® XP, Windows Vista, and Windows 7 (both 32-bit and 64-bit versions).

Install the software before connecting the [SDP board](#) to the USB port of the PC to ensure that the SDP board is recognized when it is connected to the PC.

1. Start the Windows operating system and insert the CD.
2. The installation software opens automatically. If it does not, run the **setup.exe** file from the CD.
3. After the installation is complete, power up the evaluation board as described in the Power Supplies section.
4. Connect the [EVAL-AD5232DBZ](#) and EVAL-MB-LV-SDZ to the SDP board and the SDP board to the PC.
5. When the software detects the evaluation board, follow the instructions that appear to finalize the installation.

### RUNNING THE SOFTWARE

To run the program, do the following:

1. Click **Start > All Programs > Analog Devices > AD5232 > AD5232 Eval Board**. (To uninstall the program, click **Start > Control Panel > Add or Remove Programs > AD5232 Eval Board**.)

2. If the SDP board is not connected to the USB port when the software is launched, a connectivity error displays (see Figure 7). If a connectivity error is displayed, connect the evaluation board to the USB port of the PC and wait a few seconds, and then click **Rescan** and follow the instructions that appear on-screen.

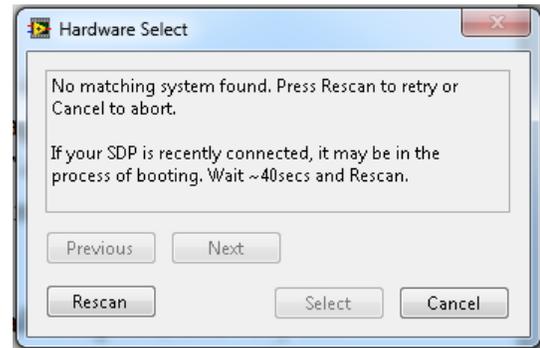


Figure 7. Pop-Up Window Error

The main window of the [EVAL-AD5232DBZ](#) software then opens, as shown in Figure 8.

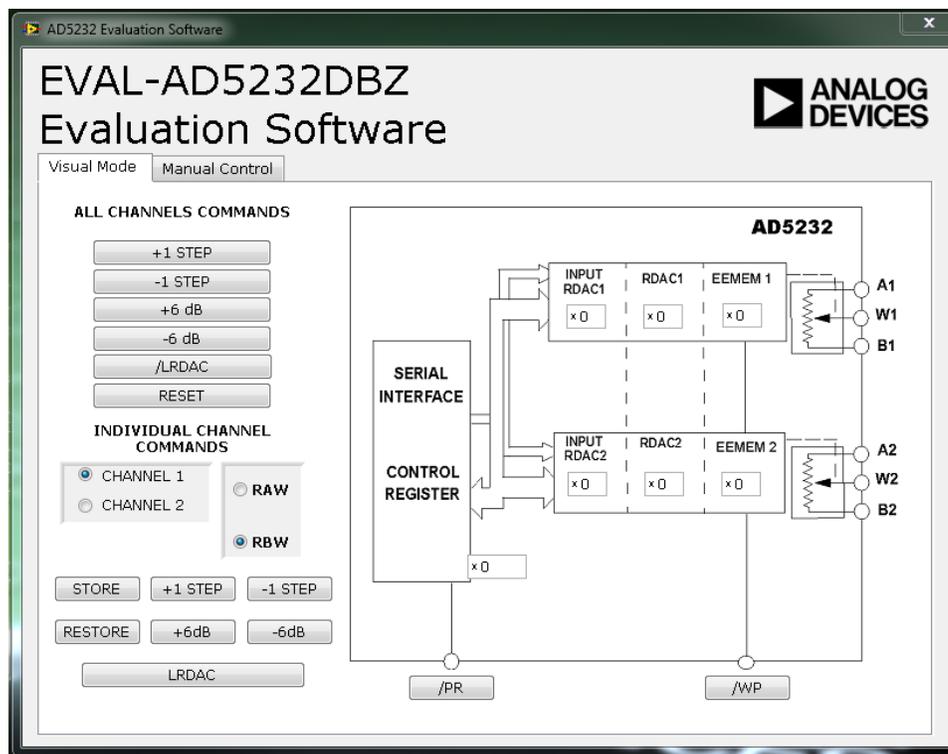


Figure 8. [EVAL-AD5232DBZ](#) Software Main Window, Visual Mode Tab

**OPERATING THE SOFTWARE**

The main window of the [EVAL-AD5232DBZ](#) software is divided into two tabs: **Visual Mode** and **Manual Control**.

**Visual Mode Tab**

The **Visual Mode** tab, as shown in Figure 8, is divided into two sections, with a block diagram on the right and command buttons on the left.

The block diagram allows updating the control register status. Each register value can easily be updated by changing the value in its respective block within the diagram.

**Manual Control Tab**

The **Manual Control** tab, as shown in Figure 9, allows customizing an SPI data-word by manually switching each serial data-word (D7 to D0) from 0 to 1 or from 1 to 0, as desired, and then clicking **SEND DATA**.

Exiting the window closes the program.

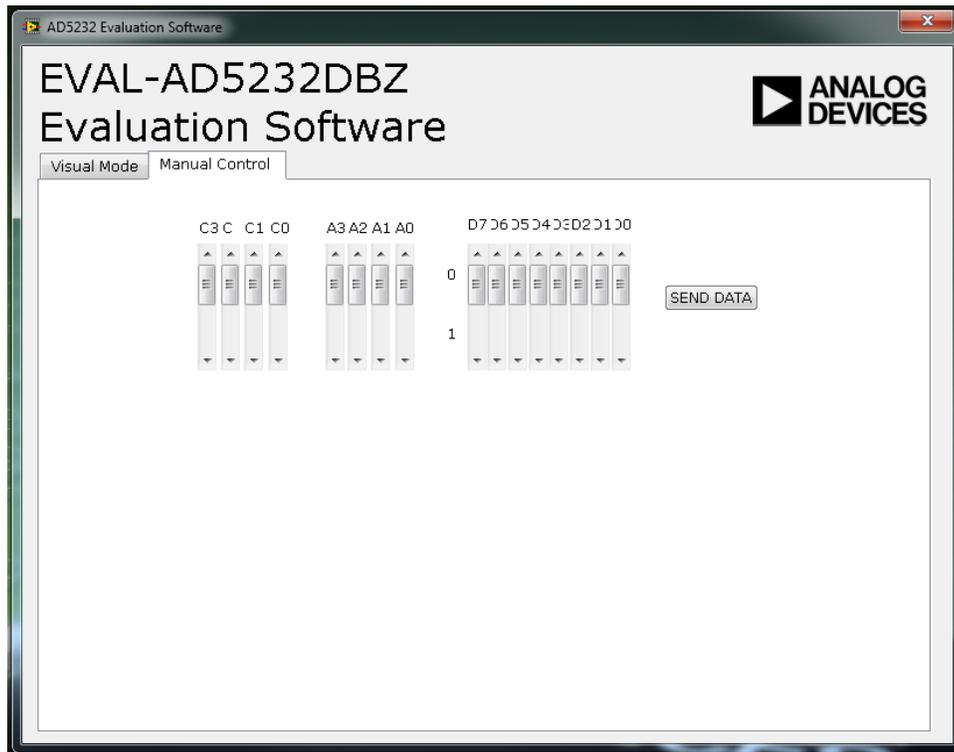
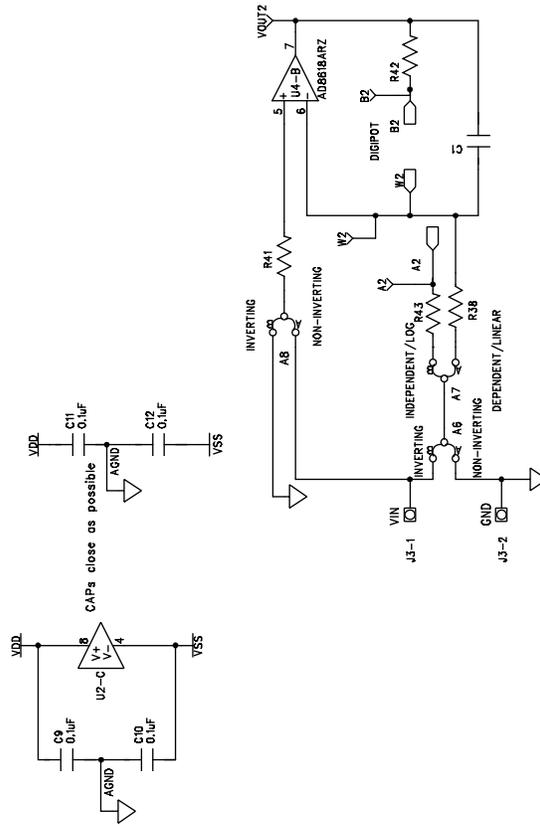
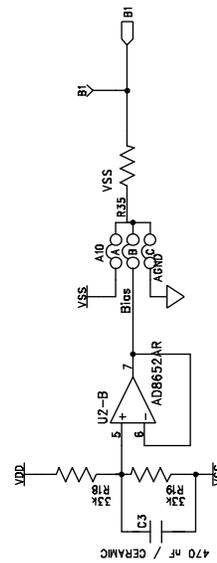
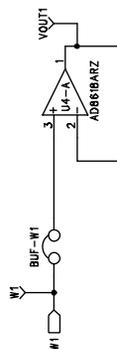
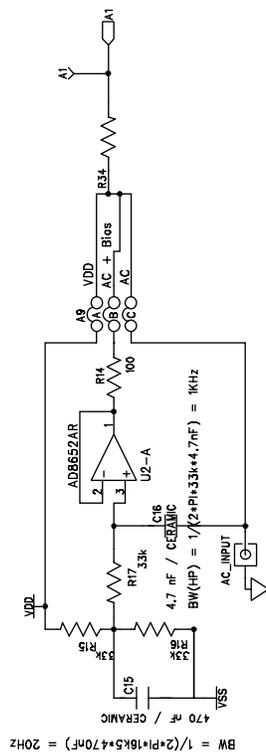


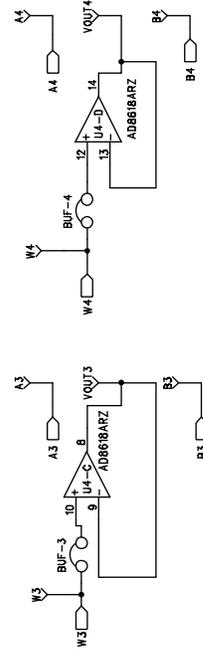
Figure 9. [EVAL-AD5232DBZ](#) Software Main Window, Manual Control Tab



DAC + FLOATING DAC + BW



INVERTING AND NON-INVERTING WITH LINEAR AND PSEUDO-LOG GAIN



11878-011

Figure 11. Schematic of Test Circuits

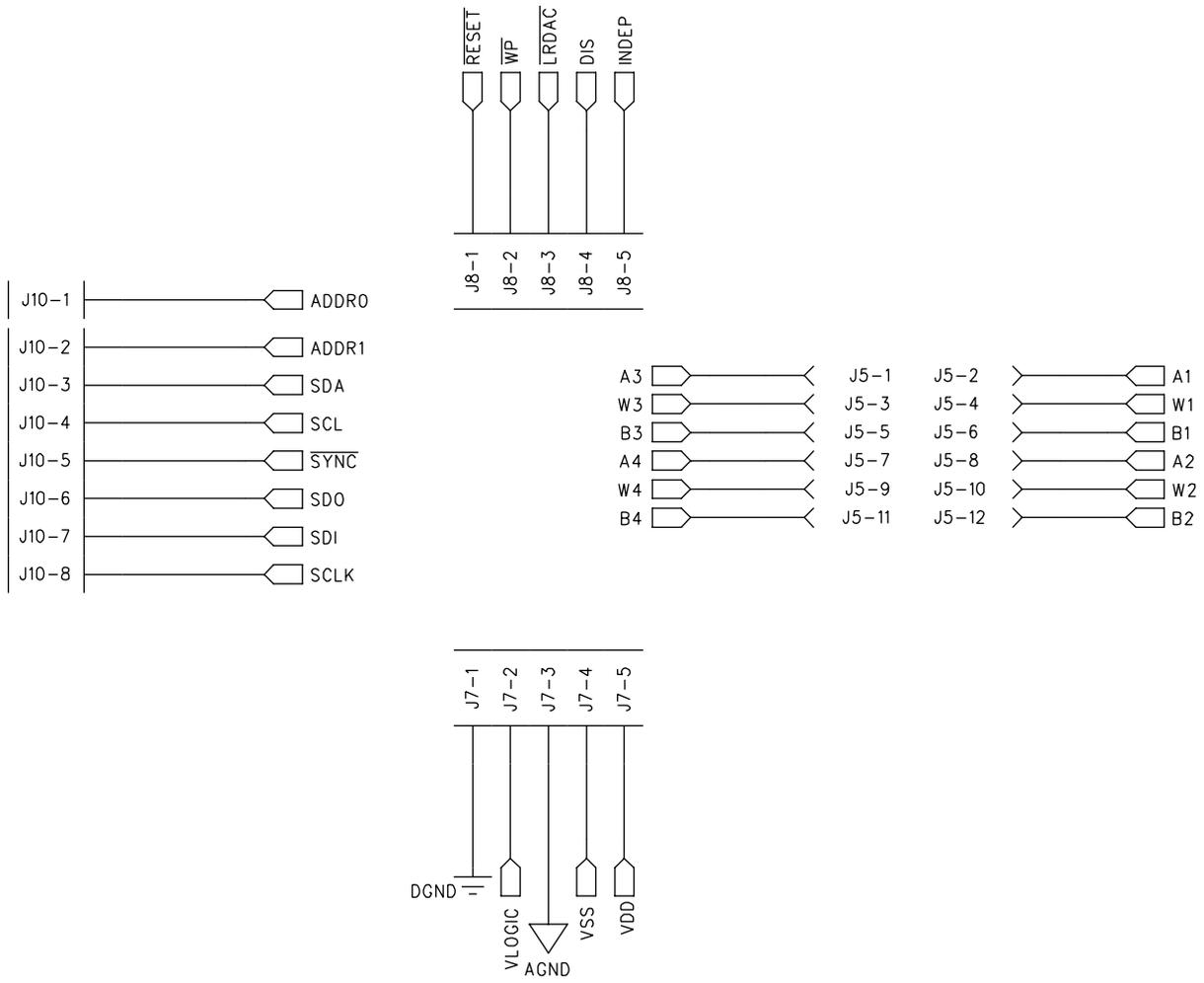


Figure 12. Schematic of Connectors to Daughter Board

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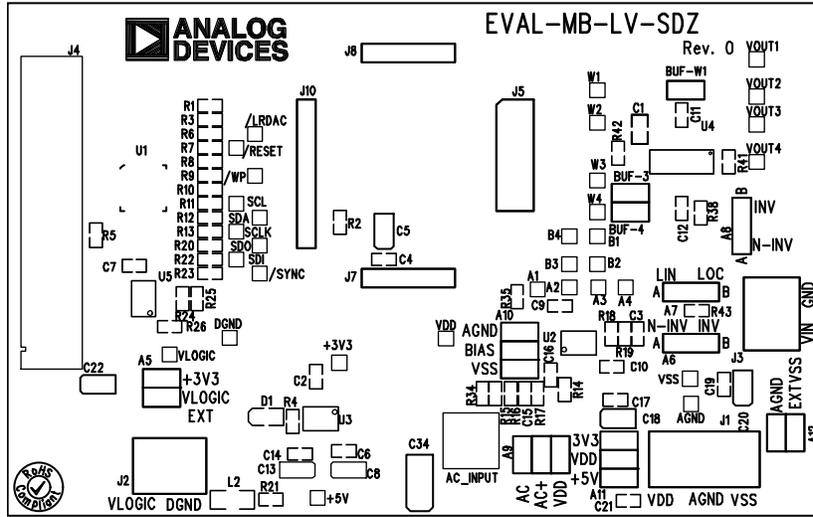


Figure 13. Component Side View

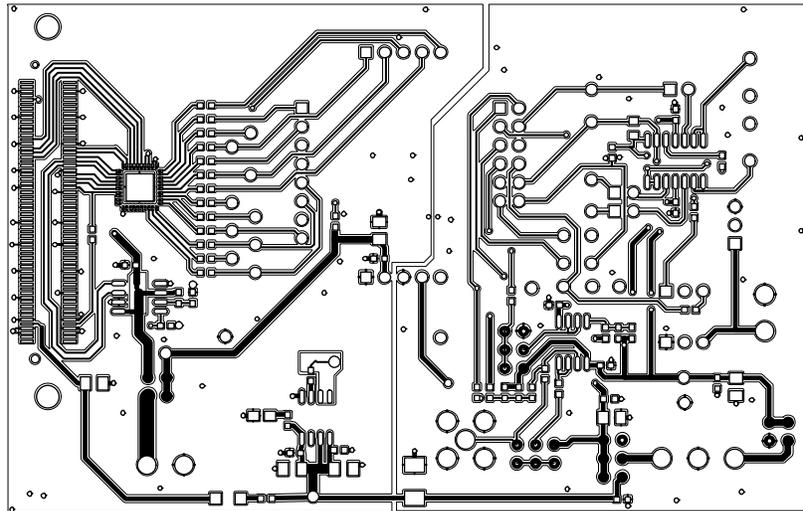


Figure 14. Component Placement Drawing

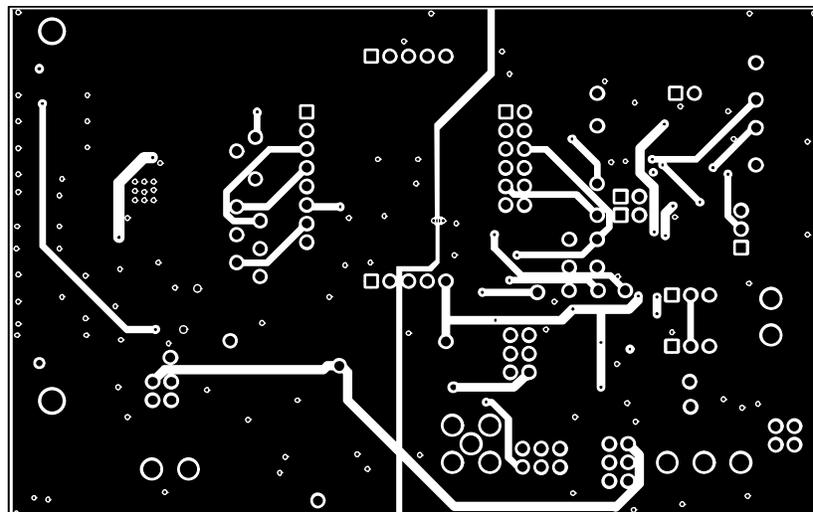


Figure 15. Layer 2 Side PCB Drawing

DAUGHTER BOARD

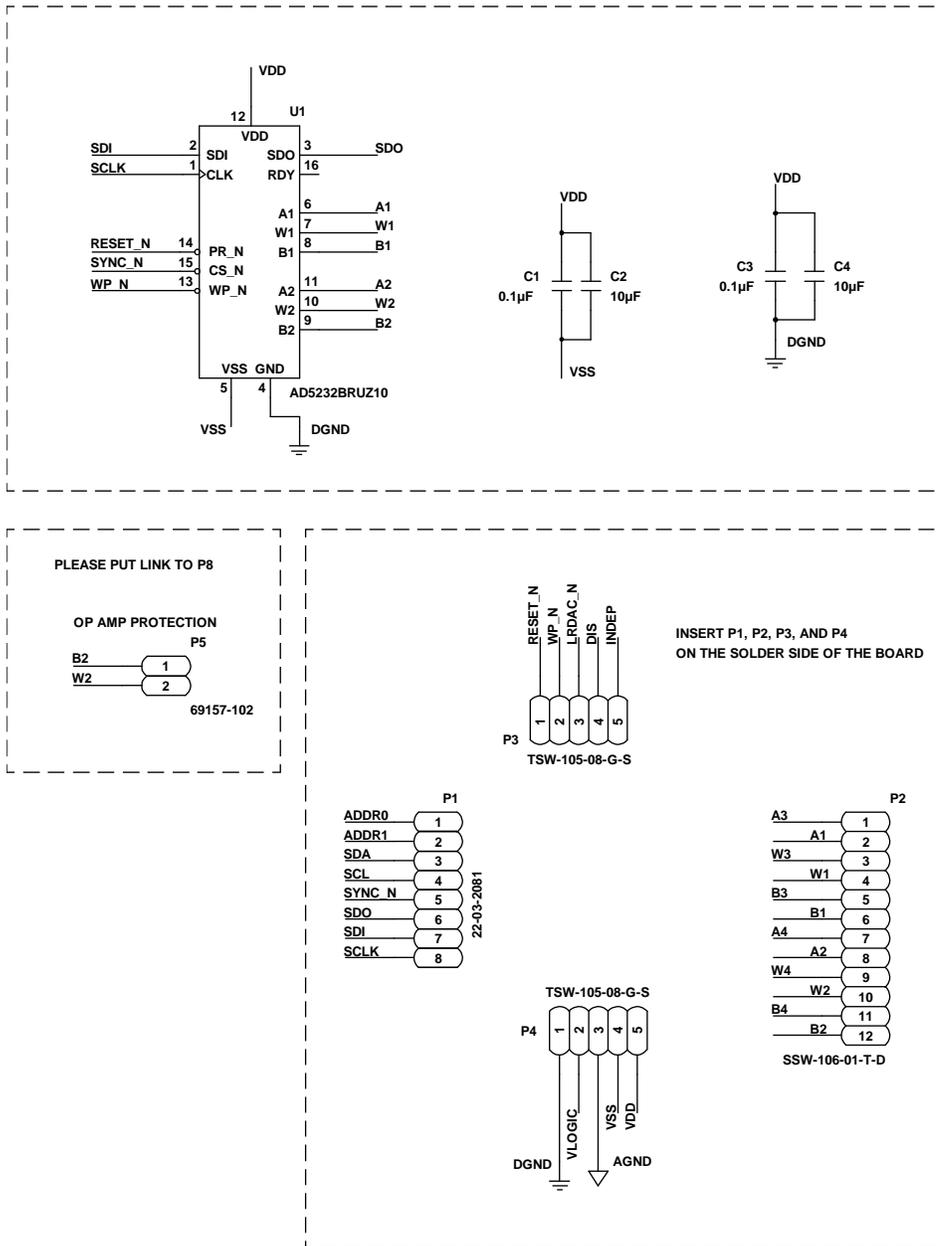


Figure 16. Schematic of Daughter Board

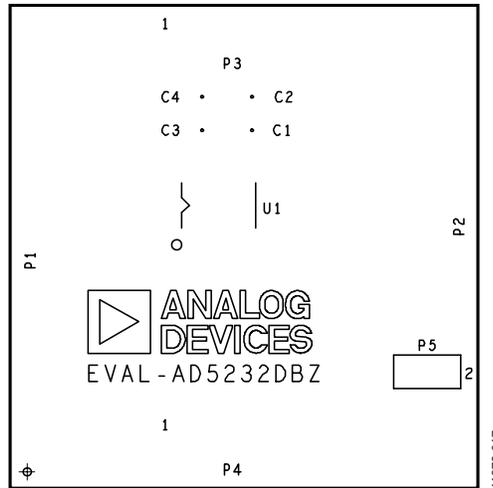


Figure 17. Component Side View

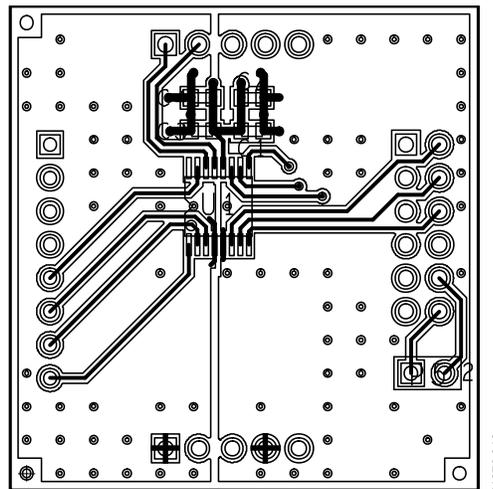


Figure 18. Component Placement Drawing

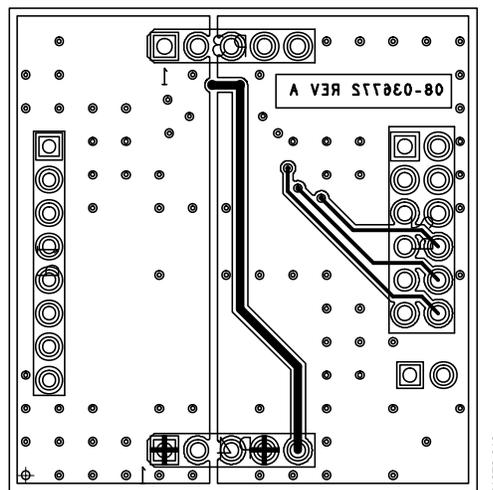


Figure 19. Layer 2 Side PCB Drawing

## BILL OF MATERIALS

Table 6. Motherboard Bill of Materials

| Qty | Reference Designator   | Description  | Supplier <sup>1</sup> /Part Number       |
|-----|--|--|--|
| 3   | BUF-3, BUF-4, BUF-W1   | 2-pin (0.1" pitch) header and shorting shunt       | FEC 1022247 and FEC 150411               |
| 3   | A6, A7, A8   | 3-pin SIL header and shorting link                 | FEC 1022248 and FEC 150410               |
| 5   | A5, A9, A10, A11, A12  | 6-pin (3 × 2), 0.1" header and shorting block      | FEC 148535 and FEC 150411 (36-pin strip) |
| 1   | J1   | 3-pin terminal block (5 mm pitch)                  | FEC 151790                               |
| 2   | J7, J8   | 4-pin SIL header                                   | FEC 1098035                              |
| 1   | J4   | Receptacle, 0.6 mm, 120-way                        | Digi-Key H1219-ND                        |
| 1   | J10  | 8-pin inline header; 100 mil centers               | FEC 1098038                              |
| 1   | J5   | 12-pin (2 × 6), 0.1" pitch header                  | FEC 1098051                              |
| 2   | J2, J3   | 2-pin terminal block (5 mm pitch)                  | FEC 151789                               |
| 17  | R1, R3, R6, R7, R8, R9, R10, R11, R12, R13, R20, R22, R23, R34, R35, R42, R43                    | SMD resistor, 0 Ω, 0.01, 0603                      | FEC 9331662                              |
| 1   | R2   | SMD resistor, 2.2 kΩ, 0.01, 0603                   | FEC 1750676                              |
| 1   | R41  | SMD resistor, 1.7 kΩ, 1%, 0603                     | FEC 1170811                              |
| 1   | R21  | Resistor, surge, 1.6 Ω, 1%, 0603                   | FEC 1627674                              |
| 1   | R38  | SMD resistor, 2.7 kΩ, 1%, 0603                     | FEC 1750678                              |
| 1   | R14  | SMD resistor, 100 Ω, 1%, 0603                      | FEC 9330364                              |
| 1   | R4   | SMD resistor, 1 kΩ, 0.01, 0603                     | FEC 9330380                              |
| 3   | R5, R25, R26   | SMD resistor, 100 kΩ, 1%, 0603                     | FEC 9330402                              |
| 5   | R15, R16, R17, R18, R19  | SMD resistor, 33 kΩ, 1%, 0603                      | FEC 9331034                              |
| 1   | C1   | SMD capacitor, 100 nF, 10%, 0805                   | FEC 1650863                              |
| 8   | C4, C9, C10, C11, C12, C17, C19, C21   | SMD capacitor, 0.1 μF, ±10%, 0603                  | FEC 1759122                              |
| 4   | C2, C6, C7, C14  | SMD capacitor, 0.1 μF, ±10%, 0603                  | FEC 3019482                              |
| 2   | C8, C13  | SMD capacitor, 10 μF, ±10%                         | FEC 197130                               |
| 4   | C18, C20, C22, C5  | Capacitor, 10 μF, ±20%                             | FEC 1190107                              |
| 2   | C3, C15  | Capacitor, 470 nF, ±10%, 0603                      | FEC 1414037                              |
| 1   | C16  | Capacitor, 4.7 nF, ±10%, 0603                      | FEC 1414642                              |
| 1   | C34  | Capacitor, 4.7 nF, ±20%                            | FEC 1432350                              |
| 1   | L2   | Inductor, SMD, 600Z                                | FEC 9526862                              |
| 1   | D1   | Green SMD LED                                      | FEC 5790852                              |
| 1   | U1   | Two-port level translating bus switch              | <a href="#">ADG3247BCPZ</a>              |
| 1   | U2   | Dual op amp  | <a href="#">AD8652ARZ</a>                |
| 1   | U3   | Precision low dropout voltage regulator            | <a href="#">ADP3303ARZ-3.3</a>           |
| 1   | U4   | Operational amplifier                              | <a href="#">AD8618ARZ</a>                |
| 1   | U5   | I <sup>2</sup> C serial EEPROM, 64k, 2.5 V, MSOP-8 | FEC 1331335                              |
| 18  | LRDAC, RESET, SYNC, WP, A1, A2, A3, A4, AGND, B1, VOUT_C1, VOUT_C2, VOUT3, VOUT4, W1, W2, W3, W4 | Terminal, PCB, black, PK100, test point            | FEC 8731128                              |
| 5   | +3.3V, +5V, EXT_VDD, VLOGIC, EXT_VSS   | Terminal, PCB, red, PK100                          | FEC 8731144                              |

<sup>1</sup> FEC refers to Farnell Electronic Component Distributors; Digi-Key refers to Digi-Key Corporation.

**Table 7. Daughter Board Bill of Materials**

| Qty | Reference Designator | Description                                  | Supplier <sup>1</sup> /Part Number |
|-----|----------------------|--|------------------------------------|
| 1   | U1                   | 256-position digital potentiometer           | <a href="#">AD5232BRUZ10</a>       |
| 1   | P5                   | 2-pin (0.1" pitch) header and shorting shunt | FEC 1022247 and FEC 150411         |
| 2   | C2, C4               | 6.3 V, X5R, ceramic capacitor, 10 μF, ±20%   | GRM188R60J106ME47D                 |
| 2   | C1, C3               | 50 V, X7R, ceramic capacitor, 0.1 μF, ±10%   | GRM188R71H104KA93D                 |
| 1   | P1                   | Header, 2.54 mm, PCB, 1 × 8-way              | FEC 1766172                        |
| 1   | P2                   | 12-pin (2 × 6), 0.1" pitch header            | FEC 1804099                        |
| 2   | P3, P4               | 5-pin SIL header                             | FEC 1929016                        |

<sup>1</sup> FEC refers to Farnell Electronic Component Distributors.

## NOTES

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

**Legal Terms and Conditions**

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS (\$100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.