EV-21568-SOM ® Manual

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ANALOG DEVICES

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Regulatory Compliance

The *EV-21568-SOM* evaluation board is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer-end product or as a portion of a consumer-end product. The board is an open system design, which does not include a shielded enclosure and, therefore, may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The *EV-21568-SOM* evaluation board contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused boards in the protective shipping package.	

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1 Preface

Thank you for purchasing the Analog Devices, Inc. System-on-Module (SoM) *EV-21568-SOM* evaluation board.

The *EV-21568-SOM* primarily hosts the ADSP-21568 audio processor, 256Mb xSPI RAM, 256Mb xSPI Flash, a 512 Mbit Quad SPI FLASH, voltage regulation, a UART to USB interface, and a high speed external connector array that contains all of the peripheral I/O signals. Through the high speed external connector array, the *EV-21568-SOM* is intended for use with a growing family of SoM carrier products that contain a variety of peripherals to support different applications. The EV-21568-SOM is compatible with the *EV-SOMCRR-EZLITE* carrier board.

The CrossCore Embedded Studio® (CCES) software development tool chain is required for a full evaluation of this hardware platform. The *EV-21568-SOM* can also be used in a limited standalone mode while not plugged into a SoM Carrier. The standalone mode is useful for evaluating the CCES Software Development Tools and benchmarking software algorithms that do not require peripheral I/O.

The ADSP-21568 processor is a member of the SHARC® family of products. The ADSP-21568 processor is based on the SHARC+ core. The ADSP-21568 SHARC processor is a member of the SIMD SHARC family of DSPs that feature Analog Devices Super Harvard Architecture. These 32-bit/40- bit/64-bit floating-point processors are optimized for high performance audio/floating-point applications with their large onchip SRAM, multiple internal buses to eliminate I/O bottlenecks, and innovative digital audio interfaces (DAI). New enhancements to the SHARC+ core add cache enhancements, branch prediction, and other instruction set improvements—all while maintaining instruction set compatibility to previous SHARC products.

The evaluation board is designed to be used in conjunction with the CrossCore Embedded Studio® 3.0.1+ development environment for advanced application code development and debug, with features that enable the ability to:

- Create, compile, assemble, and link application programs written in C++, C, and assembly
- Load, run, step, halt, and set breakpoints in application programs
- Read and write data and program memory
- Read and write core and peripheral registers

Purpose of This Manual

This manual provides instructions for installing the product hardware (board). This manual describes the operation and configuration of board components and provides guidelines for running code on the board.

Manual Contents

The manual consists of:

- ***Using the board***

  Provides basic board information.

- ***Hardware Reference***

  Provides information about the hardware aspects of the board.

- ***Bill of Materials***

  A companion file in PDF format that lists all of the components used on the board is available on the website at http://www.analog.com/EV-21568-SOM.

- ***Schematic***

  A companion file in PDF format documenting all of the circuits used on the board is available on the website at http://www.analog.com/EV-21568-SOM.

Technical Support

You can reach Analog Devices technical support in one of the following ways:

- Post your questions in the processors and DSP support community at EngineerZone®:

  http://ez.analog.com/community/dsp

- Submit your questions to technical support directly at:

  http://www.analog.com/support

- E-mail your questions about processors, DSPs, and tools development software from ***CrossCore Embedded Studio*** or ***VisualDSP++***®:

  If using CrossCore Embedded Studio or VisualDSP++ choose ***Help*** > ***Email Support***. This creates an e-mail to processor.tools.support@analog.com and automatically attaches your CrossCore Embedded Studio or VisualDSP++ version information and `license.dat` file.

- E-mail your questions about processors and processor applications to:

  processor.support@analog.com

- Contact your Analog Devices sales office or authorized distributor. Locate one at:

  http://www.analog.com/adi-sales

Supported Integrated Circuit

This evaluation system supports the Analog Devices ADSP-21568 IC.

Supported Tools

Information about code development tools for the *EV-21568-SOM* evaluation board and ADSP-2156x product family is available at:

http://www.analog.com/EV-21568-SOM

Product Information

Product information can be obtained from the Analog Devices website and the online help system.

Information about the ADSP-21568 product family is available at:

Analog Devices Website

The Analog Devices website, http://www.analog.com, provides information about a broad range of products - analog integrated circuits, amplifiers, converters, transceivers, and digital signal processors.

To access a complete technical library for each processor family, go to http://www.analog.com/processors/technical_library. The manuals selection opens a list of current manuals related to the product as well as a link to the previous revisions of the manuals. When locating your manual title, note a possible errata check mark next to the title that leads to the current correction report against the manual.

Also note, MyAnalog.com is a free feature of the Analog Devices website that allows customization of a web page to display only the latest information about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the web pages that meet your interests, including documentation errata against all manuals. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

Visit MyAnalog.com to sign up. If you are a registered user, just log on. Your user name is your e-mail address.

EngineerZone

EngineerZone is a technical support forum from Analog Devices, Inc. It allows you direct access to ADI technical support engineers. You can search FAQs and technical information to get quick answers to your embedded processing and DSP design questions.

Use EngineerZone to connect with other DSP developers who face similar design challenges. You can also use this open forum to share knowledge and collaborate with the ADI support team and your peers. Visit http://ez.analog.com to sign up.

2 Using the Board

This chapter provides information on the major components and peripherals on the board, along with instructions for installing and setting up the emulation software.

Product Overview

The board features:

- Analog Devices ADSP-21568 processor
  - SHARC+ DSP Core
  - 400 ball BGA
  - 24.576 MHz crystal
- xSPI Memory
  - 256Mbit xSPI Flash
  - 256Mbit xSPI RAM
  - ISSI IS72WVO32M8BLO256-133HLA2
  - Single/Dual/Quad/Octal MCP
- SPI Flash Quad (`SPI1`) Memory
  - 512Mbit
  - ISSI IS25LP512M - 512M-bit Serial Flash Memory with Dual and Quad SPI
  - Single/Dual/Quad SPI
- Debug Interface (JTAG)
  - JTAG 10-pin 0.05” header
- LEDs
  - 8 LEDs: one power (green), one board reset (red), three general-purpose (amber), one fault (red) and two UART LEDs (amber)

- Pushbuttons
  - One pushbutton, RESET
- SoM Interface Connector
  - DAI
  - SPORT
  - SPI
  - UART
  - TWI
  - GPIO
  - GND/3.3V/5V/12V output

Package Contents

Your *EV-21568-SOM* package contains the following items.

- *EV-21568-SOM* board
- CCES license key card

Contact the vendor where you purchased your *EV-21568-SOM* evaluation board or contact Analog Devices, Inc. if any item is missing.

Default Configuration

The ***Default Hardware Setup*** figure shows the default settings for jumpers and switches and the location of the jumpers, switches, connectors, and LEDs. Confirm that your board is in the default configuration before using the board.

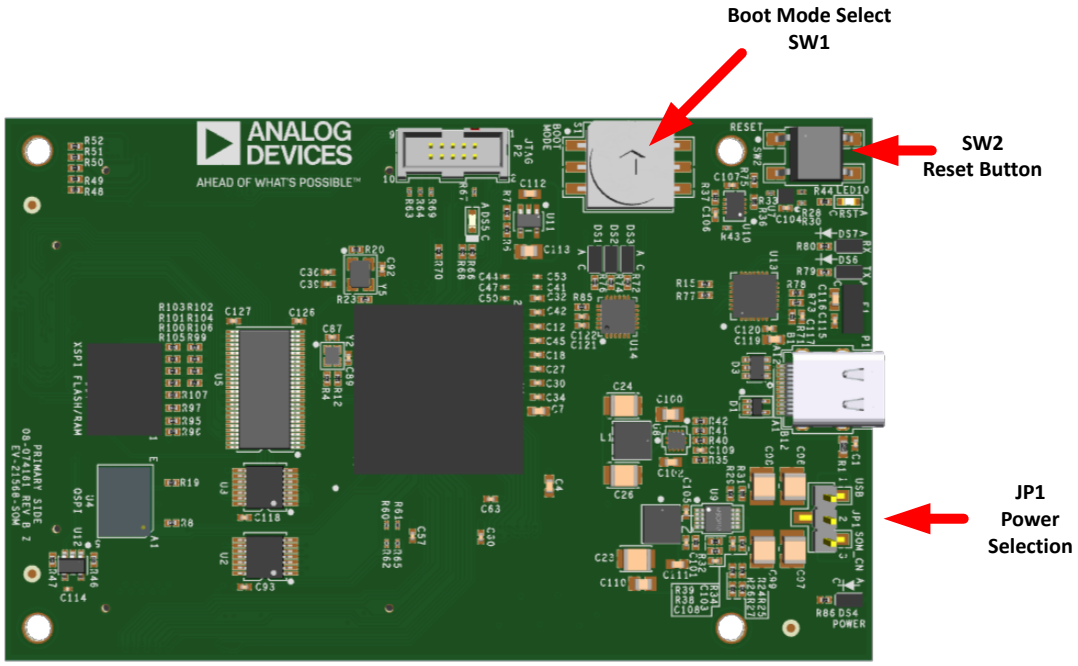

Figure 2-1: Default Hardware Setup

CrossCore Embedded Studio (CCES) Setup

Debug Interface

The *EV-21568-SOM* provides a JTAG connection via `P2`. This is for attaching an emulator, such as the ICE-1000 or ICE-2000 for debugging.

Board Power

The *EV-21568-SOM* is powered via `P1` when the board is in standalone mode. When in this mode the jumper on `JP1` should be on Pins 1-2 to select power input from `P1`. When the *EV-21568-SOM* is connected to a carrier board the power is supplied via the carrier board. When in this mode the jumper on `JP1` should be on Pins 2-3 to select power input from the carrier board.

Power-On-Self Test

The Power-On-Self-Test Program (POST) tests all the SOM board peripherals and validates functionality as well as connectivity to the processor. Once assembled, each SOM carrier board is fully tested for an extended period of time with POST for all the compatible SoM modules. All SOM carrier boards are shipped with POST preloaded into flash memory. The POST is executed by resetting the board and connecting the USB To UART to your PC with an open terminal window. The POST also can be used as a reference for a custom software design or hardware troubleshooting.

Note that the source code for the POST program is included in the Board Support Package (BSP) along with the readme file that describes how the board is configured to run POST.

Example Programs

Example programs are provided with the *EV-21568-SOM* Board Support Package (BSP) to demonstrate various capabilities of the product. The programs can be found in the `EV-21568-SOM\examples` installation folder. Refer to the readme file provided with each example for more information.

Reference Design Information

A reference design info package is available for download on the Analog Devices Web site. The package provides information on the schematic design, layout, fabrication, and assembly of the board.

The information can be found at:

http://www.analog.com/EV-21568-SOM

CP2102N-A02-GQFN28 - USB to UART

The CP2102N devices, part of the USBXpress family, are designed to quickly add USB to your applications by eliminating firmware complexity and reducing development time. These highly-integrated USB-to-UART bridge controllers provide a simple solution for updating RS-232 designs to USB using a minimum of components and PCB space.

CP2102N includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, and Universal Asynchronous Receiver/Transmitter (UART) in packages as small as 3 mm x 3 mm. No other external USB components are required for development. All customization and configuration options can be selected using a simple GUI-based configurator. By eliminating the need for complex firmware and driver development, the CP2102N devices enable quick USB connectivity with minimal development effort.

The CP2102N devices have the following features:

• Single-Chip USB-to-UART Data Transfer

• Integrated USB transceiver; no external resistors required

• Integrated clock; no external crystal required

• Internal 960-byte programmable ROM for vendor ID, product ID, serial number, power descriptor, release number, and product description strings

• On-chip power-on reset circuit

• On-chip voltage regulator — 3.3 V output

• Pin compatible with CP2101/2/9 (QFN28 package)

• Pin compatible with CP2104 (QFN24 package)

• USB Function Controller

• USB Specification 2.0 compliant; full-speed (12 Mbps)

• USB suspend states supported via SUSPEND pins

• USB Battery Charger Detection (USB BCS 1.2 Specification)

• Remote wakeup for waking a suspended host

• Single power supply of 3.0 to 3.6 V or 3.0 to 5.25 V

• Universal Asynchronous Receiver/Transmitter (UART)

• All handshaking and modem interface signals

• Data formats supported:

• Data bits — 5, 6, 7, and 8

• Stop bits — 1, 1.5, and 2

• Parity — odd, even, mark, space, no parity

• Baud rates: 300 baud to 3 Mbaud

• 512 byte receive buffer

• 512 byte transmit buffer

• Hardware or Xon/Xoff handshaking supported

• Virtual COM Port Device Drivers

• Works with existing COM port Applications

• Royalty-free distribution license

• Direct Driver Support

IS25LP512M - 512M-bit Serial Flash Memory with Dual and Quad SPI

The IS25LP512M Serial Flash memory offers a versatile storage solution with high flexibility and performance in a simplified pin count package. ISSI's "Industry Standard Serial Interface" Flash is for systems that require limited space, a low pin count, and low power consumption. The device is accessed through a 4-wire SPI Interface consisting of a Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins, which can also be configured to serve as multi-I/O (see pin descriptions).

The device supports Dual and Quad I/O, as well as standard, Dual Output, and Quad Output SPI. Clock frequencies of up to 133MHz allow for equivalent clock rates of up to 532MHz (133MHz x 4) which equates to 66.5Mbytes of data throughput. The IS25xE series of Flash adds support for DTR (Double Transfer Rate) commands that transfer addresses and read data on both edges of the clock.These transfer rates can outperform 16-bit Parallel Flash memories, allowing for efficient memory access to support XIP (eXecute In Place) operation.

The memory array is organized into programmable pages of 256/512 bytes. This family supports page program mode where 1 to 256/512 bytes of data are programmed in a single command.

QPI (Quad Peripheral Interface) supports 2-cycle instructions, further reducing instruction times. Pages can be erased in groups of 4Kbyte sectors, 32Kbyte blocks, 64K/256Kbyte blocks, and/or the entire chip. The uniform sector and block architecture allows for a high degree of flexibility so that the device can be utilized for a broad variety of applications requiring solid data retention.

IS72WVO32M8BLO256-133HLA2- 3.0V 256Mb OctalRAM + 3.0V 256Mb xSPI Flash

IS72WVO32M8BLO256 MCP Features

- 256Mb OctalRAM (PSRAM)

- 256 xSPI Flash

- Temp Grades: Auto. A2 : -40°C to +105°C Auto. A3 : -40°C to +125°C(1, 2)

- Package: 6mm x 8mm 24-ball 5x5 array TFBGA

JEDEC standard xSPI interface - Supports Standard SPI(1-1-1), Multi- I/O SPI(1-8-8/1-1-8), Octal (8-8-8) Interface - Low Signal Counts :11 Signal pins (S#, C, DQS, DQ0~DQ7)+ optional W#, ERR# - Double Transfer Rate (DTR) Operation 200MHz (400MB/s) at 1.8V VCC 133MHz (266MB/s) at 3.0V VCC

LT8609 - 2A/3A Peak Synchronous Step-Down Regulator with 2.5µA Quiescent Current

The LT8609 is a compact, high efficiency, high speed synchronous monolithic step-down switching regulator that consumes only 1.7µA of non switching quiescent current. The LT8609 can deliver 2A of continuous current with

peak loads of 3A (<1sec). Burst Mode operation enables high efficiency down to very low output currents while keeping the output ripple below 10mVP-P. A SYNC pin allows synchronization to an external clock, or spread spectrum modulation for low EMI operation. Internal compensation with peak current mode topology allows the use of small inductors and results in fast transient response and good loop stability. The EN/UV pin has an accurate 1V threshold and can be used to program VIN UVLO or to shut down the part. A capacitor on the TR/SS pin programs the output voltage ramp rate during start-up while the PG flag signals when VOUT is within ±8.5% of the programmed output voltage as well as fault conditions.

LTC3307A - 5V, 3A Synchronous Step-Down Silent Switcher in 2mm × 2mm LQFN

The LTC3307A is a very small, high efficiency, low noise, monolithic synchronous 3A step-down DC/DC converter operating from a 2.25V to 5.5V input supply. Using constant frequency, peak current mode control at switching frequencies up to 3MHz and minimum on-time as low as 22ns, this regulator achieves fast transient response with small external components. Silent Switcher architecture minimizes EMI emissions.

The LTC3307A operates in forced continuous or pulse skip mode for low noise, or low-ripple Burst Mode operation for high efficiency at light loads, ideal for battery-powered systems. The IC regulates output voltages as low as 500mV. Other features include output overvoltage protection, short-circuit protection, thermal shutdown, clock synchronization, and up to 100% duty cycle operation for low dropout. The device is available in a low profile 12-lead 2mm × 2mm × 0.74mm LQFN package with exposed pad for low thermal resistance.

ADP151 - Ultralow Noise, 200 mA, CMOS Linear Regulator

The ADP151 is an ultralow noise, low dropout (LDO) linear regulator that operates from 2.2 V to 5.5 V and provides up to 200 mA of output current. The low 135 mV dropout voltage at 200 mA load improves efficiency and allows operation over a wide input voltage range.

Using an innovative circuit topology, the ADP151 achieves ultralow noise performance without the necessity of a bypass capacitor, making the device ideal for noise-sensitive analog and RF applications. The ADP151 also achieves ultralow noise performance without compromising the power supply rejection ratio (PSRR) or transient line and load performance. The low 265 µA of operating supply current at 200 mA load makes the ADP151 suitable for battery-operated portable equipment.

The ADP151 also includes an internal pull-down resistor on the EN input.

The ADP151 is specifically designed for stable operation with tiny 1 µF, ±30% ceramic input and output capacitors to meet the requirements of high performance, space constrained applications.

The ADP151 is capable of 16 fixed output voltage options, ranging from 1.1 V to 3.3 V.

Short-circuit and thermal overload protection circuits prevent damage in adverse conditions. The ADP151 is available in tiny 5-lead TSOT, 6-lead LFCSP, and 4-ball, 0.4 mm pitch, halide-free WLCSP packages for the smallest footprint solution to meet a variety of portable power application requirements.

3 Hardware Reference

This chapter describes the hardware design of the *EV-21568-SOM*.

System Architecture

The board's configuration is shown in the ***Block Diagram*** figure.

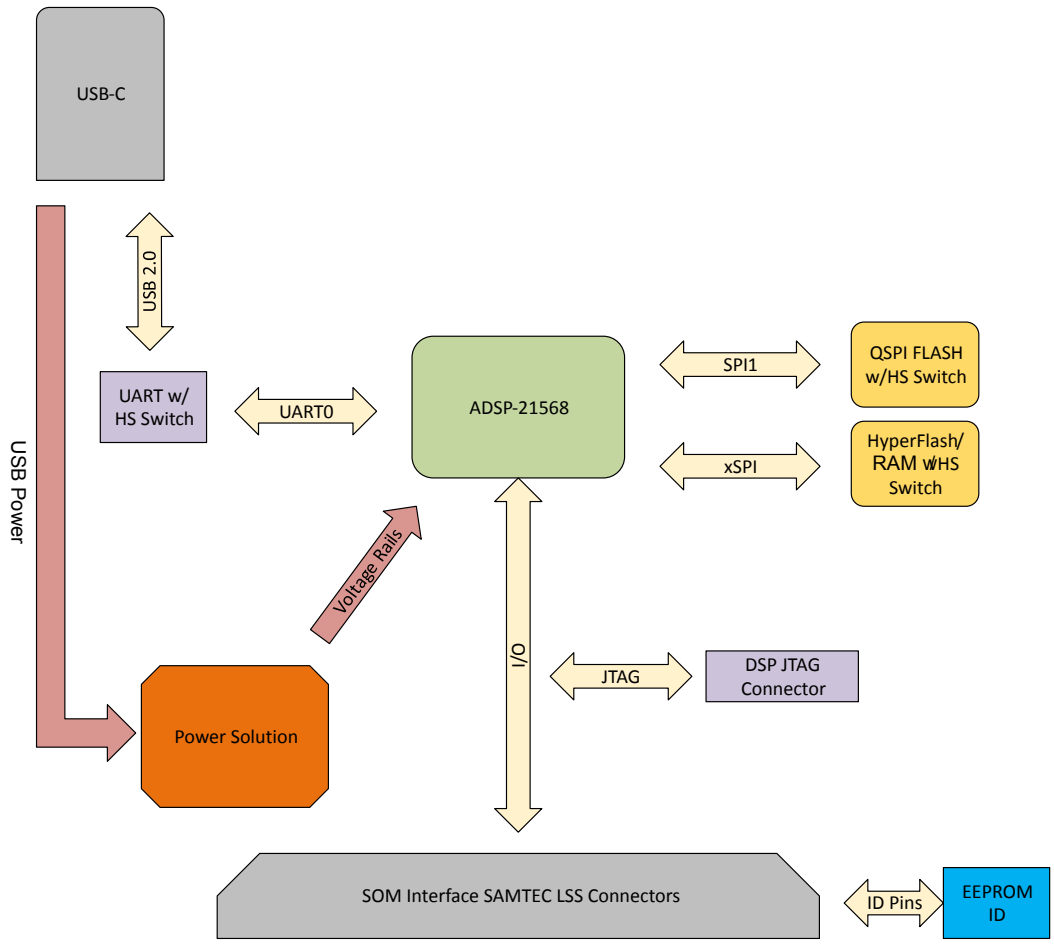

Figure 3-1: Block Diagram

This System on Module is designed to demonstrate the ADSP-21568 processor's capabilities. The board has a 24.576 MHz input clock and runs at a max core clock frequency of 933MHz.

User I/O to the processor is provided in the form of two pushbuttons and three LEDs.

The software-controlled switches (SoftConfig) facilitate the switch multi-functionality by disconnecting the push-buttons from their associated processor pins and reusing the pins elsewhere on the board.

Software-Controlled Switches (SoftConfig)

On the board, most of the traditional mechanical switches and jumpers have been replaced by I^2C software-controlled switches. The remaining mechanical switches are provided for the boot mode and pushbuttons. Reference any `SoftConfig*.c` file found in the installation directory for an example of how to set up the SoftConfig feature of

the board through software. The SoftConfig section of this manual serves as a reference to any user that intends to modify an existing software example. If software provided by ADI is used, there should be little need to reference this section.

NOTE: Care should be taken when changing SoftConfig settings not to create a conflict with interfaces. This is especially true when connecting extender cards.

Overview of SoftConfig

In order to further clarify the use of electronic single FET switches and multi-channel bus switches, an example of each is illustrated and compared to a traditional mechanical switching solution. This is a generic example that uses similar FET and bus switch components that are on the board.

After this generic discussion there is a detailed explanation of the SoftConfig interface specific to the *EV-21568-SOM*.

The ***Example of Individual FET Switches*** figure shows two individual FET switches (Pericom PI3A125CEX) with reference designators UA and UB. Net names ENABLE_A and ENABLE_B control UA and UB. The default FET switch enable settings in this example are controlled by resistors RA and RB which pull the enable pin 1 of UA and UB to ground (low). In a real example, these enable signals are controlled by the IO expander. The default pull-down resistors connects the signals EXAMPLE_SIGNAL_A and EXAMPLE_SIGNAL_B and also connects signals EXAMPLE_SIGNAL_C and EXAMPLE_SIGNAL_D. To disconnect EXAMPLE_SIGNAL_A from EXAMPLE_SIGNAL_B, the IO expander is used to change ENABLE_A to a logic 1 through software that interfaces with the Microchip. The same procedure for ENABLE_B disconnects EXAMPLE_SIGNAL_C from EXAMPLE_SIGNAL_D.

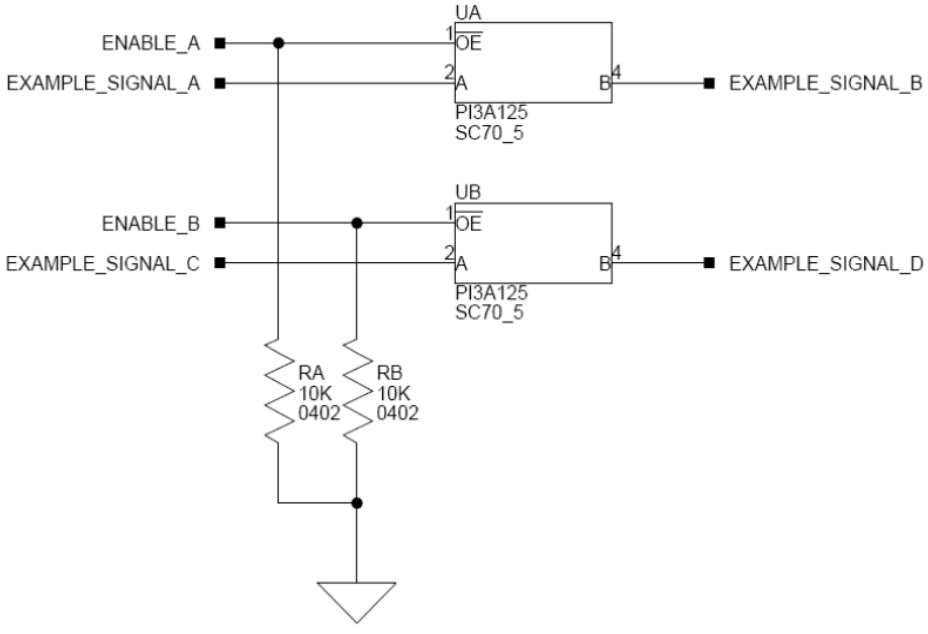

Figure 3-2: Example of Individual FET Switches

The following figure shows the equivalent circuit to the ***Example of Individual FET Switches*** figure but utilizes mechanical switches that are in the same package. Notice the default is shown by black boxes located closer to the ***ON*** label of the switches. In order to disconnect these switches, physically move the switch to the OFF position.

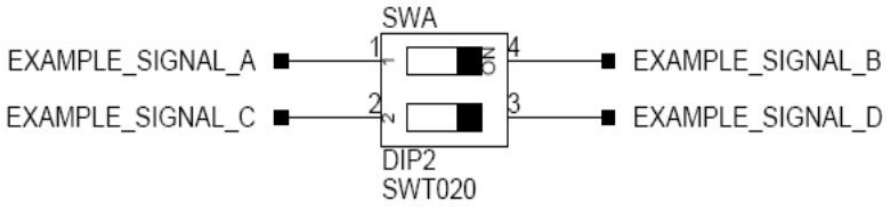

Figure 3-3: Example of a Mechanical Switch (Equivalent to Example of Individual FET Switches Figure)

The ***Example of Bus Switch*** figure shows a bus switch example, reference designator `UC` (Pericom PI3LVD512ZHE), selecting between lettered functionality and numbered functionality. The signals on the left side are multiplexed signals with naming convention letter_number. The right side of the circuit shows the signals separated into letter and number, with the number on the lower group (`0B1`) and the letter on the upper group (`0B2`). The default setting is controlled by the signal `CONTROL_LETTER_NUMBER` which is pulled low. This selects the number signals on the right to be connected to the multiplexed signals on the left by default. In this example, the IO expander is not shown but controls the signal `CONTROL_LETTER_NUMBER` and allows the user to change the selection through software.

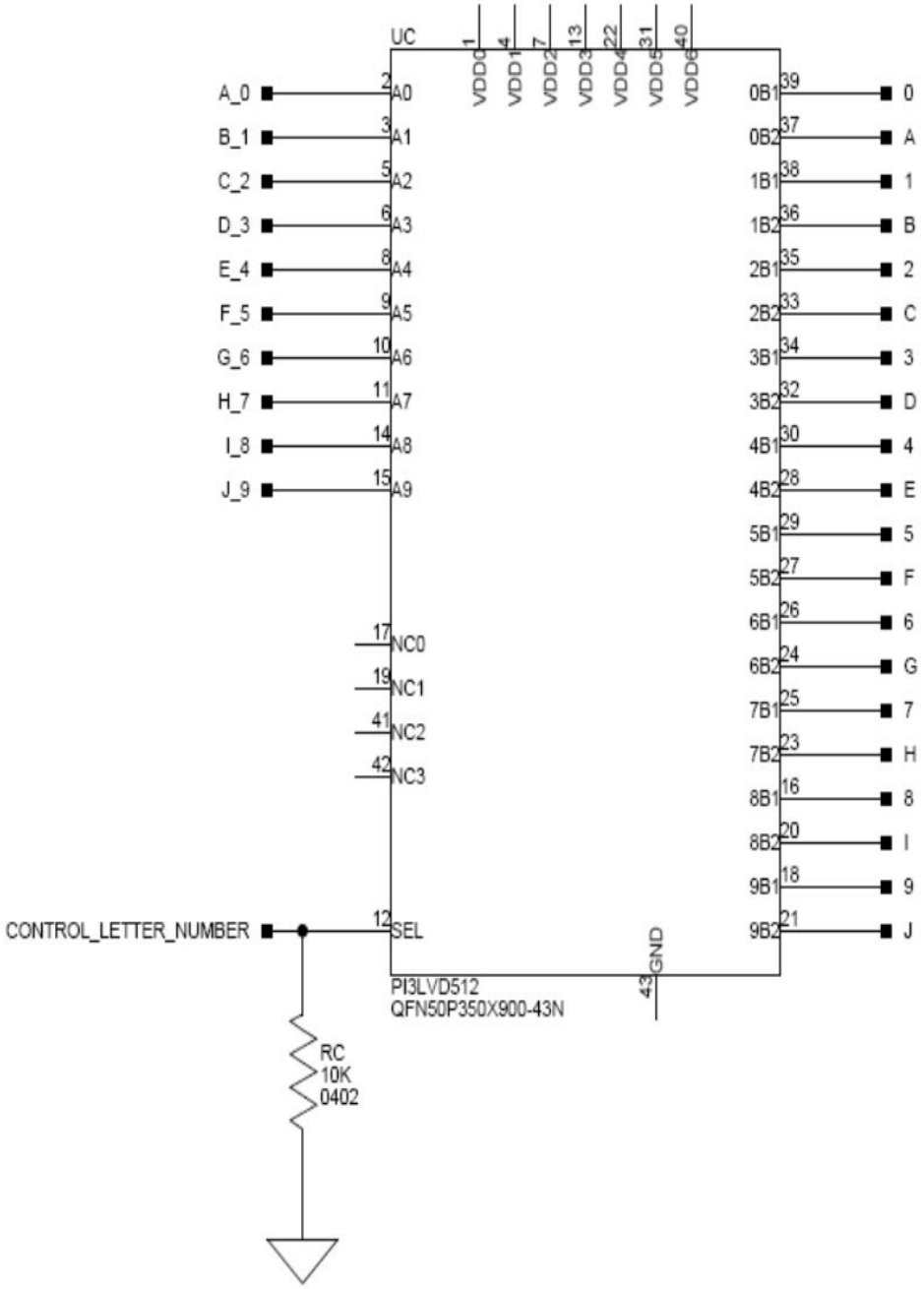

Figure 3-4: Example of a Bus Switch

The following figure shows the equivalent circuit to the ***Example of Bus Switch*** figure but utilizes mechanical switches. Notice the default for reference designators SWC and SWD is illustrated by black boxes located closer to the ***ON*** label of the switches to enable the number signals by default. Also notice the default setting for reference designators SWE and SWF is OFF. In order to connect the letters instead of the numbers, the user physically changes all switches on SWC and SWD to the OFF position and all switches on SWE and SEF to the ON position.

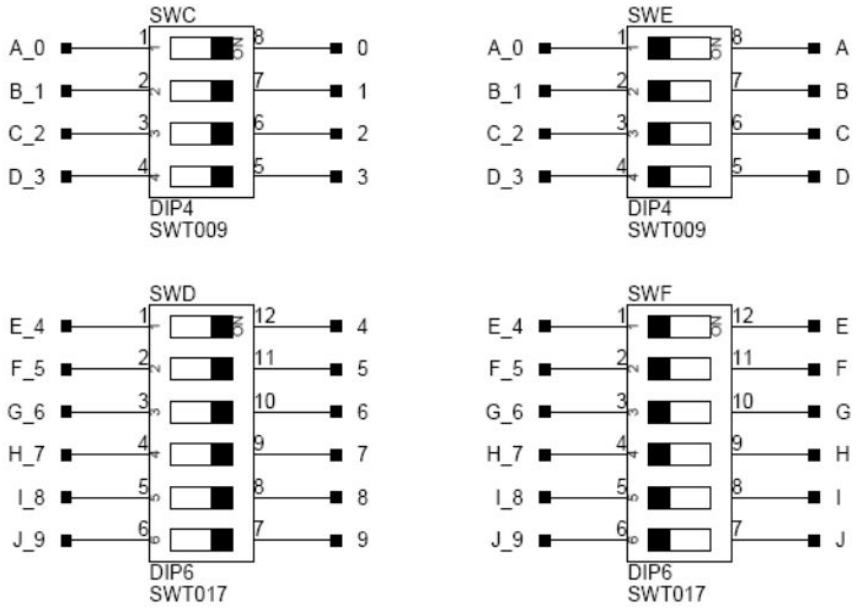

Figure 3-5: Example of a Mechanical Switch (Equivalent to Example of Bus Switch)

SoftConfig on the Board

The Analog Devices ADP5587 GPIO extenders provide control for individual electronic switches. The TWI interface of the processor communicates with the GPIO extender devices. There are individual switches with default settings that enable basic board functionality.

The ***Default Processor Interface Availability*** table lists the processor and board interfaces that are available by default. Note that only interfaces affected by software switches are listed in the table.

Table 3-1: Default Processor Interface Availability

Interface	*Availability by Default*
UART0	USB to UART IC
SPI 1 Flash	Quad mode enabled
xSPI	xSPI device enabled,xSPI to SOM Interface disabled
LEDs	Enabled

Programming SoftConfig Switches

On the board, an ADI ADP5587 device exist. The ADP5587 can be configured as a GPIO extender or a keypad interface. It is used as a GPIO Extended on the System on Module evaluation board.

Refer to the ASP5587-1 datasheet for programming information. https://www.analog.com/media/en/technical-documentation/data-sheets/adp5587.pdf

Each example in the Board Support Software (BSP) includes source files that program the soft switches, even if the default settings are being used. The `README` for each example identifies only the signals that are being changed

from their default values. The code that programs the soft switches is located in the `SoftConfig_XXX.c` file in each example where XXX is the name of the baord.

The part number of the ADP5587 determines the address of the IC. The ADP5587ACPZ has (***I^2C Hardware Address 0x68*** and the ADP5587ACPZ-1 has ***I^2C Hardware Address 0x60***).

Table below ***Output Signals of ADP5587 GPIO Expander (U14)*** show the output signals of the ADI GPIO extender (***U14***), with a TWI address of `0110 100X`, where `X` represents the read or write bit. The signals that control an individual FET have an entry in the ***FET*** column. The ***Component Connected*** column shows the board IC that is connected if the FET is enabled. The (`U14`) is controlling the enable signal of a FET switch. Also note that if a particular functionality of the processor signal is being used, it is in ***bold*** font in the ***Processor Signal*** column.

Table 3-2: Output Signals of ADP5587 GPIO Extender (U14)

Connection	*Signal Name*	*Description*	*FET*	*Processor Signal (if applicable)*	*Connected*	*Default*
C9	DS1	GPIO LED		None	DS1	High
C8	DS2	GPIO LED		None	DS2	High
C7	DS3	GPIO LED		None	DS3	High
R3	$\overline{\text{SPI1FLASH\_CS\_EN}}$	Enable SPI Flash CS	U2	PA_05/SPI2_SEL1b/ OSPI_SEL1b/SMC0_D05/ SPI2_SSb	U4	High
R2	$\overline{\text{SPI1D2\_D3\_EN}}$	Enabel SPI Flash Quad Mode	U2	PA_02/SPI2_D2/OSPI_D2/ TWI3_SCL/SMC0_D02/ TM0_ACLK3 PA_03/SPI2_D3/ OSPI_D3/TWI3_SDA/ SMC0_D03	U4	High
R1	$\overline{\text{UART0\_EN}}$	Enable UART to USB	U3	PA_06/SPI0_CLK/ UART0_TXb/OSPI_D4/ SMC0_D06/TM0_ACLK1 PA_07/SPI0_MISO/ UART0_RXb/OSPI_D5/ SMC0_D07/TM0_ACI0	U13	High
R0	$\overline{\text{UART0\_FLOW\_EN}}$	Enables UART Flow Control	U3	PA_08/SPI0_MOSI/ UART0_RTSb/OSPI_D6/ SMC0_D08/TM0_ACLK2 PA_09/SPI0_SEL1b/ UART0_CTSb/OSPI_D7/ SMC0_D09/SPI0_SSb	U13	High
C1	$\overline{\text{XSPI\_EN}}$	Enables xSPI on SOM or SOM connector	U17	xSPI	U5	High

Switches

This section describes operation of the switches. The switch locations are shown in the ***Switch/Jumper Locations*** figure.

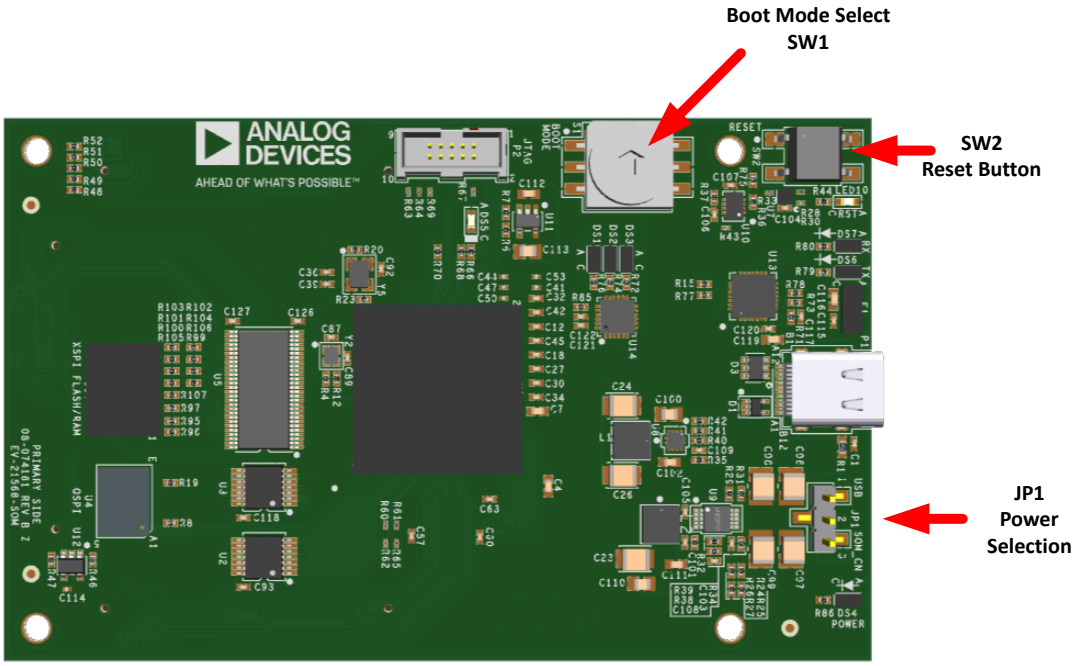

Figure 3-6: Switch/Jumper Locations

Boot Mode Select (SW1)

The Boot Mode selection switch selects between the different boot modes of the processor. The ***Boot Mode Switch*** table shows the available boot mode settings.

Table 3-3: Boot Mode Switch

Position	*Processor Boot Mode*
0	No Boot
1	SPI2 Flash Boot
2	SPI2 Host Boot
3	UART0 Host Boot

Table 3-3: Boot Mode Switch (Continued)

Position	*Processor Boot Mode*
4	Reserved
5	xSPI Flash Boot
6	SPI1 Flash Boot
7	Reserved

Reset Pushbutton (SW2)

The reset pushbutton resets the ADSP-21568 processor. The reset signal also is connected to the expansion connectors via the SYS_HWRST signal. Reset (LED10) is used to indicate when the board is in reset.

Jumpers

This section describes functionality of the configuration jumpers. The ***Switch/Jumper Locations*** figure shows the jumper locations.

Power (JP1)

The Power jumper selects the input power source to the module. Pin 1-2 selects power input from USB Type C Connector (P1) and Pin 2-3 selects Power from the SoM Interface Connection. When using the EV-SOMCRR-EZLITE or other plug in base board, use Jumper setting Pin 2-3.

LEDs

This section describes the on-board LEDs. The ***LED Locations*** figure shows the LED locations.

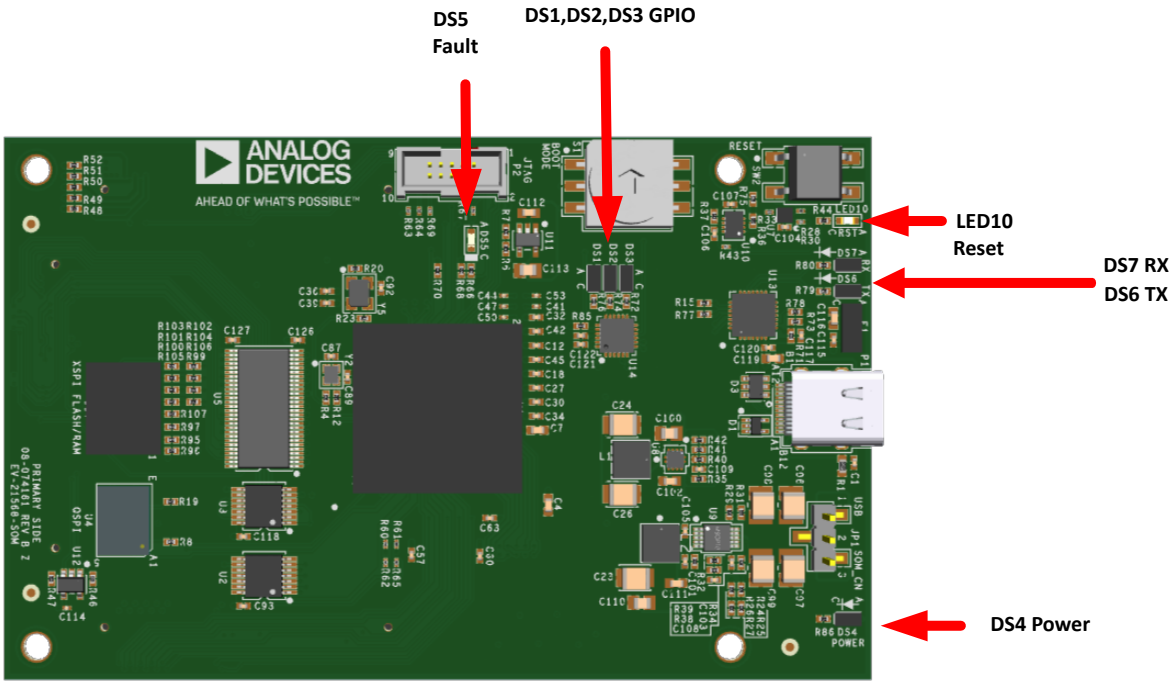

Figure 3-7: LED Locations

Fault (DS5)

When ON, it indicates a system fault. For more information, refer to the ADSP-2156x Hardware Reference Manual.

Power (DS4)

When ON (green), it indicates that power is being supplied to the board properly.

GPIO (DS1, DS2, DS3)

Three LEDs are connected to the SoftConfig(see the ***GPIO LEDs*** table). The LEDs are active high and are turned ON (amber) by writing to the U14 SoftConfig IC.

Table 3-4: GPIO LEDs

Reference Designator	*Programmable Flag Pin*
DS1	SoftSwitch
DS2	SoftSwitch
DS3	SoftSwitch

Reset (LED10)

When ON (red), it indicates that the board is in reset. A global board reset is asserted by pressing SW2, which activates the LED. For more information, see Reset Pushbutton (SW2).

Connectors

This section describes connector functionality and provides information about mating connectors. The connector locations are shown in the ***Connector Locations*** figure.

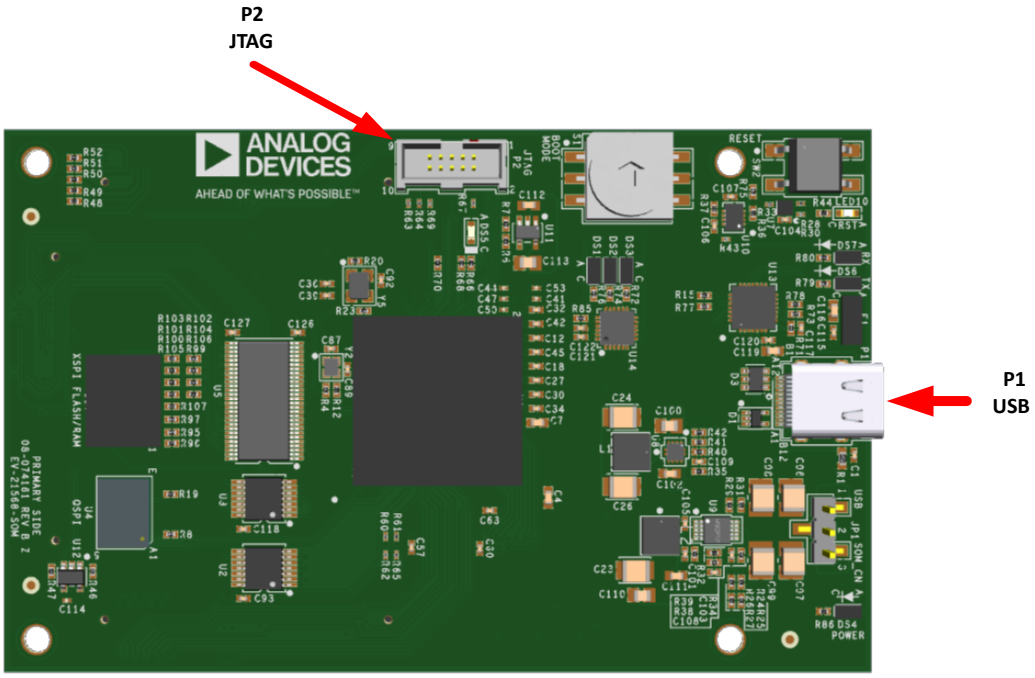

Figure 3-8: Connector Locations Top View

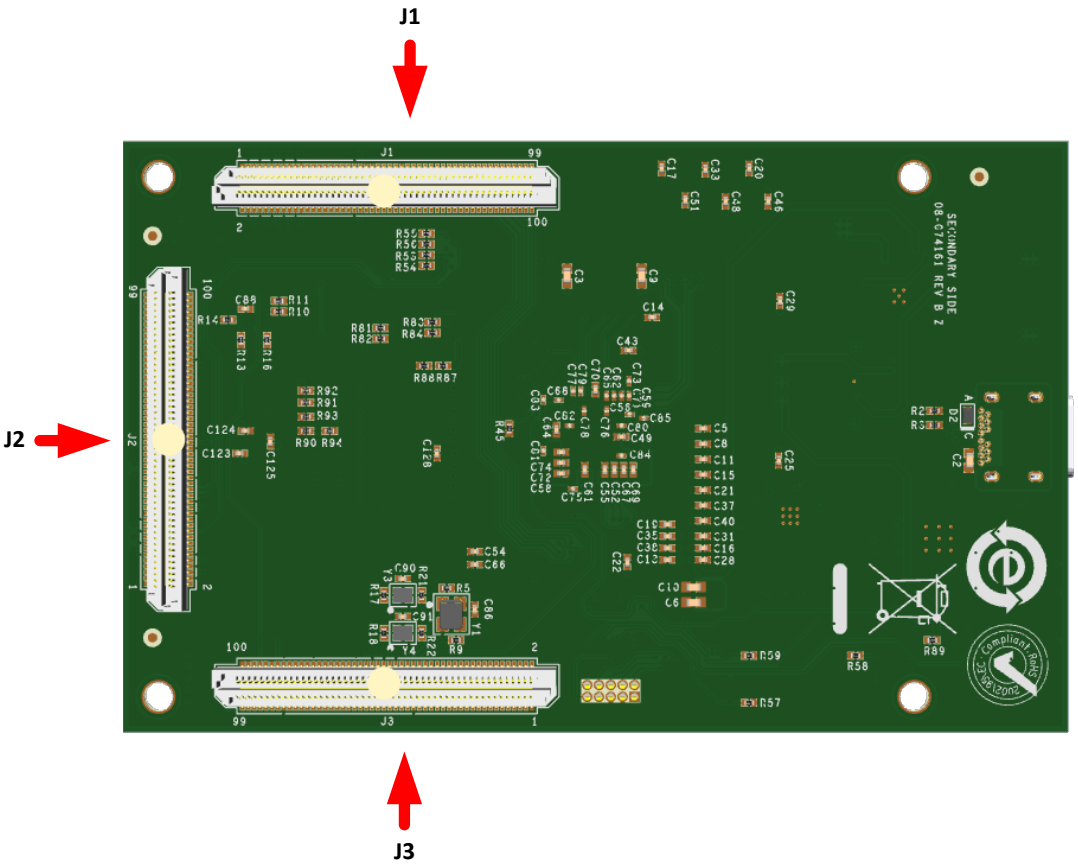

Figure 3-9: Connector Locations Bottom View

JTAG (P2)

The JTAG header provides debug connectivity for the processor. This is a 0.05" shrouded through-hole connector from SAMTEC (SHF-105-01-L-D-SM-K). This connector mates with ICE- 1000, ICE-2000, and any newer Analog Devices emulators. For more information, see Debug Interface

USB Type C Connector (P1)

USB Type C Power Delivery for powering the SoM when JP1 is set to position 1-2.

Part Description	*Manufacturer*	*Part Number*
USB Type C	MOLEX	1054500101
Mating Cable		
USB Type C	ANY	ANY

SoM Interface Connection (J1, J2 and J3)

The SoM Interface consists of three SAMTEC high speed connectors that provide the DSP peripheral signals for use with a plug in baseboard. The *SoM Connector* figure shows the connector locations.

These signals are based upon the peripheral signal needs, which allows multiple DSPs to be used with this connection. These connectors are self-mating and the pinout here reflects the connectors on the EV-21568-SOM.

Table 3-5: SoM Interface J1 Connector

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	21	DAI0_PIN10	41	DAI0_PIN20	61	NU	81	NU
2	GND	22	DAI1_PIN10	42	DAI1_PIN20	62	NU	82	NU
3	DAI0_PIN01	23	NU	43	GND	63	NU	83	NU
4	DAI1_PIN01	24	NU	44	GND	64	NU	84	NU
5	DAI0_PIN02	25	NU	45	GND	65	NU	85	NU
6	DAI1_PIN02	26	NU	46	GND	66	NU	86	NU
7	DAI0_PIN03	27	NU	47	NU	67	NU	87	GND
8	DAI1_PIN03	28	NU	48	NU	68	NU	88	CNT_UD
9	DAI0_PIN04	29	NU	49	NU	69	NU	89	NU
10	DAI1_PIN04	30	NU	50	NU	70	NU	90	CNT_ZM
11	DAI0_PIN05	31	NU	51	NU	71	NU	91	NU
12	DAI1_PIN05	32	NU	52	NU	72	NU	92	CNT_DG
13	DAI0_PIN06	33	NU	53	NU	73	NU	93	NU
14	DAI1_PIN06	34	NU	54	NU	74	NU	94	GND
15	DAI0_PIN07	35	NU	55	GND	75	NU	95	NU
16	DAI1_PIN07	36	NU	56	GND	76	NU	96	MLB_CLK
17	DAI0_PIN08	37	NU	57	NU	77	NU	97	NU
18	DAI1_PIN08	38	NU	58	NU	78	NU	98	MLB_SIG
19	DAI0_PIN09	39	DAI0_PIN19	59	NU	79	NU	99	NU
20	DAI1_PIN09	40	DAI1_PIN19	60	NU	80	NU	100	MLB_DAT

Table 3-6: SoM Interface J2 Connector

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	21	xSPI_D7	41	TWI2_SDA	61	NU	81	NU
2	GND	22	NU	42	NU	62	GND	82	NU
3	SPI2_xSPI_MISO	23	SPI2_SEL2b	43	UART0_TXb	63	NU	83	NU

Table 3-6: SoM Interface J2 Connector (Continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
4	SPI0_CLK	24	GND	44	NU	64	NU	84	NU
5	SPI2_xSPI_MOSI	25	GND	45	UART0_RXb	65	NU	85	NU
6	SPI0_MISO	26	SPI0_RDY	46	NU	66	NU	86	NU
7	SPI2_xSPI_D2	27	SPI2_xSPI_RWDS	47	UART0_RTSb	67	NU	87	NU
8	SPI0_MOSI	28	SPI1_RDY	48	GND	68	GND	88	NU
9	SPI2_xSPI_D3	29	NU	49	UART0_CTSb	69	NU	89	NU
10	SPI0_SSb	30	SPI2_RDY	50	GPIO1	70	NU	90	NU
11	SPI2_xSPI_CLK	31	TWI0_SCL	51	GND	71	GND	91	NU
12	SPI0_SEL2b	32	UART1_TXb	52	GPIO2	72	NU	92	NU
13	SPI2_xSPI_SSb	33	TWI0_SDA	53	xSPI_SEL2b	73	NU	93	NU
14	SPI1_CLK	34	UART1_RXb	54	NU	74	NU	94	NU
15	xSPI_D4	35	TWI1_SCL	55	NU	75	NU	95	NU
16	SPI1_MISO	36	UART1_RTSb	56	NU	76	NU	96	NU
17	xSPI_D5	37	TWI1_SDA	57	NU	77	NU	97	NU
18	SPI1_MOSI	38	UART1_CTSb	58	NU	78	NU	98	NU
19	xSPI_D6	39	TWI2_SCL	59	NU	79	GND	99	NU
20	SPI1_SSb	40	NU	60	NU	80	GND	100	NU

Table 3-7: SoM Interface J3 Connector

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	21	NU	41	GND	61	NU	81	NU
2	GND	22	GND	42	CLK1	62	NU	82	NU
3	NU	23	NU	43	NU	63	NU	83	NU
4	NU	24	NU	44	CLK2	64	NU	84	NU
5	NU	25	GND	45	NU	65	NU	85	GND
6	NU	26	NU	46	GND	66	NU	86	NU
7	NU	27	NU	47	NU	67	NU	87	VDD_EXT
8	NU	28	NU	48	JTG0_TMS/ SWDIO	68	NU	88	$\overline{\text{SYS\_FAULT}}$*
9	NU	29	NU	49	NU	69	NU	89	VDD_VREF
10	NU	30	NU	50	JTG0_TCK/ SWCLK	70	NU	90	GND

Table 3-7: SoM Interface J3 Connector (Continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
11	NU	31	NU	51	NU	71	NU	91	VDD_VREF
12	NU	32	NU	52	JTG0_TDO/SW0	72	NU	92	NU
13	NU	33	NU	53	NU	73	NU	93	VDD_INT
14	NU	34	NU	54	JTG0_TDI	74	NU	94	$\overline{\text{SYS\_HWRST}}$
15	NU	35	NU	55	NU	75	NU	95	VDD_EXT
16	NU	36	GND	56	$\overline{\text{JTG0\_TRST}}$	76	GND	96	NU
17	NU	37	NU	57	NU	77	NU	97	Power_VDD
18	NU	38	SYS_CLKOUT	58	$\overline{\text{TARGET\_RESET}}$	78	NU	98	Power_GND
19	NU	39	GND	59	NU	79	NU	99	Power_VDD
20	NU	40	AUDIO_CLK	60	GND	80	NU	100	Power_GND

Table 3-8: Mating Connector

Part Description	*Manufacturer*	*Part Number*
100-pin, 0.64 mm	SAMTEC	LSS-150-01-L-DV-A-K
Mating Connector		
100-pin, 0.64 mm	SAMTEC	LSS-150-01-L-DV-A-K