Evaluating the ADPA1122 43 dBm (20 W), 8.2 GHz to 11.8 GHz, GaN Power Amplifier

FEATURES

- 2-layer Rogers 4350B evaluation board with heat spreader
- End launch 2.92 mm jack RF connectors
- Through calibration path (depopulated)
- Drain or gate pulsing capability

EVALUATION KIT CONTENTS

- ADPA1122-EVALZ evaluation board
- 30 V drain pulser board

EQUIPMENT NEEDED

- Pulse generator
- Oscilloscope, Keysight DSOX3034T or equivalent
- 32 V, 2 A power supply, Keysight E3634A or equivalent
- −4 V power supply
- Keysight 1147B current probe or equivalent
- Keysight N2820A current probe or equivalent
- RF signal generator
- Directional coupler
- RF power sensor
- RF power meter
- RF attenuator
- Spectrum analyzer

DOCUMENTS NEEDED

- ADPA1122 data sheet

GENERAL DESCRIPTION

The ADPA1122-EVALZ consists of a 2-layer printed circuit board (PCB) fabricated from a 10 mil thick, Rogers 4350B copper clad mounted to an aluminum heat spreader. The heat spreader assists in providing thermal relief to the device as well as mechanical support to the PCB. Mounting holes on the heat spreader allow the spreader to be attached to a heat sink. Alternatively, the spreader can be clamped to a hot and cold plate. The RFIN and RFOUT ports on the ADPA1122-EVALZ are populated by 2.92 mm (K) female coaxial connectors. The ADPA1122-EVALZ is populated with components suitable for use over the entire operating temperature range of the device. To calibrate board trace losses, a through calibration path is provided between the J1 and J2 connectors. J1 and J2 must be populated with 2.92 mm (K) coaxial connectors to use the through calibration path.

Ground, power, and gate control are provided by two 24-pin headers (J3 and J4) on the ADPA1122-EVALZ. The pinouts for these two headers are shown in Table 1.

RF traces on the ADPA1122-EVALZ are 50 Ω, grounded, coplanar waveguide. The package ground leads and the exposed paddle connect directly to the ground plane. Multiple vias connect the top and bottom ground planes with particular focus on the area directly beneath the ground paddle to provide adequate electrical conduction and thermal conduction to the heat spreader.

The ADPA1122-EVALZ ships with a drain pulser board that assists with control and application of a pulsed drain bias. The ADPA1122-EVALZ also ships with an extender board that can interconnect the pulser board and evaluation board, providing a cutout to allow drain-current monitoring with a current probe. The extender board also allows the ADPA1122-EVALZ to be inserted into an oven without having to insert the pulser board.

For full details on the ADPA1122, see the ADPA1122 data sheet, which must be consulted in conjunction with this user guide when using the ADPA1122-EVALZ.

TABLE OF CONTENTS

REVISION HISTORY

3/2023—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPHS

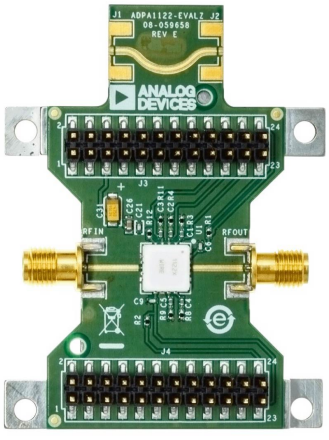

Figure 1. ADPA1122-EVALZ Evaluation Board, Primary Side

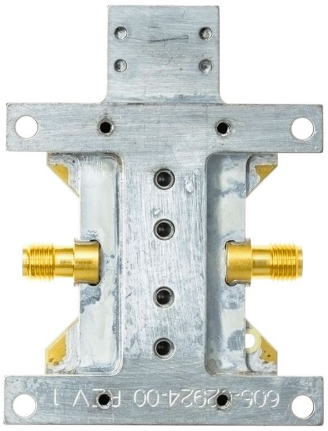

Figure 2. ADPA1122-EVALZ Evaluation Board, Secondary Side

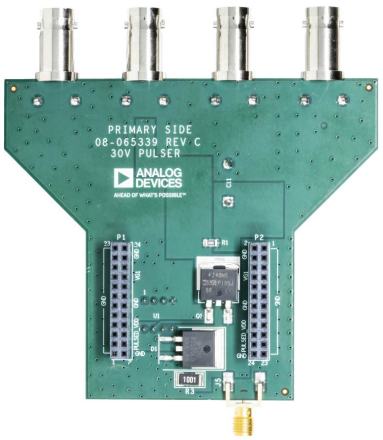

Figure 3. Pulser Board, Primary Side

Figure 4. Pulser Board, Secondary Side

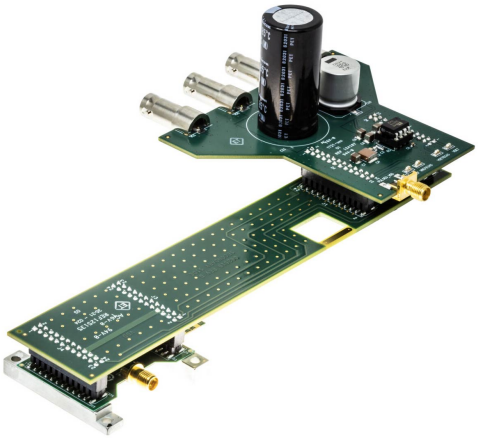

Figure 5. ADPA1122-EVALZ Evaluation Board with Extender Board and Pulser Board

HEADER PINOUT

The schematic for the ADPA1122-EVALZ is shown in Figure 10. The ADPA1122-EVALZ contains two headers, J3 and J4, and Table 1 describes the pinout of these headers.

Table 1. J3 and J4 Header Connections on the ADPA1122-EVALZ

Header	Header Pin Number	Header Pin Name
J3	1, 2, 3, 4, 6, 8, 10, 11, 12, 13, 14, 15, 16, 18, 20, 22	GND
	5	VGG
	7, 9	Not connected
	17	VDD1
	19	VDD2A
	21	VDD3A
	23	VDET_BIAS
	24	VDET
J4	1, 2, 3, 4, 5, 7, 9, 11, 12, 13, 14, 15, 16, 17, 19, 21	GND
	6, 8, 10, 18, 20, 22	Not connected
	23	VREF
	24	VREF_BIAS

INSERTION LOSS OF THE THROUGH CALIBRATION PATH

To calibrate board trace losses, a through calibration path is provided between the J1 and J2 connectors. J1 and J2 must be populated with 2.92 mm, (K) RF connectors to use the through calibration path. Figure 6 shows the insertion loss, input return loss, and output return loss of the through calibration path. Table 2 lists the insertion loss of the through path vs. frequency.

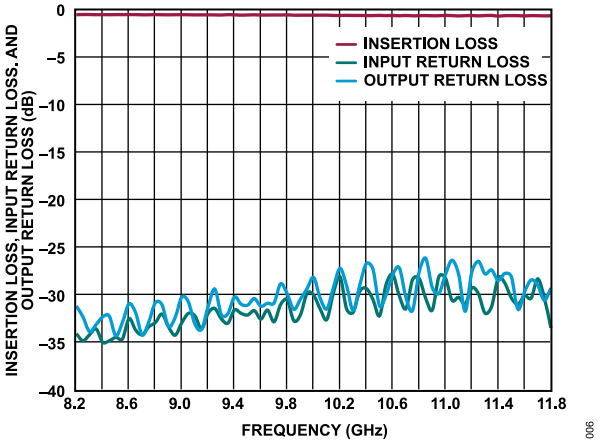

Figure 6. Insertion Loss, Input Return Loss, and Output Return Loss vs. Frequency of the Through Calibration Path

Table 2. Insertion Loss of Through Calibration Path

Frequency (GHz)	Insertion Loss (dB)
8.2	−0.50
8.4	−0.49
8.6	−0.48
8.8	−0.48
9	−0.49
9.2	−0.52
9.4	−0.52
9.6	−0.54
9.8	−0.52
10	−0.56
10.2	−0.60
10.4	−0.62
10.6	−0.60
10.8	−0.63
11	−0.60
11.2	−0.61
11.4	−0.69
11.6	−0.66
11.8	−0.64

OPERATING THE ADPA1122-EVALZ WITH THE DRAIN BIAS PULSER BOARD

The ADPA1122-EVALZ ships with a drain bias pulser board. A schematic of the pulser board is shown in Figure 7. The pulser board has two primary components. The IRFZ48NSTRLPBF is a 55 V, 64 A, metal-oxide semiconductor field effect transistor (MOSFET) that switches the drain voltage to the ADPA1122 on and off, and the MIC5021YN is a high-side, negative channel metal-oxide semiconductor (NMOS), static switch driver that controls the MOSFET.

The pulser board plugs into the J3 and J4 headers of ADPA1122-EVALZ and can be configured to provide a pulsed drain voltage and a negative gate control voltage to control the biasing of the ADPA1122.

Table 3. J1 to J5, TP1 to TP4, P1, and P2 Pulser Board Connections to the ADPA1122

Header	Header Pin Number	Header Pin Name
J1	Not applicable (BNC connector)	VDD
J2	Not applicable (BNC connector)	SENSE
J3	Not applicable (BNC connector)	VG1
J4	Not applicable (BNC connector)	PULSE
J5	Not applicable (Subminiature A (SMA) connector)	PULSED_VDD

Table 3. J1 to J5, TP1 to TP4, P1, and P2 Pulser Board Connections to the ADPA1122 (Continued)

Header	Header Pin Number	Header Pin Name
TP1	Not applicable (surface-mount test point)	VREF_BIAS
TP2	Not applicable (surface-mount test point)	VREF
TP3	Not applicable (surface-mount test point)	VDET
TP4	Not applicable (surface-mount test point)	VDET_BIAS
P1	1	VDET
	2	VDET_BIAS
	3, 5, 7, 9, 10, 11, 12, 13, 14, 15, 17, 19, 21, 22, 23, 24	GND
	4, 6, 8	PULSED_VDD
	16, 18, 20	VG1
P2	1, 2, 3, 4, 5, 7, 9 ,11, 12, 13, 14, 15, 16, 17, 19, 21	GND
	6, 8, 10	VG1
	18, 20, 22	PULSED_VDD
	23	VREF
	24	VREF_BIAS

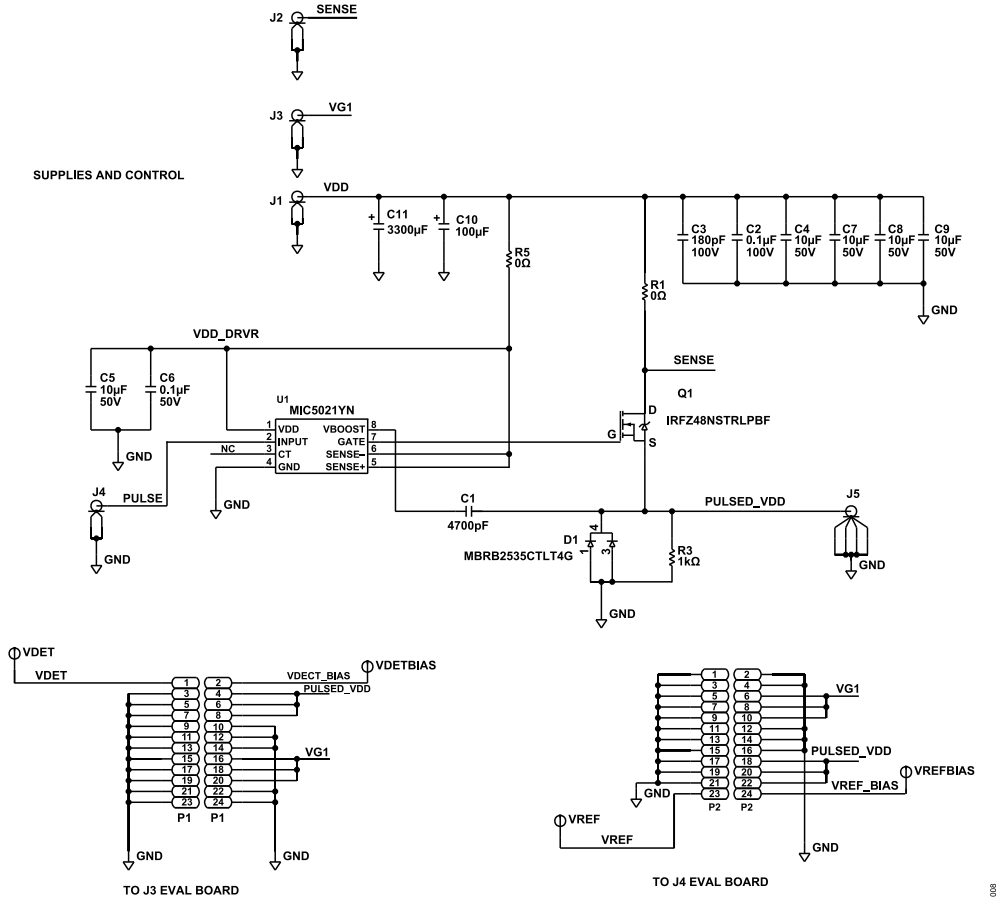

Figure 7. Analog Devices, Inc., Pulser Board Schematic

OPERATING THE ADPA1122-EVALZ WITH THE DRAIN BIAS PULSER BOARD

SETUP

The connections required to use the ADPA1122-EVALZ with the drain bias pulser board are shown in Figure 8. Before applying any bias or signals, plug the pulser board into the extender board and plug the extender board into the ADPA1122-EVALZ as shown in Figure 5. The P1 and P2 headers of the pulser board plug into the J2 and J1 headers of the extender board, and the J3 and J4 headers of the extender board plug into the J3 and J4 headers of the ADPA1122-EVALZ. The extender board is not strictly necessary but does serve the two following benefits:

- Contains a notched out section (the gold strip as shown in Figure 5) where a current clamp can be attached.
- Allows the ADPA1122-EVALZ to be inserted into a temperature chamber while the pulser board remains outside.

All external supply voltages and control signals are applied to the pulser board through the J1 through J4 connectors, which are listed in Table 3.

The gate control voltage applied to the J3 connector passes directly through the pulser board and drives the VGG pin of the ADPA1122. Because the VDD and GND lines carry currents up to 2 A, the use of heavy gauge, twisted pair wires is recommended to minimize voltage drops. To observe the pulsed drain voltage (PULSED_VDD) that drives the VDDx pins of the ADPA1122, connect an oscilloscope to the J5 coaxial connector on the pulser board.

Connect a pulse generator that can generate 0 V to 5 V pulses with a pulse width of 100 µs and a duty cycle of 10% to the J4 connector.

To observe and measure the drain current and the RF output power of the ADPA1122, use a current probe and a pulsed RF power meter. If these methods are not available, make approximations as described in the Making Average to Pulsed Approximations section.

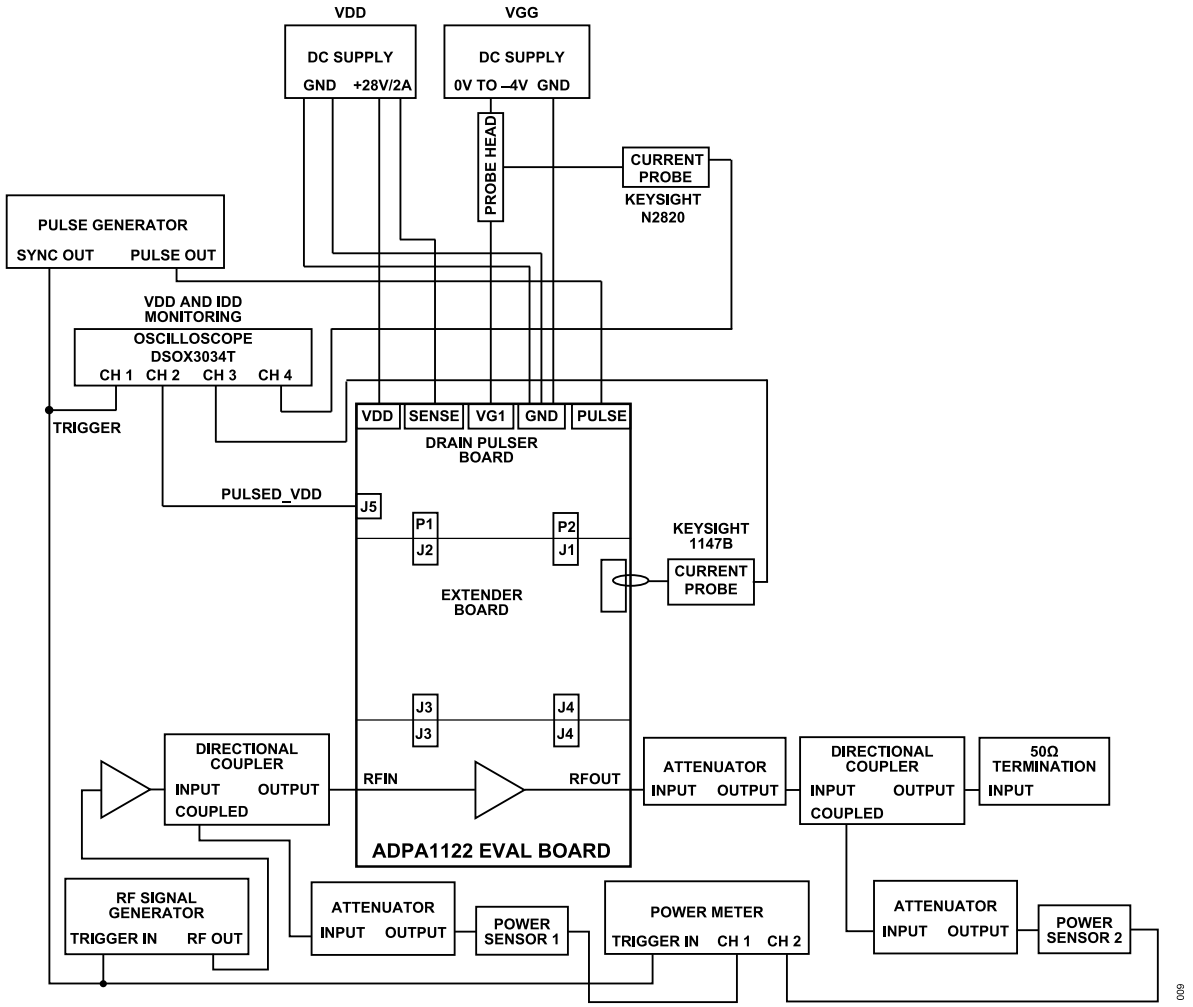

Figure 8. Setup Block Diagram

OPERATING THE ADPA1122-EVALZ WITH THE DRAIN BIAS PULSER BOARD

OPERATION

Take the following steps to power up (unless otherwise stated, all signals are applied to the pulser board):

1. Set the voltage on the J4 connector, PULSE, to 0 V.
2. Set the voltage on the J3 connector, VG1, to −4 V.
3. Set the voltage on the J1 connector, VDD, to 28 V.
4. Turn on the J4 connector, PULSE (0 V/5 V, 100 µs, 10% duty cycle).
5. Increase the voltage on the J3 connector, VG1, until the target pulsed I_{DQ} is reached (nominally 200 mA).
6. Apply the RF input signal to the RFIN connector of the AD-PA1122-EVALZ. Trigger the RF source so that the RF is applied only during the time the drain pulse is high.

Take the following steps to power down:

1. Turn off the RF input signal.
2. Set the voltage on the J3 connector, VG1, to −4 V.
3. Turn off the J4 connector, PULSE (set to 0 V).
4. Set the voltage on the J1 connector, VDD, to 0 V.
5. Set the voltage on the J3 connector, VG1, to 0 V.

OPERATING THE ADPA1122-EVALZ WITH A PULSED GATE VOLTAGE

To implement gate pulsed operation, apply a negative voltage pulse to the VGG input of the ADPA1122 while the voltage on the VDD1, VDD2A, and VDD3A pins of the ADPA1122 is held constant. The power supply that provides the drain voltage must have a fast transient response to minimize the voltage droop. The Keysight E3634A power supply or equivalent is recommended.

SETUP

All power supply, ground, and control signals are applied to the J3 and J4 headers of the ADPA1122-EVALZ. For this mode of operation, pulse the gate voltage between −4 V (off) and approximately −2.6 V (on) to set the quiescent current (I_{DQ}) to approximately 200 mA. The pulse width and duty cycle must be approximately 100 µs and 10%, respectively.

To observe and measure the drain current and the RF output power of the ADPA1122, use a current probe and a pulsed RF power meter. If these methods are not available, make approximations as detailed in the Making Average to Pulsed Approximations section.

OPERATION

Take the following steps to power up:

1. Set VDD1, VDD2A, VDD3A (Pin 17, Pin 19, and Pin 21 of J3) to 0 V.
2. Set VGG (Pin 5 of J3) to off (−4 V).
3. Set VDD to 28 V.
4. Turn on the gate voltage pulse (V_{GG} pulsing between −4 V and approximately −2.6 V).
5. Fine tune the pulse high voltage to achieve the desired pulsed I_{DQ} (nominally 200 mA) while maintaining the pulse off voltage level at −4 V.
6. Apply the RF input signal to the RFIN connector of the ADPA1122-EVALZ. Trigger the RF source so that the RF is applied only during the time the gate pulse is high.

Take the following steps to power down:

1. Turn off the RF signal.
2. Turn off the pulse to V_{GG} (V_{GG} = −4 V).
3. Set VDD to 0 V.
4. Increase the pulse to V_{GG} to 0 V.

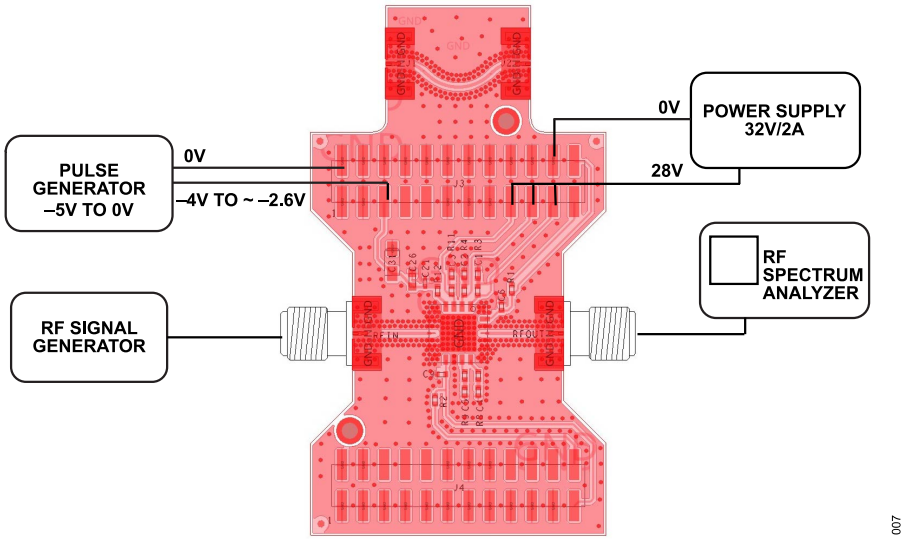

Figure 9. Gate Pulsing Setup

MAKING AVERAGE TO PULSED APPROXIMATIONS

Instruments that can be triggered are required to measure the RF power, drain current, and power added efficiency (PAE) accurately under pulsed operation. When such instrumentation is not available, use averaging and approximations. The most common approximations involve measuring the average values and then adjusting those values to account for the duty cycle. These approximations can result in errors because of limited measurement bandwidths of instruments and/or the inclusion of on and off transients and/or partial periods in the measurement.

To ensure that partial periods do not contribute significant errors to the measurements, perform averaging over a large number of pulse periods. The results of such approximations can vary with the instruments and settings used. Therefore, experimentation can be necessary to achieve credible and repeatable results. When it is not possible to make pulse triggered measurements, the only pulse connection required is the connection from the pulse generator to the J4 connector of the pulser (see Figure 8).

EVALUATION BOARD SCHEMATIC AND ARTWORK

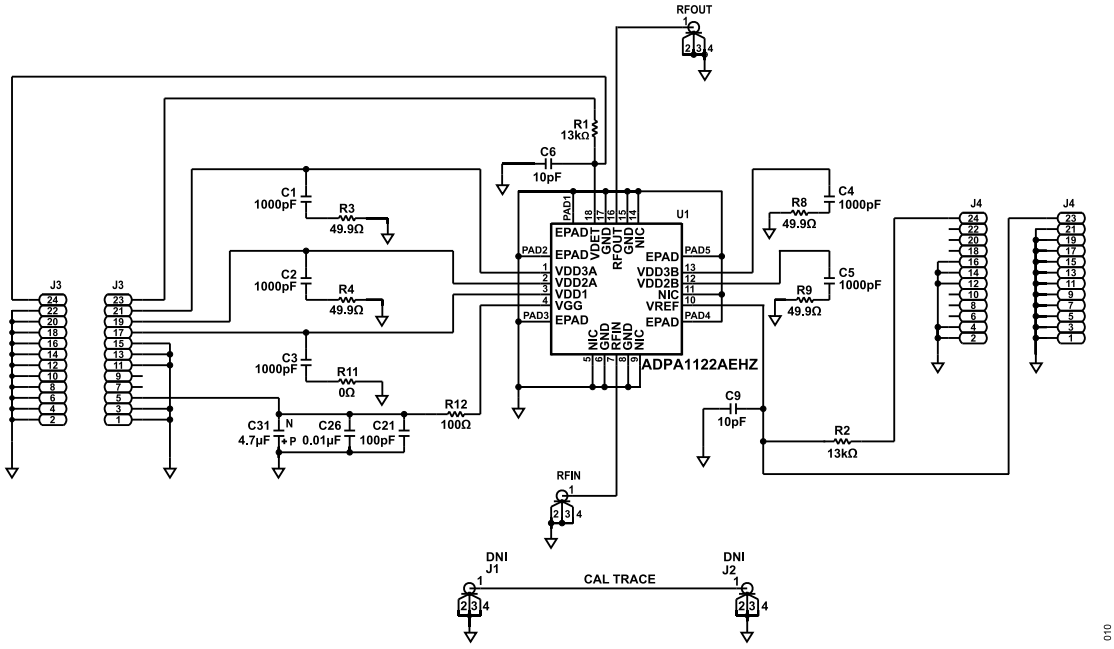

Figure 10. ADPA1122-EVALZ Schematic

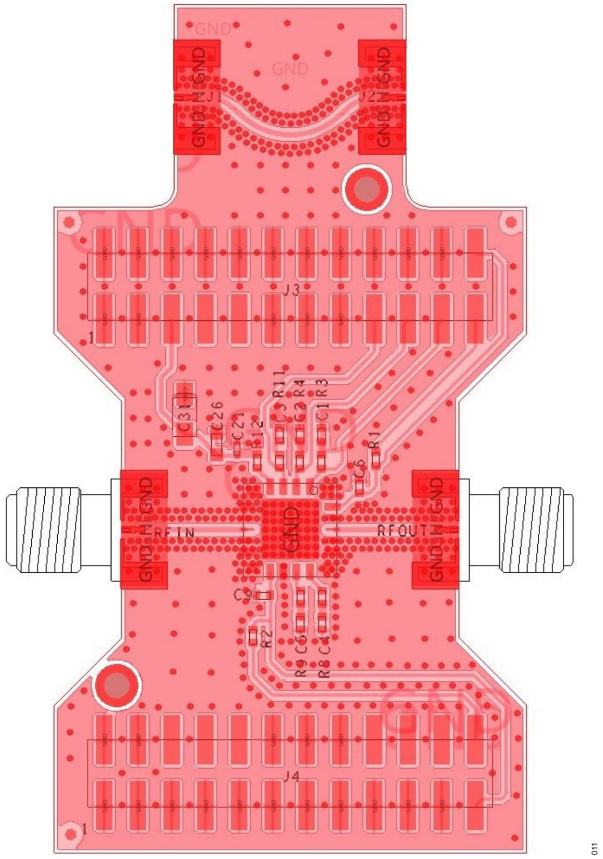

Figure 11. ADPA1122-EVALZ Assembly Drawing (J1 and J2 Not Installed)

ORDERING INFORMATION

BILL OF MATERIALS

Table 4. Bill of Materials

Reference Designator	Description	Manufacturer	Part Number
C1, C2, C3, C4, C5	1000 pF ceramic capacitors, 50 V, 5%, C0G, 0402	Murata Manufacturing, Co., Ltd.	GRM1555C1H102JA01
C6, C9	10 pF ceramic capacitors, 50 V, 5%, C0G, 0402	Yageo	CC0402JRNPO9BN100
C21	100 pF ceramic capacitor, 50 V, 5%, C0G, 0402, extreme low equivalent series resistance (ESR)	KEMET Corporation	C0402C101J5GACTU
C26	0.01 µF ceramic capacitor, 50 V, 10%, X7R, 0603	YAGEO	CC0603KRX7R9BB103
C31	4.7 µF tantalum capacitor, 20 V, 10%, 3216-18	AVX Corporation	TAJA475K020RNJ
J1, J2	2.92 mm (K) RF connectors, jack, EDGE_LAUNCH (not installed)	Winchester Interconnect	25-146-1000-92
J3, J4	Printed circuit board (PCB) connector, surface-mount, 24-position, male header, unshrouded double row ST, 2.54 mm pitch	Samtec, Inc.	TSM-112-01-L-DV
RFIN, RFOUT	K connectors, jack, EDGE_LAUNCH	Winchester Interconnect	25-146-1000-92
R1, R2	13 kΩ, surface-mounted device (SMD) resistors, 1%, 1/16 W, 0402	Yageo	9C04021A1302FLHF3
R3, R4, R8, R9	49.9 Ω SMD resistors, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF49R9X
R11	0 Ω SMD resistor, jumper, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2GE0R00X
R12	100 Ω SMD resistor, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF1000X
U1	43 dBm (20 W), 8 GHz to 11.5 GHz, gallium nitride (GaN) power amplifier	Analog Devices	ADPA1122AEHZ
Not Applicable	Aluminum heat sink 2.51 in × 1.91 in	Not applicable	Not applicable

ORDERING INFORMATION

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.