

Evaluating the ADPA9007 DC to 28 GHz, GaAs, pHEMT, 2 W Power Amplifier

FEATURES

- ▶ 2-layer Rogers 4350B evaluation board with heat spreader
- ▶ End launch 2.92 mm RF connectors
- ▶ Through calibration path

EVALUATION KIT CONTENTS

- ▶ 2-layer Rogers 4350B, EVAL-ADPA9007 evaluation board with heat spreader

EQUIPMENT NEEDED

- ▶ RF signal generator
- ▶ RF spectrum analyzer
- ▶ RF network analyzer
- ▶ 15 V, 1.0 A power supply
- ▶ 0 V to -2.0 V, 10 mA power supply
- ▶ 5 V, 100 mA power supply
- ▶ DC block, Marki Microwave, DCZM29F29 or equivalent
- ▶ Bias tee, Marki Microwave, BT20050 or equivalent
- ▶ 5 W attenuator ≥ 10 dB

GENERAL DESCRIPTION

The EVAL-ADPA9007 consists of a 2-layer printed circuit board (PCB) fabricated from 10 mil thick Rogers 4350B copper clad mounted to an aluminum heat spreader. The heat spreader assists in providing thermal relief to the [ADPA9007](#) and mechanical support to the PCB. The mounting holes on the heat spreader allow for attachment to larger heat sinks to improve thermal management. The RFIN and RFOUT/VDD ports are populated by 2.92 mm female coaxial connectors, and the respective RF traces are of 50 Ω characteristic impedance. The EVAL-ADPA9007 is populated with components suitable for use over the entire operating temperature range of the ADPA9007.

The RF transmission lines are 50 Ω grounded coplanar waveguides. The package ground leads and the exposed pad connect directly to the ground plane. Multiple vias are used to connect the top and bottom ground planes, with particular focus on the area directly beneath the ground paddle, to provide adequate electrical conduction and thermal conduction to the heat spreader.

The power supply decoupling capacitors shown in the [Figure 5](#) represent the configuration used in characterizing the device.

Full details about the part are available in the ADPA9007 data sheet, which must be consulted when using the EVAL-ADPA9007.

ADPA9007-EVALZ EVALUATION BOARD PHOTOGRAPHS

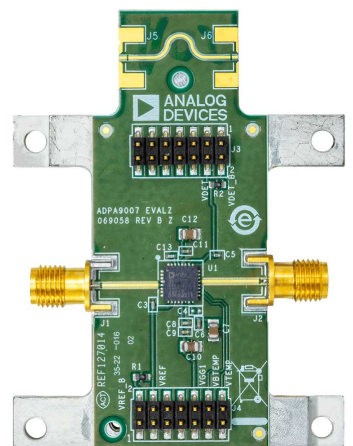


Figure 1. Primary Side

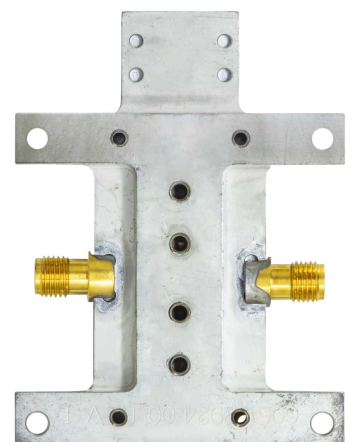


Figure 2. Secondary Side

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REVISION HISTORY

11/2023—Revision 0: Initial Version

OPERATING THE ADPA9007-EVALZ

The DC connections required to operate the EVAL-ADPA9007 are accessed through the J3 and J4 header pins (see [Table 1](#) for pin descriptions). [Figure 3](#) shows the connections necessary to operate the EVAL-ADPA9007.

The on-chip temperature monitor provides a voltage that is proportional to the temperature. To use this feature, apply +5 V to the VBTEMP pin and monitor the corresponding voltage on the VTEMP pin. User calibration is required.

An on-chip power monitor is provided to allow for convenient monitoring of the power present at the output of the ADPA9007. To use this feature, apply +5 V to VDET_B and VREF_B and monitor the voltage on the VREF pin and the VDET pin. The temperature compensated voltage proportional to the [ADPA9007](#) output power is (VREF – VDET). User calibration is required when using this feature.

Table 1. J3 and J4 Header Connections to the ADPA9007

| Header Pin No. | Mnemonic |
|-----------------------|-------------------|
| J3 | |
| 1, 3, 5, 7, 9, 11, 13 | GND |
| 2 | VDET_B |
| 4 | VDET |
| 6, 8, 10, 12, 14 | Open (do not use) |
| J4 | |
| 1, 3, 5, 7, 9, 11, 13 | GND |
| 2 | VREF_B |
| 4 | VREF |
| 6, 8 | Open (do not use) |
| 10 | VGG1 |
| 12 | VBTEMP |
| 14 | VTEMP |

POWER-UP SEQUENCE

Take the following steps to power up:

1. Set the VGG1 pin (Pin 10 of J4) to –2 V.
2. Set the RFOUT/VDD pin to +15 V through an external bias tee.
3. Adjust the VGG1 pin between –2 V and 0 V to achieve a quiescent drain current of 500 mA.
4. To operate the on-chip temperature monitor and on-chip power detectors, apply +5 V to the VREF_B, VBTEMP, and VDET_B pins (Pin 2 and 12 of J4 and Pin 2 of J3).
5. Apply the RF signal to the RFIN connector of the EVAL-ADPA9007.

POWER-DOWN SEQUENCE

Take the following steps to power down:

1. Turn off the RF signal
2. Set the gate voltage (V_{GG1}) to –2 V
3. Set the supply voltage (V_{DD}) to 0 V
4. Set the VREF_B, VBTEMP, and VDET_B pins to 0 V
5. Increase the VGG1 pin to 0 V

OPERATING THE ADPA9007-EVALZ

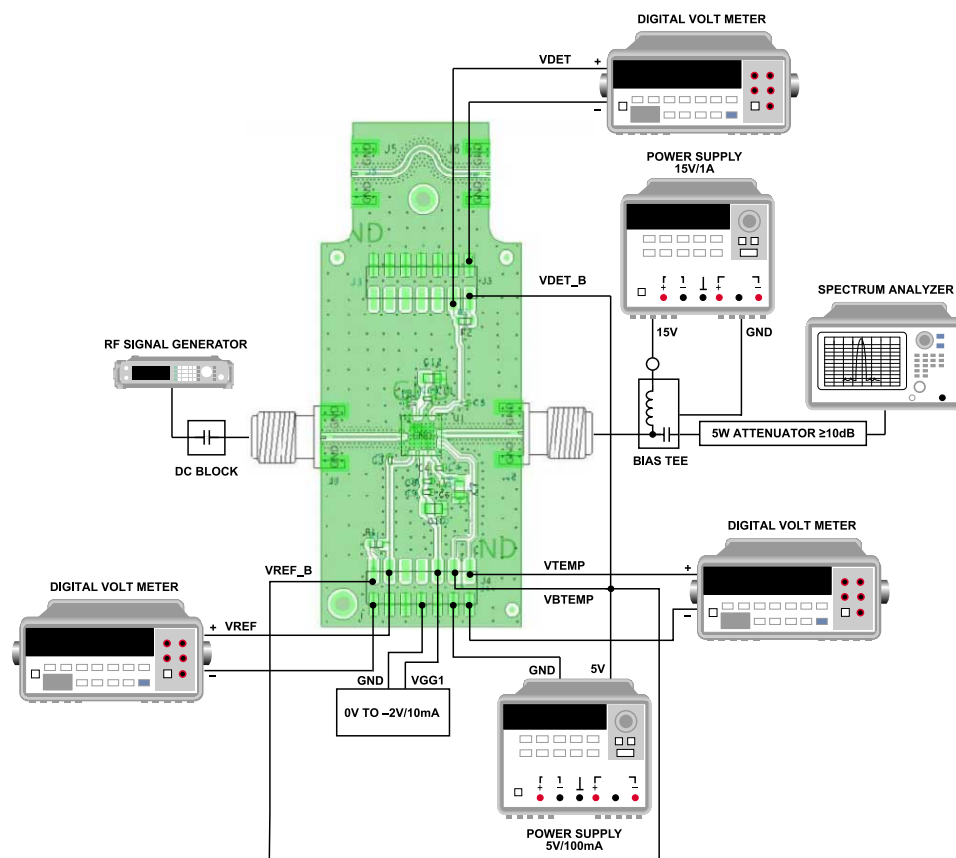


Figure 3. Operation Connections

OPERATING THE ADPA9007-EVALZ

THROUGH CALIBRATION PATH

To calibrate out board trace losses, a through calibration path is provided.

J5 and J6 must be populated with 2.92 mm RF connectors to use the through calibration path.

Figure 4 shows the plot of the data in Table 2 of the through calibration path (J5 to J6). See Figure 5 for the evaluation board schematic.

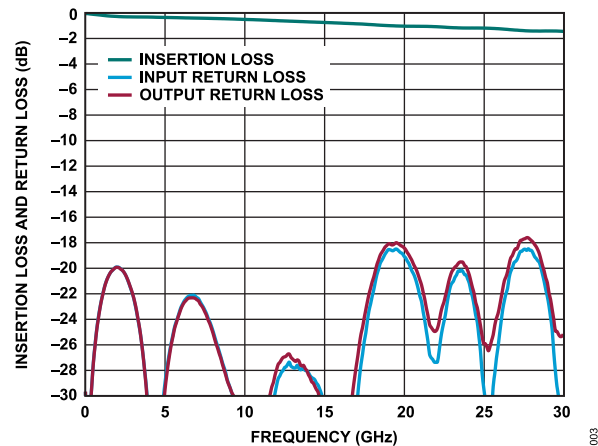


Figure 4. Insertion Loss of Through Calibration Path

Table 2. Insertion Loss of Through Calibration Path

| Frequency (GHz) | Insertion Loss (dB) |
|-----------------|---------------------|
| 0.01 | -0.05 |
| 0.5 | -0.10 |
| 1 | -0.17 |
| 2 | -0.27 |
| 5 | -0.35 |
| 10 | -0.51 |
| 15 | -0.74 |
| 20 | -1.03 |
| 25 | -1.19 |
| 28 | -1.41 |
| 30 | -1.44 |

Figure 5. ADPA9007-EVALZ Evaluation Board Schematic

EVALUATION BOARD SCHEMATIC AND ARTWORK

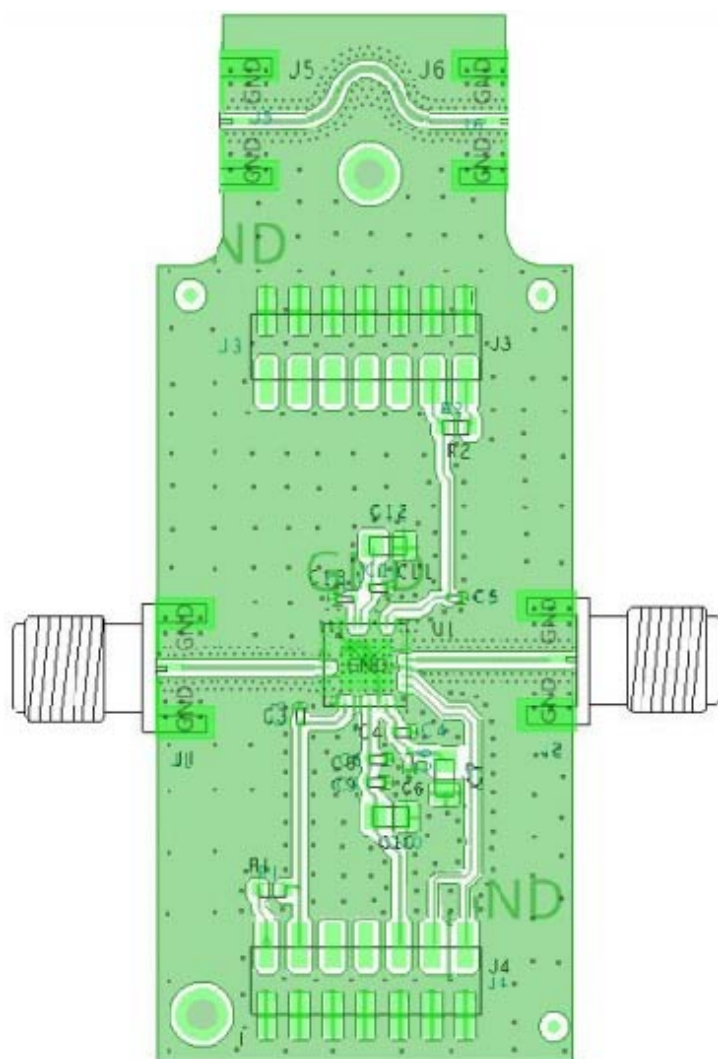


Figure 6. ADPA9007-EVALZ Assembly Drawing (J5 and J6 Are Not Installed)

ORDERING INFORMATION

BILL OF MATERIALS

Table 3.

| Reference Designator | Description | Manufacturer | Part Number |
|----------------------|--|-------------------------|-------------------------------|
| C7, C10, C12 | Ceramic capacitors, 4.7 μ F, 50 V, 10%, X5R, 0805, low effective series resistance | TDK Corporation | C2012X5R1H475K125AB |
| C6, C9, C11 | Ceramic capacitors, 0.01 μ F, 25 V, 10%, X7R, 0402 | KEMET Corporation | C0402C103K3RACTU |
| C8, C13 | Ceramic capacitors, 100 pF, 50 V, 5%, C0G, 0402 | YAGEO | CC0402JRNPO9BN101 |
| C3, C5 | Ceramic capacitors, 10 pF, 50 V, 5%, C0G, 0402 | Johanson Dielectrics | 500R07N100JV4T |
| J1, J2 | Edge launch jack connectors | Winchester Interconnect | 25-146-1000-92 |
| J3, J4 | PCB connection header, 2 mm pitch, dual row with peg, 0.5 mm square post and 3.8 mm long | Molex | 87759-1450 |
| U1 | GaAs, pHEMT, 2 W, DC to 28 GHz power amplifier | Analog Devices, Inc. | ADPA9007ACGZN |
| C4 | Ceramic capacitor, 100 pF, 50 V, 5%, C0G, 0402 (not installed) | YAGEO | CC0402JRNPO9BN101 |
| J5, J6 | Edge launch jack connectors (not installed) | Winchester Interconnect | 25-146-1000-92 |
| R1, R2 | Resistors, 40.2 k Ω , 1%, 1/10 W 0603 AEC-Q200 | Vishay | CRCW060340K2FKEA |
| Not applicable | Aluminum heat spreader, 2.51 in \times 1.9 in | Not applicable | Not applicable |

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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