Evaluating the ADRF5532, 2.3 GHz to 2.7 GHz, Receiver Front End

FEATURES

- Full featured evaluation board for the ADRF5532
- Easy connection to test equipment
- Thru line for calibration

EQUIPMENT NEEDED

- DC power supplies
- Network analyzer

GENERAL DESCRIPTION

The ADRF5532 is an integrated RF, front-end multichip module designed for time division duplex (TDD) applications. The device operates from 2.3 GHz to 2.7 GHz. The ADRF5532 is configured with a low-noise amplifier (LNA) and a high-power, silicon, single pole double throw (SPDT) switch.

This user guide describes the ADRF5532-EVALZ, designed to easily evaluate the features and performance of the ADRF5532. Figure 1 shows a photograph of the ADRF5532-EVALZ.

Note that the ADRF5532 IC is populated on the ADRF5534 bare evaluation board. However, the whole assembly is the ADRF5532-EVALZ

Full details about the device are available in the ADRF5532 data sheet. Consult it when using the ADRF5532-EVALZ.

EVALUATION BOARD PHOTOGRAPH

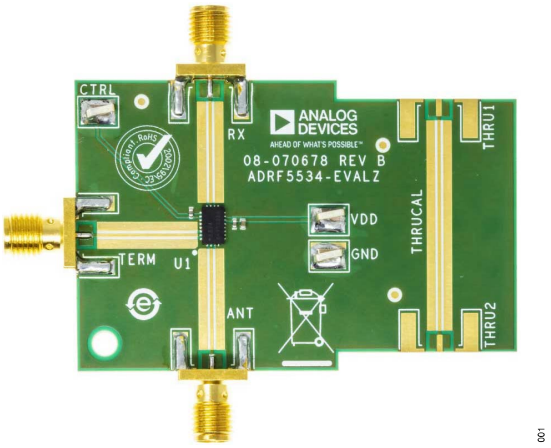

Figure 1. Evaluation Board Photograph

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REVISION HISTORY

3/2024—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

OVERVIEW

The ADRF5532-EVALZ is preinstalled with connectors (end launch subminiature version A (SMA)) and assembled with the ADRF5532 and its application circuitry. All components are placed on the primary side of the ADRF5532-EVALZ. Figure 8 shows an assembly drawing for the ADRF5532-EVALZ. Figure 9 provides an ADRF5532-EVALZ schematic.

LAYOUT

The ADRF5532-EVALZ is designed using RF circuit design techniques on an 8-layer printed circuit board (PCB). Figure 2 shows the PCB stack-up.

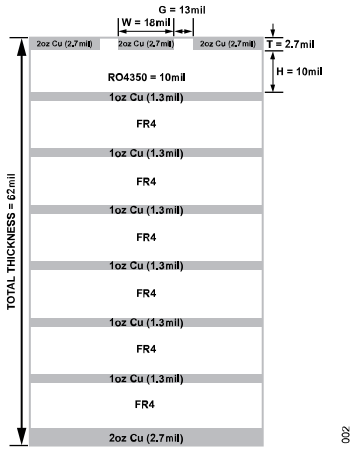

Figure 2. Evaluation Board Stack-Up

The outer copper layers are 2 oz (2.7 mil) thick and the inner layers are 1 oz (1.3 mil) thick. The top dielectric material is 10 mil Rogers 4350B, which provides 50 Ω controlled impedance and optimizes high-frequency performance. The remaining six dielectric layers are FR4 based filler layers that improve the mechanical strength of the ADRF5532-EVALZ and meet the overall board thickness of 62 mil.

All RF traces are routed on the top layer, and the remaining seven layers are ground planes that provide a solid ground for RF transmission lines and help to manage thermal rise on the ADRF5532-EVALZ during high-power operations.

The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a width of 18 mil and a ground spacing of 13 mil to have a characteristic impedance of 50 Ω. Ground via fences are arranged on both sides of a CPWG to improve isolation between nearby RF lines and other signal lines.

The exposed ground pad of the ADRF5532, which is soldered on the PCB ground pad, is the main thermal conduit for heat dissipation. The PCB ground pad is densely populated with filled through vias to provide the lowest possible thermal resistance path temperature from the top to the bottom of the PCB. The connections from the package ground leads to ground are kept as short as possible.

RF INPUTS AND OUTPUTS

The ADRF5532-EVALZ has five edge-mounted SMA connectors for the RF inputs and outputs, as shown in Table 1. The SMA connectors on the thru line are not populated by default and can be connected to measure and calibrate the evaluation board loss effects. Use the thru line on THRU1 and THRU2 to calibrate the ANT, TERM, and RX evaluation board loss.

Table 1. RF Inputs and Outputs

SMA Connectors	Description
ANT	Antenna input
TERM	Termination output
RX	Receiver output
THRU1	Thru line input or output, DNI
THRU2	Thru line input or output, DNI

POWER SUPPLY AND CONTROL INPUTS

The ADRF5532-EVALZ has one power-supply input, one control input, and one ground, as shown in Table 2. The DC test points are populated on the V_{DD}, CTRL, and GND test points.

A single 5 V supply is connected to the DC test point on the V_{DD} test point. Ground reference can be connected to the GND test point. The typical total current consumption for the ADRF5532 is 118 mA in receive operation. The supply pin of the ADRF5532-EVALZ is decoupled with 100 pF and 4.7 µF capacitors.

A single 5 V supply is connected to the DC test point on the CTRL test point. The control pin of the ADRF5532-EVALZ is decoupled with 100 pF. When no connection is made to the CTRL control input, the RF channel is in termination mode with LNA powered down.

Table 2. Test Points for Power Supply and Control Inputs

Test Points	Description
V_{DD}	Positive supply voltage
CTRL	Transmit/receive control logic input
GND	Ground

TEST PROCEDURE

BIASING SEQUENCE

To bias up the ADRF5532-EVALZ, perform the following steps:

1. Ground the GND test point.
2. Bias up V_{DD} test point.
3. Bias up the CTRL test point.
4. Apply an RF input signal.

The ADRF5532-EVALZ is shipped fully assembled and tested. Figure 3 provides a basic test setup diagram to evaluate the s-parameters (receive gain, transmit insertion loss and isolation, and RF input and output return losses) using a network analyzer. Note that PSU in Figure 3 means power supply unit. Perform the following steps to complete the test setup and verify the operation of the ADRF5532-EVALZ:

1. Connect the GND test point to the ground terminal of the power supply.
2. Connect the V_{DD} test point to the voltage output terminal of the 5 V supply that sources a current of approximately 118 mA in receive operation or 15 mA for transmit operation.
3. Connect the CTRL test point to the voltage output terminal of the 5 V supply for receive operation. The ADRF5532-EVALZ can be configured in different modes by connecting the CTRL control test point to 5 V or ground, as shown in Table 3.
4. Connect a calibrated network analyzer to the ANT, TERM, and RX SMA connectors. Sweep frequency from 1 GHz to 6 GHz and set power to −25 dBm.
5. The ADRF5532-EVALZ is expected to have a receive gain of 35.5 dB and transmit insertion loss of 0.7 dB at 2.6 GHz. See the expected results in Figure 4 to Figure 6.

Table 3. Truth Table: Signal Path Selection

	Signal Path Selection	
CTRL	Transmit Operation (ANT to TERM)	Receive Operation (ANT to RX)
Low	On	Off, LNA powered down
High	Off, isolation state	On

Additional test equipment is needed to fully evaluate the device functions and performance.

For noise figure evaluation, use either a noise figure analyzer or a spectrum analyzer with noise option. The use of a low excess noise ratio (ENR) noise source is recommended.

For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high isolation power combiner is recommended.

For power compression and power handling evaluations, use a two-channel power meter and a signal generator. A power amplifier with great enough power is recommended at the input. Test accessories such as couplers and attenuators must have enough power handling.

The ADRF5532-EVALZ comes with a support plate attached to the bottom side. To ensure maximum heat dissipation and to reduce thermal rise on the ADRF5532-EVALZ during high-power evaluations, the support plate must be attached to a heatsink using thermal grease.

Note that the measurements performed at the SMA connectors of the ADRF5532-EVALZ include the losses of the SMA connectors and the PCB. The thru line must be measured to calibrate out the ADRF5532-EVALZ effects. The thru line is the summation of an RF input line and an RF output line connected to the device and equal in length.

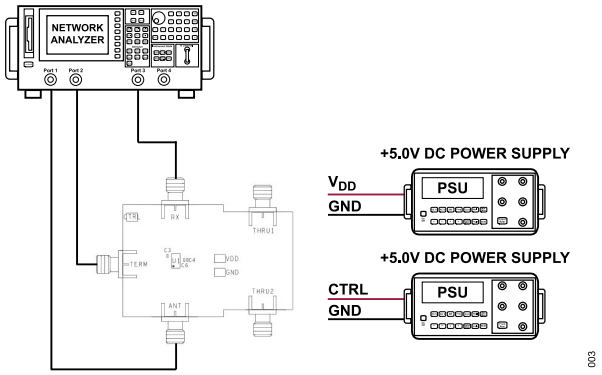

Figure 3. Test Setup Diagram

TEST PROCEDURE

EXPECTED RESULTS

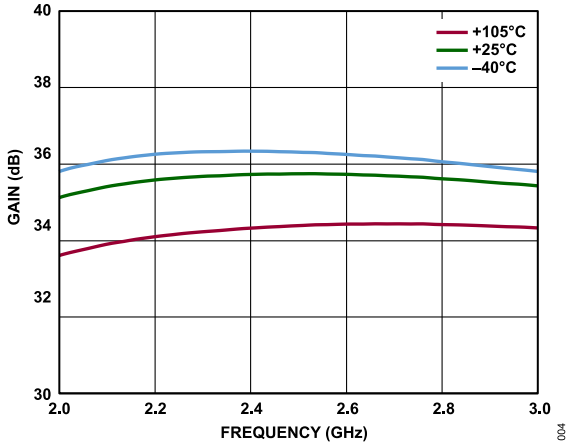

Figure 4. Gain vs. Frequency at Various Temperatures

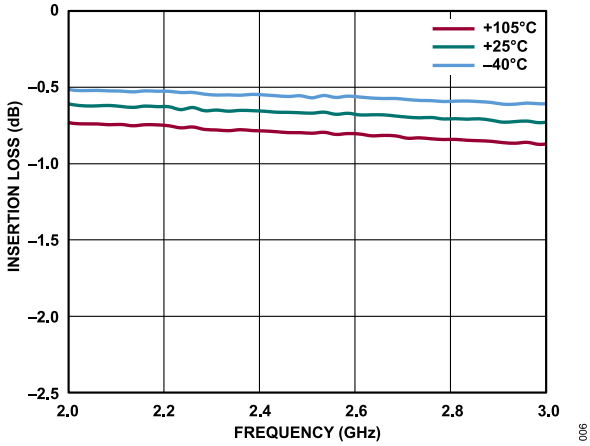

Figure 6. Insertion Loss vs. Frequency at Various Temperatures

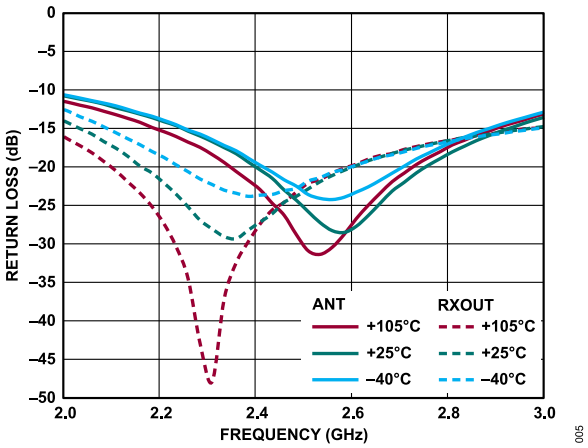

Figure 5. Receive Mode Return Loss vs. Frequency at Various Temperatures

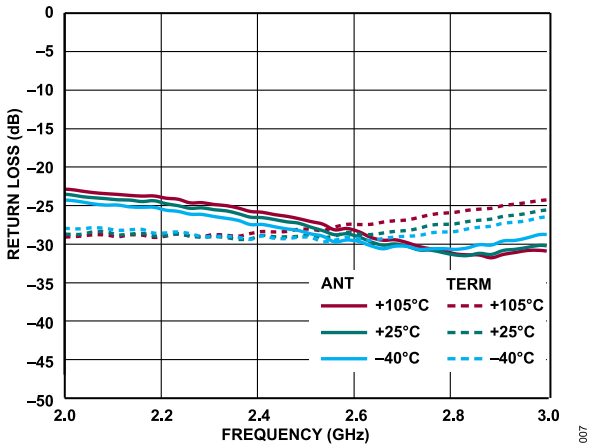

Figure 7. Transmit Mode Return Loss vs. Frequency at Various Temperatures

EVALUATION BOARD ARTWORK AND SCHEMATIC

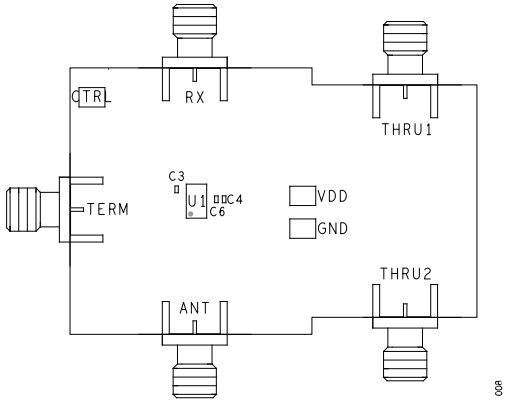

Figure 8. Assembly Diagram

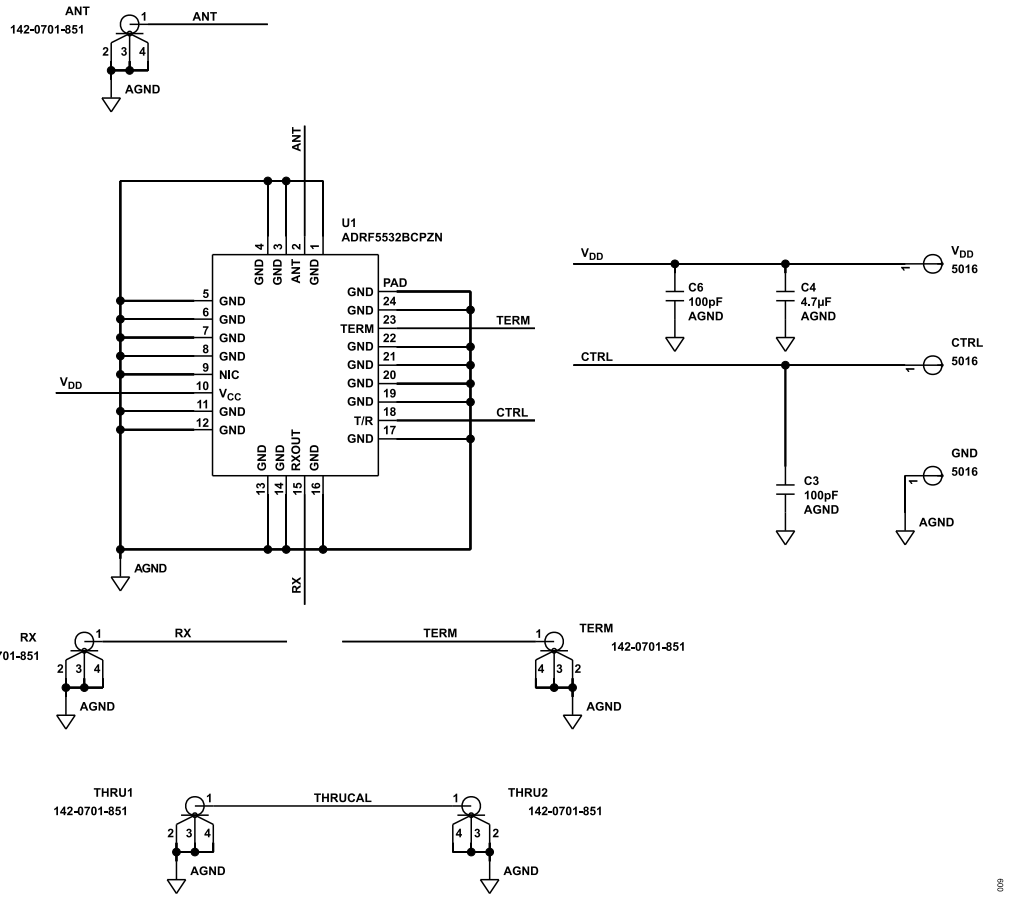

Figure 9. Schematic

ORDERING INFORMATION

BILL OF MATERIALS

Reference Designator	Description	Manufacturer	Part Number
ANT, RX, TERM	PCB mount SMA connectors	Johnson/Cinch Connectivity Solutions	142-0701-851
THRU1, THRU2	PCB mount SMA connectors, do not install (DNI)	Johnson/Cinch Connectivity Solutions	142-0701-851
C3, C6	100 pF capacitors, 50 V, 0402 package	KEMET	C0402C101J5GACTU
C4	4.7 µF capacitors, 10 V, 0402 package	TDK	C1005X5R1A475K050BC
CTRL, V_{DD}, GND	Surface-mount test points	Keystone Electronics	5016
U1	2.3 GHz to 2.7 GHz, receiver front end	Analog Devices, Inc.	ADRF5532
PCB	Printed circuit board	Analog Devices, Inc.	08-070678B

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.