Evaluating the ADuM4146 11 A High Voltage Isolated Bipolar Gate Driver in Half Bridge Configuration

FEATURES

- Optimized for use with Wolfspeed SiC MOSFETs and power modules
- Compatible with Wolfspeed SpeedVal Kit™
- Compatible with Wolfspeed CIL test boards and half bridge evaluation boards
- High frequency, ultrafast switching operation
- Input and output side UVLO
- Short-circuit protection
- Shoot-through protection interlock
- Internal Miller clamp
- Differential inputs for increased noise immunity
- Fault and ready indicators
- Isolated NTC thermistor measurement

EVALUATION KIT CONTENTS

- EVAL-ADuM4146WHB1Z evaluation board

EQUIPMENT NEEDED

- Wolfspeed SpeedVal Kit modular evaluation platform
  - For double pulse testing and high power testing
- For evaluating Wolfspeed half-bridge modules
  - CAB011M12FM3 or CAB016M12FM3
  - Wolfspeed CIL board (KIT-CRD-CIL12N-FMA)
- For evaluating Wolfspeed six-pack modules
  - CCB021M12FM3 or CCB032M12FM3
  - Wolfspeed CIL board (KIT-CRD-CIL12N-FMC)
- CGD12HB00D differential transceiver board
  - Differential outputs for improved noise immunity

DOCUMENTS NEEDED

- ADuM4146 data sheet

GENERAL DESCRIPTION

The EVAL-ADuM4146WHB1Z is a half bridge gate drive board that allows simple evaluation of the performance of the ADuM4146 when driving advanced Wolfspeed third generation C3M™ silicon carbide (SiC) metal-oxide semiconductor field-effect transistors (MOSFETs) and power modules. The EVAL-ADuM4146WHB1Z is intended to be used with Wolfspeed SpeedVal Kit, clamped inductive load (CIL) test boards, half bridge evaluation boards, and a differential transceiver board.

The EVAL-ADuM4146WHB1Z has an isolated return channel that is configured to read a negative temperature coefficient (NTC) thermistor and provide a variable frequency output corresponding to the resistance and temperature of the NTC.

The control and input interface for the EVAL-ADuM4146WHB1Z uses RS-422 signaling for improved noise and disturbance immunity and includes a 12 V power input.

For full details on the ADuM4146, see the ADuM4146 data sheet, which must be consulted when using the EVAL-ADuM4146WHB1Z.

EVALUATION BOARD PHOTOGRAPHS

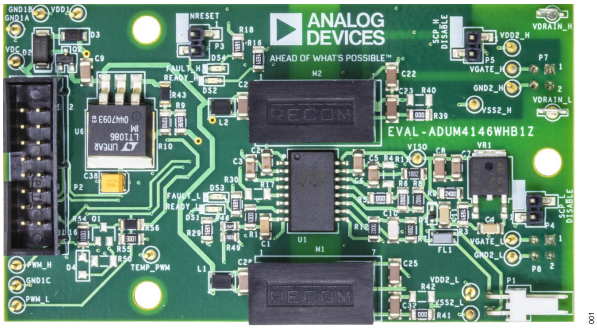

Figure 1. Evaluation Board Photograph, Top

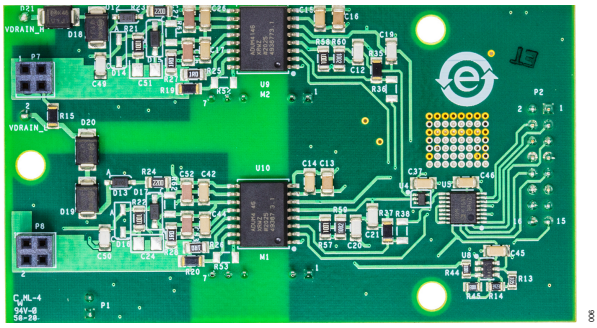

Figure 2. Evaluation Board Photograph, Bottom

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REVISION HISTORY

5/2023—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

LOGIC SIDE DIFFERENTIAL INTERFACE

The P2 logic side interface connector is a 16-position, 100 mil (2.54 mm) pitch, dual row header that is compatible with standard insulation displacement contact (IDC) connectors. The pinout for this interface is described in Table 1.

Table 1. Control Interface (P2) Pinout

Pin No.	Parameter[1]	Description
1	V_{DC}	12 V nominal power supply input.
2	Common	Common.
3	HS-P	Positive line of the 5 V differential, high-side, pulse-width modulation (PWM) signal pair.
4	HS-N	Negative line of the 5 V differential, high-side, PWM signal pair.
5	LS-P	Positive line of the 5 V differential, low-side, PWM signal pair.
6	LS-N	Negative line of the 5 V differential, low-side, PWM signal pair.
7	$\overline{\text{FAULT}}$−P	Positive line of the 5 V differential, fault condition, output signal pair.
8	$\overline{\text{FAULT}}$−N	Negative line of the 5 V differential, fault condition, output signal pair.
9	RTD-P	Positive line of the 5 V differential, temperature dependent resistor, output signal pair.
10	RTD-N	Negative line of the 5 V differential, temperature dependent resistor, output signal pair.
11	No connection	No connection.
12	Common	Common.
13	No connection	No connection.
14	Common	Common.
15	$\overline{\text{RESET}}$	Active low reset pin to clear fault. Bring low for at least 700 ns to clear fault and return high to allow the driver to resume operation.
16	Common	Common.

[1] Pin 3 to Pin 10 are differential pairs.

OUTPUT CONNECTIONS TO POWER SWITCH

The P7 and P8 output connectors connect to the power switch interface board using a 4-position header, 100 mil (2.54 mm) pitch, through hole, gold plated connector (Samtec ESQ-102-xx-L-D series).

When using the EVAL-ADuM4146WHB1Z with a Wolfspeed XM3 module, use the long connector (Samtec ESQ-102-33-L-D) to clear the bus bars located between the module and the EVAL-ADuM4146WHB1Z.

When using the EVAL-ADuM4146WHB1Z with a baseplateless module interface board, use the short connector (Samtec ESQ-102-12-L-D) to reduce the gate source path length.

The EVAL-ADuM4146WHB1Z comes with the short connector by default.

DRAIN VOLTAGE SENSE FOR SHORT-CIRCUIT PROTECTION (SCP)

The EVAL-ADuM4146WHB1Z SCP feature uses the drain voltage of the switch to detect the short-circuit condition. The VDRAIN_H (high-side) and VDRAIN_L (low-side) connectors are 0.110 inch (2.97 mm), quick connect male pins that must be connected to the associated switch drain.

To prevent errors in the measurement of the drain voltage, minimize the parasitic inductance between the drain and source measurement points when connecting to the switch. Kelvin style connections are encouraged.

In a traditional half bridge configuration, the low-side drain is connected to the high-side source. The EVAL-ADuM4146WHB1Z includes a 0 Ω resistor, R15, that connects VRDRAIN_L to the high-side source. When R15 is present, only the VDRAIN_H connection must be made and VDRAIN_L can be open circuited.

NTC THERMISTOR TEMPERATURE FEEDBACK

The EVAL-ADuM4146WHB1Z provides a varying frequency square wave on Pin 9 and Pin 10 of the P2 interface connector that is related to the resistance of an NTC thermistor. Note that one terminal of the thermistor is electrically connected to the low-side switch source.

The ADuM4190 isolated amplifier measures the voltage generated by the biased NTC thermistor and provides a scaled voltage that is galvanically isolated from the thermistor. The LTC6990 voltage-controlled oscillator (VCO) generates a varying frequency square wave based on this scaled voltage.

Table 2 shows the output frequency as a function of the NTC temperature when the EVAL-ADuM4146WHB1Z NTC input is connected to a Littelfuse SM502F1K NTC thermistor.

The temperature reported by the NTC differs largely from the junction temperature of the SiC MOSFETs. Therefore, it is not recommended to use the temperature reported by the NTC as an accurate junction temperature measurement.

Table 2. Temperature to Output Frequency

NTC Thermistor Temperature (°C)	NTC Thermistor Resistance (Ω)	Output Frequency (kHz)
0	14,283	6.71
25	5,000	20.38
50	2,059	30.29
75	963	35.70
100	499	38.45
125	281	39.85
150	169	40.60
175	108	41.02

EVALUATION BOARD HARDWARE

CONFIGURATION JUMPERS AND RESISTORS

Manual Reset

The reset function for the high-side and low-side gate drivers can be manually controlled by using the P3 jumper. Placing a 100 mil (2.54 mm) jumper on P3 overrides the state of the reset input by forcing the $\overline{\text{RESET}}$ pin low. Remove the jumper to allow the gate drivers to function.

SCP Disable

The SCP circuitry can be manually disabled by inserting a 100 mil (2.54 mm) jumper on P5 (high-side) or P4 (low-side). Remove the jumper to allow the SCP circuitry to function.

Shoot-Through Protection Interlock

The shoot-through protection interlock feature of the ADuM4146 can be enabled or disabled based on the population of the R35 and R36 resistors (high-side) or R37 and R38 resistors (low-side). This interlock only allows one switch, high-side or low-side, to be on at a time. Attempting to turn both switches on at the same time when the interlock is enabled results in both switches turning off.

Populating R35 or R37 with a 1206 package, 0 Ω resistor (and depopulating R36 or R38) disables the shoot-through protection interlock of the associated gate driver.

Populating R36 or R38 with a 1206 package, 0 Ω resistor (and depopulating R35 or R37) enables the shoot-through protection interlock of the associated gate driver.

The EVAL-ADuM4146WHB1Z by default has the shoot-through protection interlock disabled for both the high-side and low-side gate drivers.

DIAGNOSTIC LIGHT-EMITTING DIODES (LEDS)

The states (ready and fault) of the ADuM4146 gate drivers are indicated by different diagnostic LEDs.

Ready

The green LEDs, DS1 (low-side) and DS2 (high-side), turn on when the associated gate driver is in the ready state. The gate driver is in the ready state when the logic and isolated side supply voltages are above their undervoltage lockout (UVLO) level and there is no SCP fault. The green LEDs are off if either supply is below its UVLO threshold or there is an SCP fault.

Fault

The red LEDs, DS3 (low-side) and DS4 (high-side), turn on when the associated gate driver is in an SCP fault state and the gate output is driven low. The gate driver is in the fault state when it experiences an overcurrent event that needs to be cleared along with the completion of a reset cycle.

TEST POINTS

The EVAL-ADuM4146WHB1Z contains test points that allow the testing and monitoring of key signals on the gate drive board.

EVALUATION BOARD HARDWARE

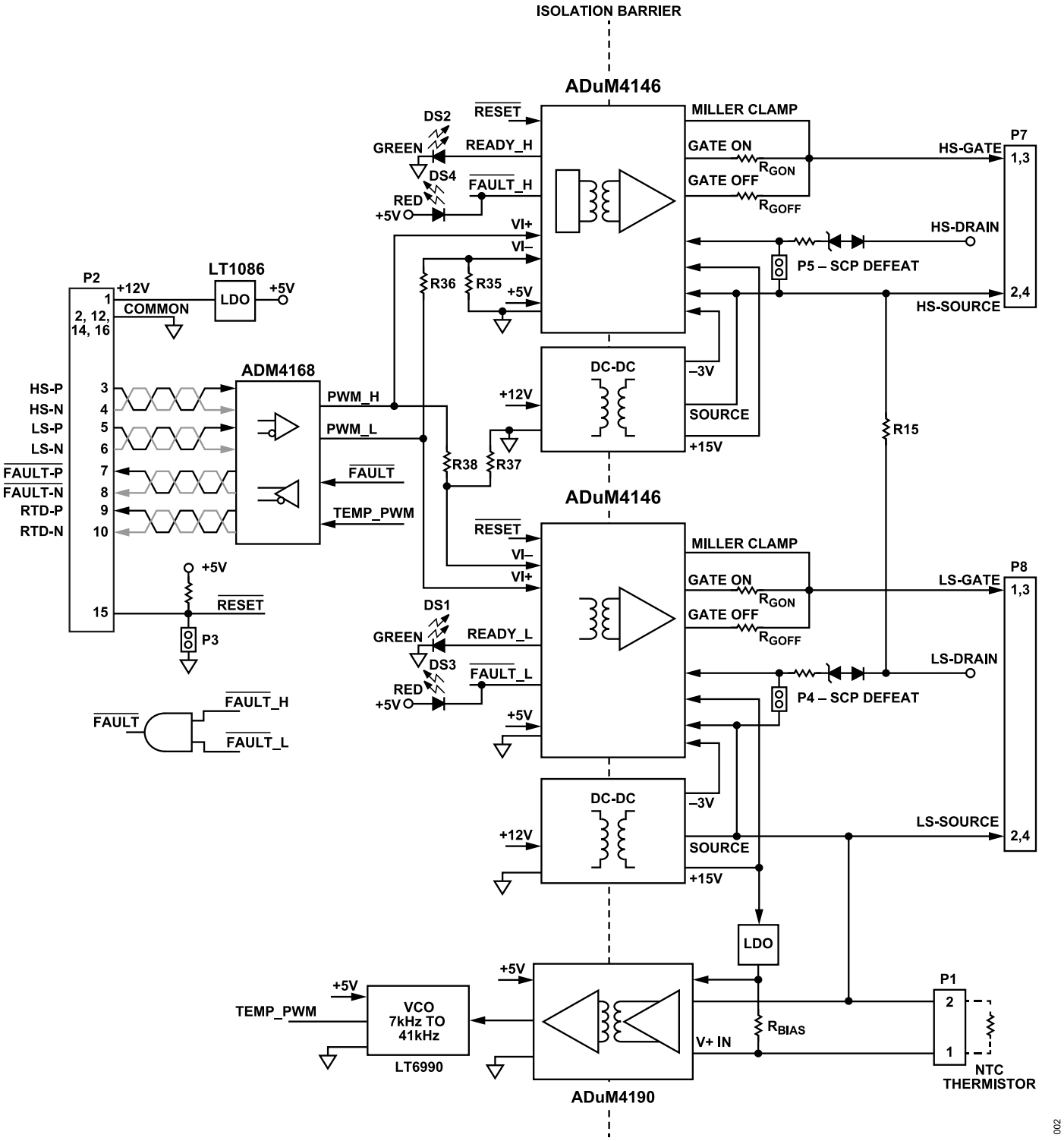

Figure 3. Functional Block Diagram

EVALUATION BOARD HARDWARE

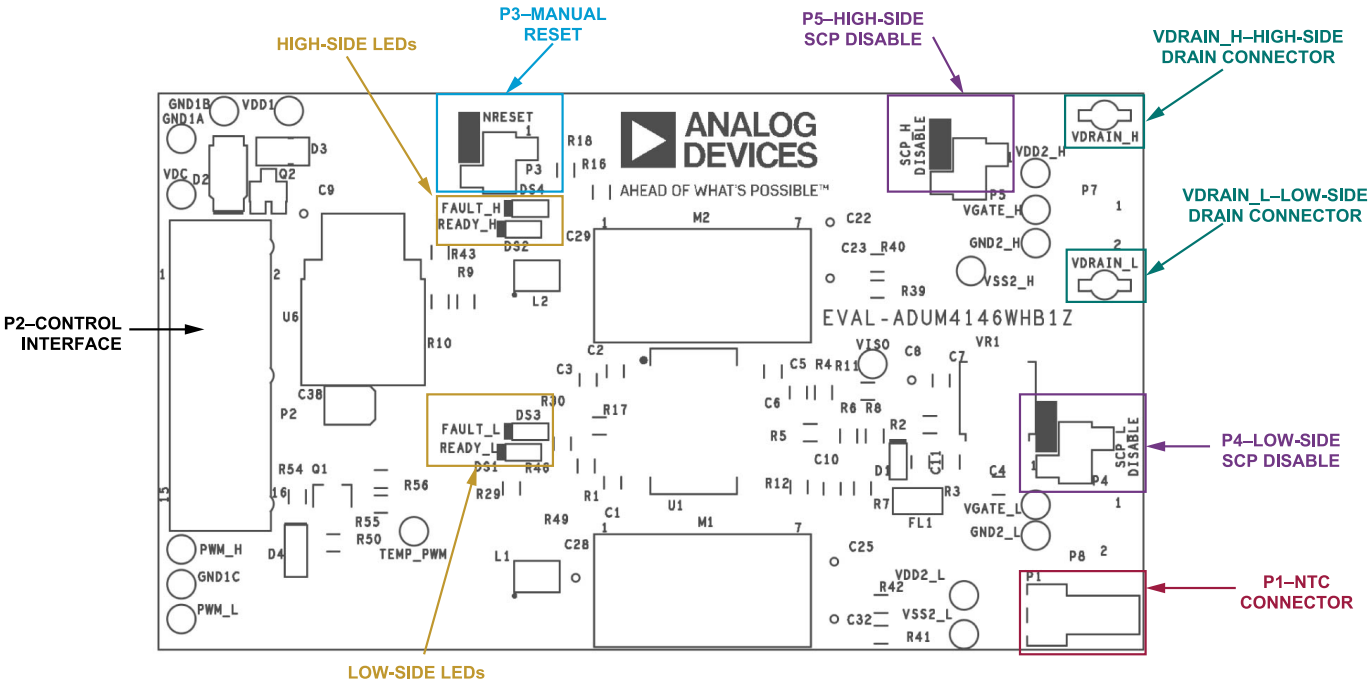

Figure 4. Top Side Feature Locations

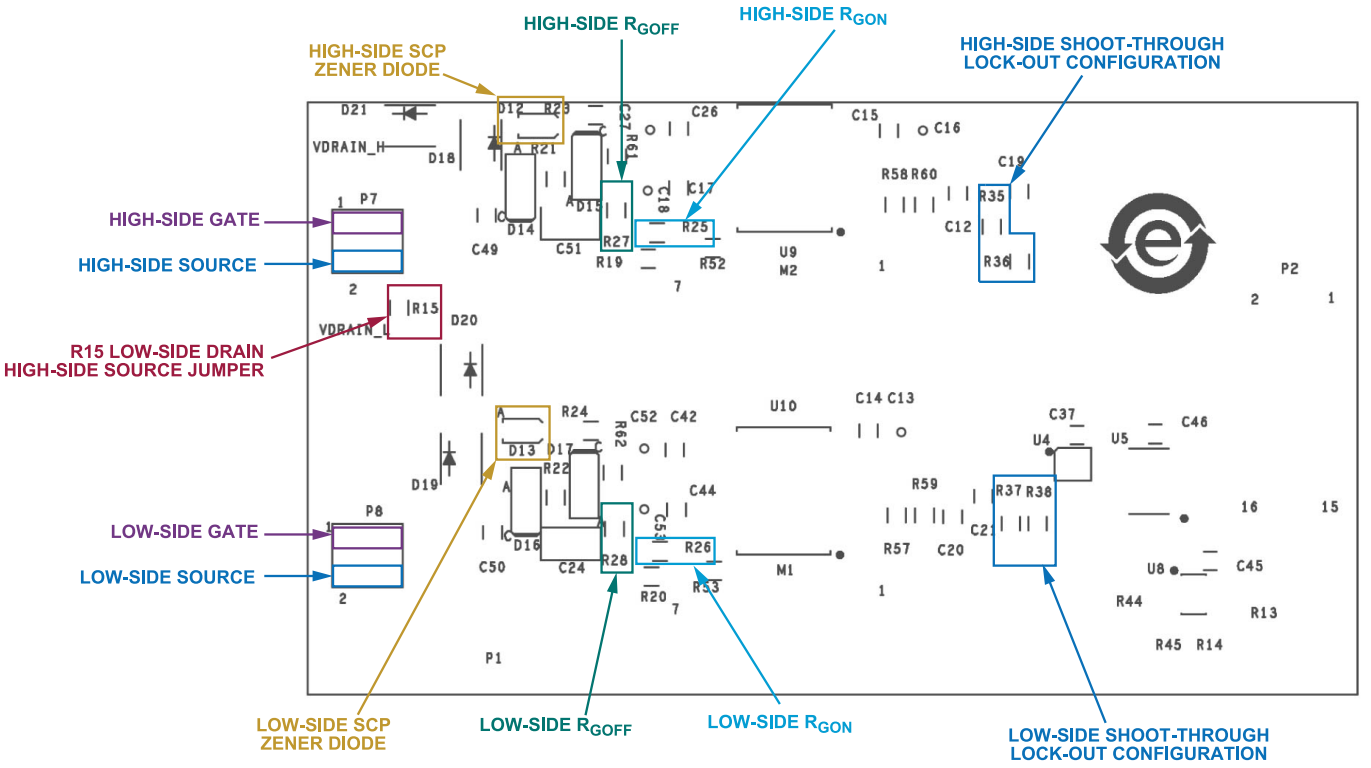

Figure 5. Bottom Side Feature Locations

BOARD USE AND CONFIGURATION

GATE DRIVE RESISTOR SELECTION

The ADuM4146 provides two output nodes for driving a switch. The benefit of this approach is that the user can select two separate series resistances, one for the turn on and one for the turn off, which allows different time for turn on and turn off. It is generally desired to have the turn off occur faster than the turn on.

To select the series resistance, choose the maximum allowed peak current (I_{PEAK}) for the switch. Knowing the voltage swing on the gate, as well as the internal resistance of the gate driver, an external gate resistor (R_{GOFF} or R_{GON}) can be chosen.

$$I_{PEAK} = (V_{DD2} - V_{SS2}) / (R_{DSON\_N} + R_{GOFF}) \quad (1)$$

where R_{DSON_N} is the pull-down NMOS on resistance.

Solve for R_{GOFF} using the following equation:

$$R_{GOFF} = ((V_{DD2} - V_{SS2}) - I_{PEAK} \times R_{DSON\_N}) / I_{PEAK} \quad (2)$$

For example, if the turn off peak current is 4 A with a nominal R_{DSON_N} value of 0.6 Ω and a (V_{DD2} − V_{SS2}) value of 18 V, the value is calculated as follows:

$$R_{GOFF} = (18\ V - 4\ A \times 0.6\ \Omega) / 4\ A = 3.9\ \Omega \quad (3)$$

After R_{GOFF} is selected, a slightly larger R_{GON} can be selected to arrive at a slower turn on time.

If the selected switch has a nonzero internal gate resistance (R_G), then this resistance must be subtracted from the calculated R_{GOFF} to arrive at the final R_{GOFF}.

The EVAL-ADuM4146WHB1Z is intended to work with Wolfspeed baseplateless modules with an internal R_G range of 2.4 Ω to 3.2 Ω, which suggests a final R_{GOFF} in the range of 0.7 Ω to 1.5 Ω. As a compromise to work with either module, the EVAL-ADuM4146WHB1Z has a default value of R_{GOFF} = R_{GON} = 1 Ω.

POWER DISSIPATION

The power dissipation by the gate driver is a function of the switch gate charge, switching frequency, and gate voltage swing. For one channel, the power dissipation is calculated using the following equation:

$$P_{DISS} = Q_G \times f_{SW} \times (V_{DD2} - V_{SS2}) \quad (4)$$

where:
P_{DISS} is the power dissipation of high-side or low-side gate driver.
Q_G is the switch gate charge.
f_{SW} is the switching frequency.
V_{DD2} and V_{SS2} are the isolated supply voltages.

For the EVAL-ADuM4146WHB1Z, V_{DD2} = 15 V and V_{SS2} = −3 V.

SCP TUNING

The SCP method used by the EVAL-ADuM4146WHB1Z is similar in structure and behavior to the desaturation detection circuit commonly used with insulated gate bipolar transistor (IGBTs). The SCP circuit measures the drain source voltage (V_{DS}) of the MOSFET starting a short time after the switch has turned on. If this measured voltage is above a threshold, the SCP circuit determines that a fault is present and turns off the switch using a soft turn off. After initiating the soft turn off, the SCP circuit asserts the fault status line and normal gate drive operation is locked out until the gate driver is reset.

The SCP threshold is set by the internal comparator of the ADuM4146 and the components on the EVAL-ADuM4146WHB1Z. The ADuM4146 comparator threshold is 9.2 V. However, the effective SCP threshold is lower due to the SCP sensing network shown in Figure 6.

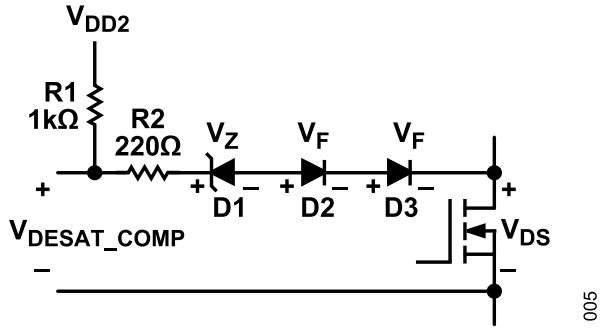

Figure 6. SCP Sensing Network

Diode D1 to Diode D3 (see Figure 6) effectively lower the comparator threshold. Therefore, the drain source voltage that triggers the SCP circuit can be adjusted by selecting the desired Zener voltage for D1.

The comparator input voltage (V_{DESAT_COMP}) is equal to the following:

$$V_{DESAT\_COMP} = \frac{R2}{R1 + R2} \times V_{DD2} + \frac{R1}{R1 + R2} \times (V_Z + 2V_F + V_{DS}) \quad (5)$$

where:
V_Z is the Zener voltage.
V_F is the forward voltage.

For the EVAL-ADuM4146WHB1Z, with V_{DD2} = 15 V, R1 = 1 kΩ, and R2 = 220 Ω, the drain source voltage that trips the SCP comparator (V_{DS_TRIP}) is solved with the following equation:

$$V_{DS\_TRIP} = V_{DESAT\_COMP} - 2.70 - 0.82\ V_Z - 1.64\ V_F \quad (6)$$

Assuming the forward voltage of the blocking diodes is approximately 0.5 V, and the default selected Zener voltage is 1.8 V, the trip voltage is approximately 4.2 V.

BOARD USE AND CONFIGURATION

When selecting a suitable SCP level, the drain current (I_D) vs. V_{DS} output characteristic of the switch must be used along with the peak transient current to find the minimum V_{DS_TRIP}, which can then be used with the previous equation to select a suitable tuning Zener diode.

To prevent the SCP circuit from tripping when the gate is asserted, the drain connections, VDRAIN_H and VDRAIN_L, must be connected to their associated switch drain. Alternatively, the SCP circuits can be independently disabled by placing a 100 mil (2.54 mm) jumper on P4 (low-side) and/or P5 (high-side).

EVALUATION BOARD DESIGN FILES

Schematic, layout, BOM, and fab files can be found in the EVAL-ADuM4146WHB1Z landing page.

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.