EV1HMC8074LP6G Evaluation Board User Guide
UG-1800

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Evaluating the HMC8074 Quad Band, MMIC, VCO, 8.3 GHz to 15.2 GHz

FEATURES

- Self contained board that includes the following
  - HMC8074 low noise, quad band, VCO
  - ADG1604 4:1 multiplexer, filtering options
  - LT3042 voltage regulator
  - Header connectivity to allow use of Arduino Uno or Linduino microcontroller
- Externally powered by a single 6.0 V supply

EVALUATION KIT CONTENTS

EV1HMC8074LP6G evaluation board

EQUIPMENT NEEDED

- 6.0 V power supply
- Low noise, variable, 0 V to 13.0 V power supply
- 50 Ω termination
- Spectrum analyzer (optional)
- Signal source analyzer

ONLINE RESOURCES

- HMC8074 data sheet
- Linduino DC2026C demo manual

GENERAL DESCRIPTION

The EV1HMC8074LP6G evaluates the performance of the HMC8074 low noise, quad band, monolithic microwave integrated circuit (MMIC), voltage controlled oscillator (VCO). Figure 1 shows a photograph of the EV1HMC8074LP6G. The EV1HMC8074LP6G contains the HMC8074 VCO, an LT3042 ultralow noise voltage regulator, jumpers, an ADG1604 4:1 multiplexer, and Subminiature Version A (SMA) and 2.92 mm K connectors.

For full details on the HMC8074, see the HMC8074 data sheet, which must be consulted in conjunction with this user guide when using the EV1HMC8074LP6G.

EVALUATION BOARD PHOTOGRAPH

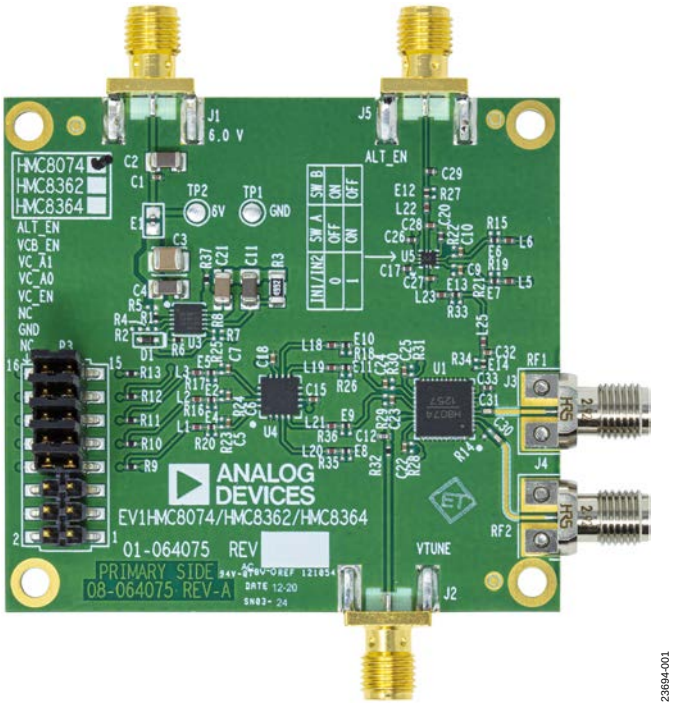

Figure 1.

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REVISION HISTORY

9/2020—Revision 0: Initial Version

GETTING STARTED

EVALUATION BOARD SETUP PROCEDURE

To configure the EV1HMC8074LP6G for the first time, perform the following steps:

1. Verify that the power supply used for analog power can output 6.0 V and 200 mA of compliance current.
2. Disable the power supply output for now or damage may occur.
3. Connect the power supply (analog) to J1 using a double shielded Bayonet Neill–Concelman (BNC) cable and a BNC to SMA adapter.
4. Use the supplied shorting jumpers to configure the logic, as shown in Figure 2. In the configuration shown in Figure 2, the ADG1604 multiplexer, VC1 of the HMC8074, and the output buffer amplifier (VCB) are all enabled. When a jumper is disconnected, the corresponding signal is pulled up to the supply voltage (V_{CC}). To reset a pin, connect the shorting jumper from the pin to the adjacent ground (GND). Figure 2 is annotated in green to indicate where a jumper is connected and shorted to ground.
5. Connect the low noise, variable power supply to the SMA connector on the tuning port (J2) using a double shielded BNC cable and a BNC to SMA adapter. Torque this connection to 8 in/lb using an SMA torque wrench.
6. Connect a 50 Ω RF cable capable of mating to the 2.92 mm K connector at J3 and torque this connection to 8 in/lb. Connect the other end of the RF cable to a signal source analyzer.
7. Enable the 6.0 V power supply. Approximately 103 mA is drawn from the supply if the EV1HMC8074LP6G has been configured properly in the previous steps.
8. Enable the variable power supply and adjust the tuning voltage to within the range of the VCO band being used.

Verify that the proper output frequency is observed on the signal source analyzer. An example output frequency is shown in Figure 4 in the Evaluation and Test section.

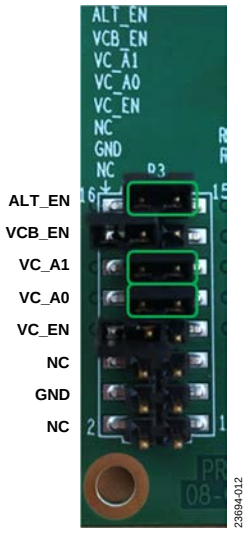

Figure 2. P3 Connector Initial Jumper Configuration with VC1 and VCB Enabled

EVALUATION BOARD HARDWARE

The EV1HMC8074LP6G schematic, silkscreen, and bill of materials are available in the Evaluation Board Schematic and Artwork section and the Ordering Information section. The Gerber fabrication files are available on the HMC8074 product page.

POWER SUPPLIES

The EV1HMC8074LP6G is powered by a 6.0 V dc (150 mA) power supply connected to the SMA connector, 6.0 V. This supply path includes a single ultralow noise, low dropout (LDO) regulator, the LT3042. As an extra safeguard, the LT3042 is configured to use the current-limit feature. A resistor (R6) sets the current limit on Pin 5 (ILIM) of the LT3042 to 102.5 mA (R6 = 1240 Ω) on the EV1HMC8074LP6G.

A second low noise power supply cable providing up to 13.0 V is required to tune the VCO cores. Using a noisy power supply on the tuning port results in narrow-band frequency modulation and sidebands.

Users that intend to use an external power supply, Linduino® microcontroller, or Arduino Uno microcontroller to directly program the logic from the P3 header must remove the five 10 kΩ resistors (R9, R10, R11, R12, and R13) or damage may occur. Refer to the Evaluation Board Software section for more information.

VCO

The HMC8074 includes four VCO cores that generate a range of fundamental frequencies. The frequency range of each core overlaps with the adjacent core to allow continuous frequency coverage, including any supply and temperature variation.

By generating fundamental frequencies, the need for additional filtering can be reduced or eliminated because there are no subharmonics. The tuning sensitivity across the frequency band is similar for each core, which simplifies the loop filter design. The consistent tuning sensitivity from core to core simplifies any frequency planning or dynamic loop bandwidth adjustment required to manage spurs or settling time. The integrated common tuning port (VTUNE) and RF output ports (RF1) simplify the layout. Each frequency band has an allowable tune voltage of 1.0 V dc to 13.0 V dc.

The VCO cores can be selected one at a time at any point by the application, depending on the frequency range required. To select a certain VCO core, enable the supply voltage at its respective bias pin (VC1 through VC4). The EV1HMC8074LP6G uses the ADG1604 4:1 multiplexer to select a VCO core. VCO cores can be enabled or disabled in any sequence desired. Refer to the ADG1604 truth table in the ADG1604 data sheet for more information.

The EV1HMC8074LP6G includes additional filtering to prevent supply voltage overshoot and undershoot that can damage the device if the supply voltage exceeds 5.5 V. This filtering provides 5 V of biasing that settles to within approximately 1 µs.

BUFFER AMPLIFIER

The buffer amplifier used in the HMC8074 is a broadband cascode design that draws approximately 12 mA and is shared by all four VCO cores. Pin 8 (VCB) of the HMC8074 provides the bias voltage for the upper half of the cascode amplifier stage, and the VCO outputs provide the biasing for the lower half of the cascode amplifier stage. When any one of the four VCO cores is enabled, the cascode amplifier fully enables and provides an output signal at Pin 5 (RF1). The buffer amplifier is designed to handle the power supplied by only one VCO core at a time. To prevent long-term damage that occurs if more than one VCO core is powered up simultaneously, the EV1HMC8074LP6G incorporates the ADG1604 4:1 multiplexer. As configured on the EV1HMC8074LP6G, the ADG1604 multiplexer incorporates exclusive OR (XOR) logic along with the ability to break contact with one VCO core for a minimum of 30 ns before closing the contacts on the next switch to power up a different VCO core. To minimize the switching time of the ADG1604, a 5 V logic was used. However, a 3 V logic can also be used by using an external power supply or microcontroller, such as a Linduino or Arduino Uno.

Refer to the ADG1604 truth table in the ADG1604 data sheet for more information regarding the ADG1604 logic and for use with other logic levels.

Users can leave the VCO enabled and power down Pin 8 (VCB) to mute the output signal, which leaves the lower stage of the cascode amplifier enabled. However, because the upper circuitry is disabled, the RF does not route to the output. Refer to the HMC8074 data sheet for additional details.

Figure 5 shows the HMC8074 with VC1 enabled and the output buffer muted (VCB_EN = 0).

For additional details on the buffer amplifier circuitry, consult the HMC8074 data sheet.

RF OUTPUT

The EV1HMC8074LP6G has two 50 Ω RF output ports, Pin 5 (RF1) and Pin 3 (RF2), which are supplied by a buffer amplifier that is common to all four VCO cores.

RF1 (J3) is a single-ended RF output that operates up to 26.6 GHz. The actual frequency range and power level at any given time depends on which VCO core is enabled.

RF2 (J4) is a single-ended, low power RF output that also operates up to 26.6 GHz. The output power at RF2 is approximately 10 dBm less than RF1. The RF2 output can be used to feed the VCO output back to the phase-locked loop (PLL) input when used in a synthesizer application.

Consult the HMC8074 data sheet for additional information relative to the specific model being evaluated.

LOOP FILTER

Although the EV1HMC8074LP6G does not incorporate the entire loop filter, the evaluation board provides the means to filter noise that can appear on the tuning port when evaluating only the VCO cores.

By default, a 100 pF capacitor (C12) is placed near Pin 27 (VTUNE) of the HMC8074 to filter high frequency noise that can couple onto the tune port path when evaluating the VCO cores.

The EV1HMC8074LP6G also includes placements for the last pole of a loop filter on the tuning port path when configuring the HMC8074 with an Analog Devices, Inc., standalone PLL product, like the ADF41513. Although, the tuning port path and input capacitance of the VCO makes up the last pole of the loop filter, the last pole in this instance is referred to as what can be accessed by the user.

Refer to the HMC8074 data sheet for an example of a synthesizer application that incorporates the EV1HMC8074LP6G and the EV-ADF41513SD1Z.

The loop filter path length typically increases when using evaluation boards to build a synthesizer. Therefore, the placement of the loop filter components is critical. To improve loop stability and overall performance, place the first pole of the loop filter as close to the PLL charge pump output as possible. Place the last pole as close as possible to the tuning port, Pin 27 (VTUNE), of the VCO. The placement of any additional poles that exist between the first and last pole of the loop filter are not as critical. Therefore, these filter poles can remain on the PLL board (EV-ADF41513SD1Z). The placements for the last pole on the EV1HMC8074LP6G are populated by default and consist of R32 (0 Ω by default) and a 100 pF capacitor (C12) near Pin 27 (VTUNE). Users can replace the 0402 surface-mount components with the proper values as needed.

The tuning voltage requirements of the HMC8074 (1 V to 13.0 V) require an active loop filter, unless the charge pump of the PLL selected by the user can output at least 14 V. PLL evaluation boards typically include placements for the operational amplifier, its biasing circuitry, and any component placements. Therefore, this circuitry is not included on the EV1HMC8074LP6G.

The SMA connector (J2) provides the means to connect the PLL charge pump output to the tuning port (VTUNE) when the EV1HMC8074LP6G is used with an optional PLL evaluation board. J2 can also manually tune the VCO within its band when evaluating the open-loop VCO performance. Keep the tuning voltage below the absolute maximum ratings for the tuning port (15 V) or damage occurs. For the absolute maximum ratings, refer to HMC8074 data sheet.

DEFAULT CONFIGURATION

All components necessary for local oscillator generation are inserted on the EV1HMC8074LP6G.

EVALUATION BOARD SOFTWARE

Currently, there is no software available for the EV1HMC8074LP6G because this evaluation board does not need software to evaluate the HMC8074. However, the EV1HMC8074LP6G layouts have been configured in a manner that allow the use of a Linduino, Arduino Uno, SDP-K1 controller board, or similar microcontroller board, which may be beneficial for customers needing to develop and test switching algorithms for their applications.

To connect the SDP-K1 board to the EV1HMC8074LP6G, flip the SDP-K1 board over so that the digital input and output pins (Pin 8 to Pin 14) line up with Pin 3 to Pin 15 of Connector P3, respectively, as shown in Figure 3.

Figure 3. SDP-K1 Board Mounted to the EV1HMC8074LP6G

EVALUATION AND TEST

To configure the EV1HMC8074LP6G for the first time, follow Step 1 through Step 6 in the Evaluation Board Setup Procedure section. To evaluate and test the performance of the EV1HMC8074LP6G, perform the following steps:

1. Enable the variable power supply and adjust the tuning voltage to 8.45 V. If the EV1HMC8074LP6G is configured properly, a signal at approximately 9.2 GHz with approximately 0 dBm to 2 dBm of output power appears on a spectrum analyzer or signal source analyzer. Refer to Figure 4.
2. Remove the bias for the buffer amplifier (VCB). This removal decreases the output power by approximately 28 dBm. Refer to Figure 5.
3. Use the signal source analyzer to measure the phase noise. Refer to Figure 6.
4. Disable the 6.0 V power supply, disconnect the 50 Ω RF cable from RF1, and connect the RF cable to RF2.
5. Repeat Step 2 through Step 4 to measure the RF2 spectrum and open-loop phase noise. Figure 7, Figure 8, and Figure 9 show the typical expected results of the RF2 spectrum and open-loop phase noise. The RF2 output power is approximately 10 dB less than the output power measured at RF1.

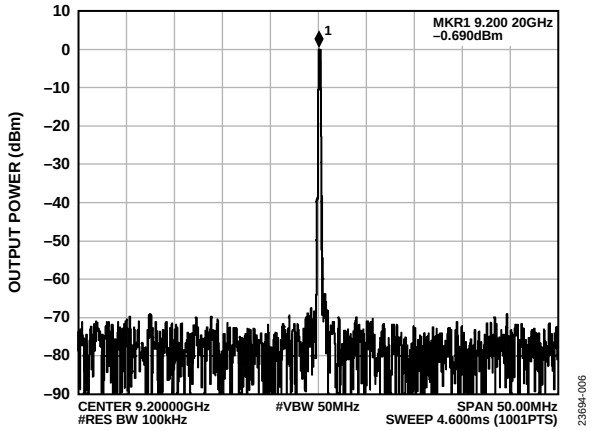

Figure 4. EV1HMC8074LP6G RF1 Output at VCO Band 1, VTUNE = 8.45 V, 9.2 GHz, Includes Insertion Loss of the RF Cable

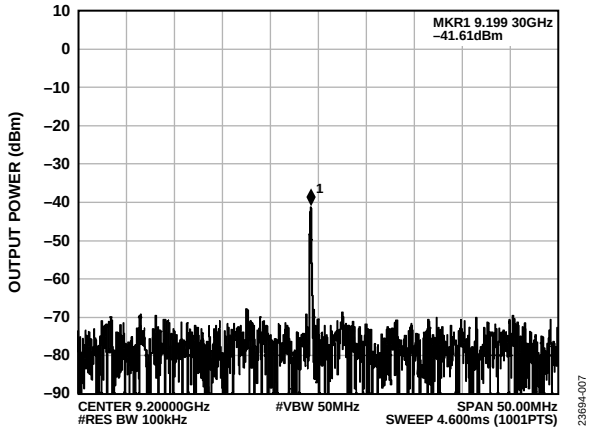

Figure 5. EV1HMC8074LP6G RF1 Output at VCO Band 1, VTUNE = 8.45 V, 9.2 GHz, Buffer Amplifier Disabled (RF1 Output Muted)

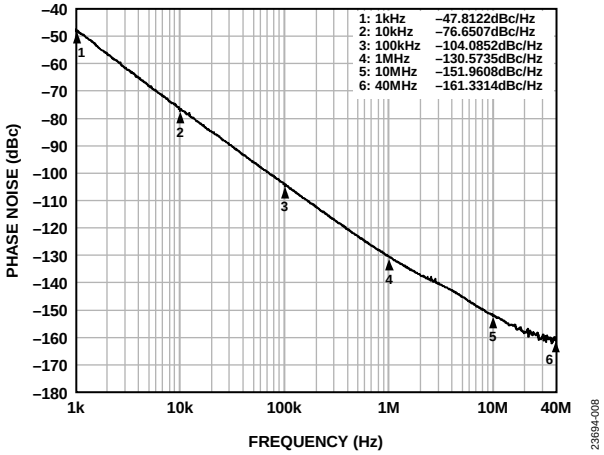

Figure 6. EV1HMC8074LP6G Open-Loop Phase Noise at RF1, VCO Band 1, VTUNE = 8.45 V, 9.2 GHz

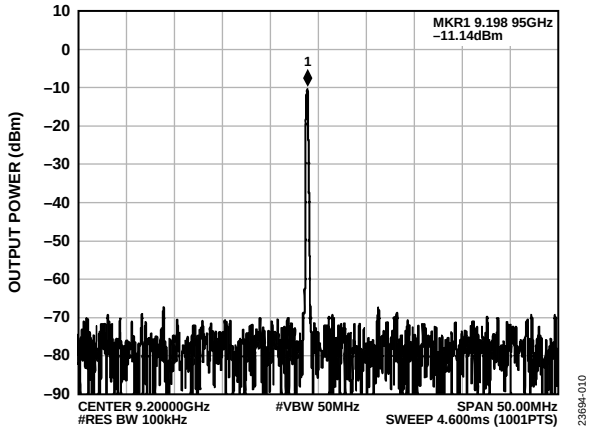

Figure 7. EV1HMC8074LP6G RF2 Output at VCO Band 1, VTUNE = 8.45 V, 9.2 GHz, Buffer Amplifier Enabled, VCB = 1, Includes Insertion Loss of the RF Cable

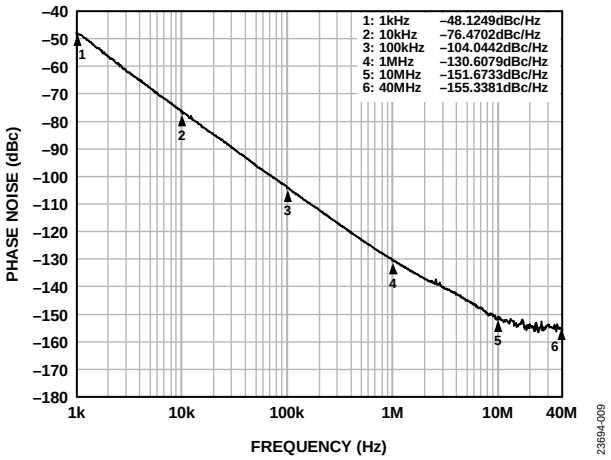

Figure 8. EV1HMC8074LP6G Open-Loop Phase Noise at RF2, VCO Band 1, VTUNE = 8.45 V, 9.2 GHz, Buffer Amplifier Enabled, VCB = 1

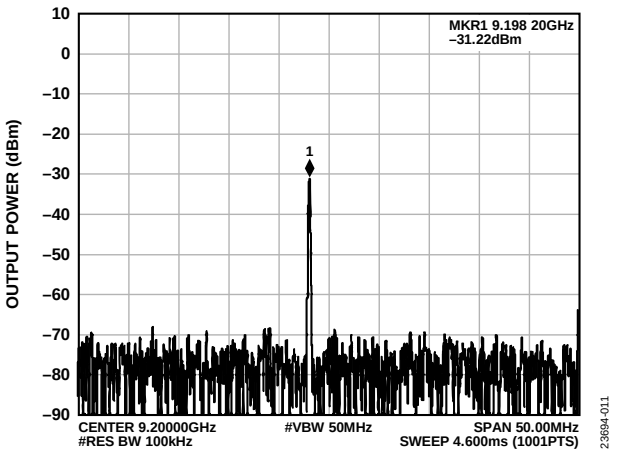

Figure 9. EV1HMC8074LP6G RF2 Output at VCO Band 1, VTUNE = 8.45 V, 9.2 GHz, Buffer Amplifier Disabled, VCB = 1, Includes Insertion Loss of the RF Cable

EVALUATION BOARD SCHEMATIC AND ARTWORK

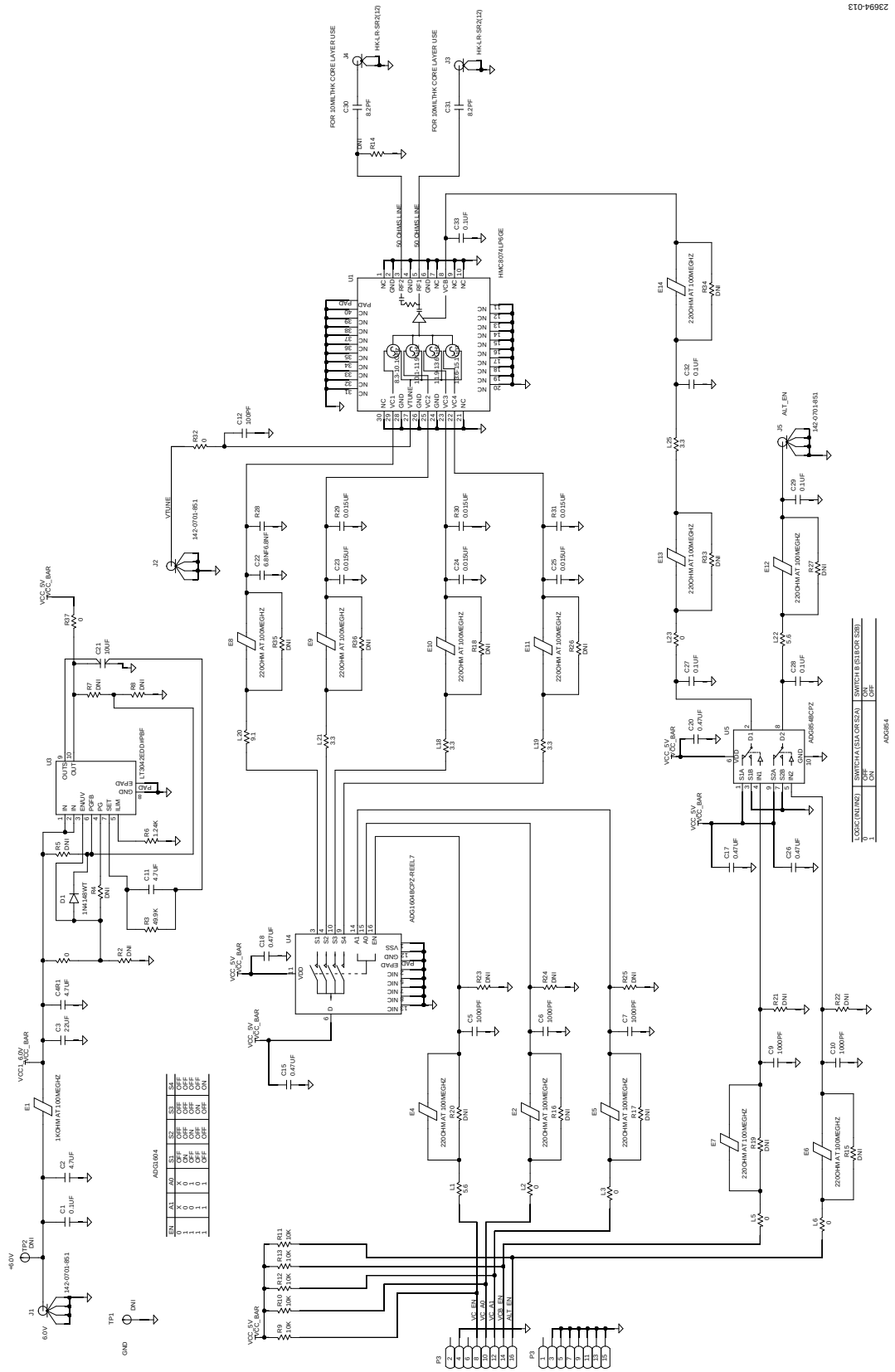

Figure 10. EV1HMC8074LP6G Schematic

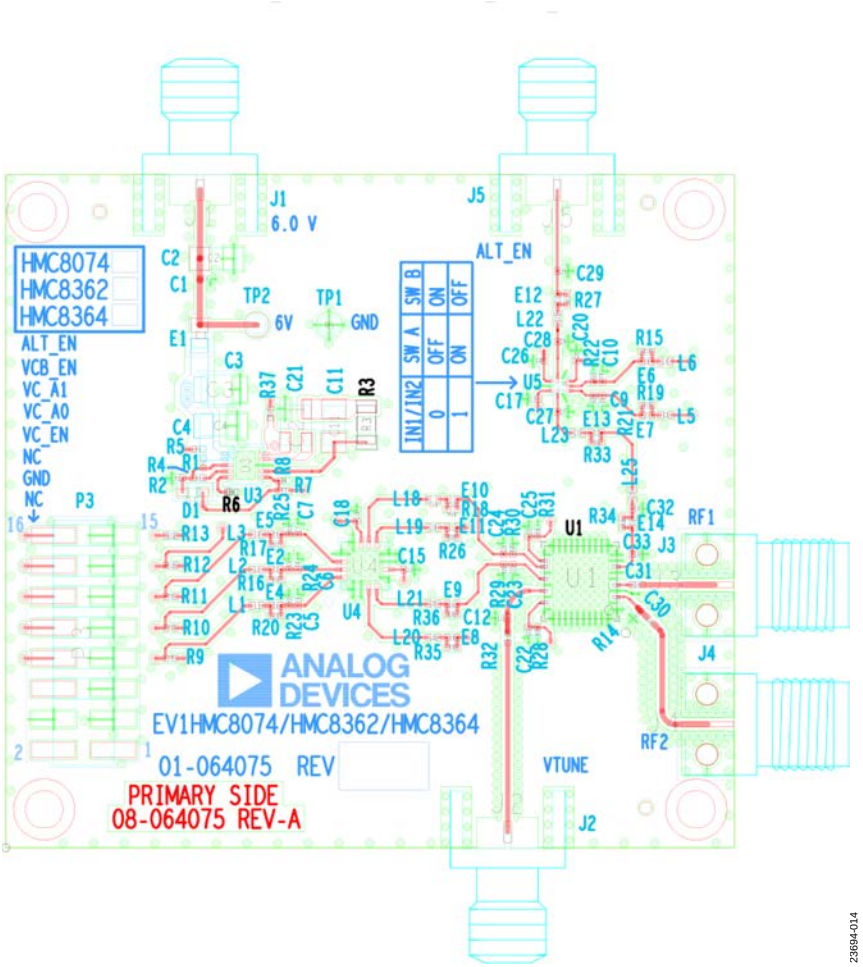

Figure 11. EV1HMC8074LP6G Silk Screen and Metal 1, Top Side

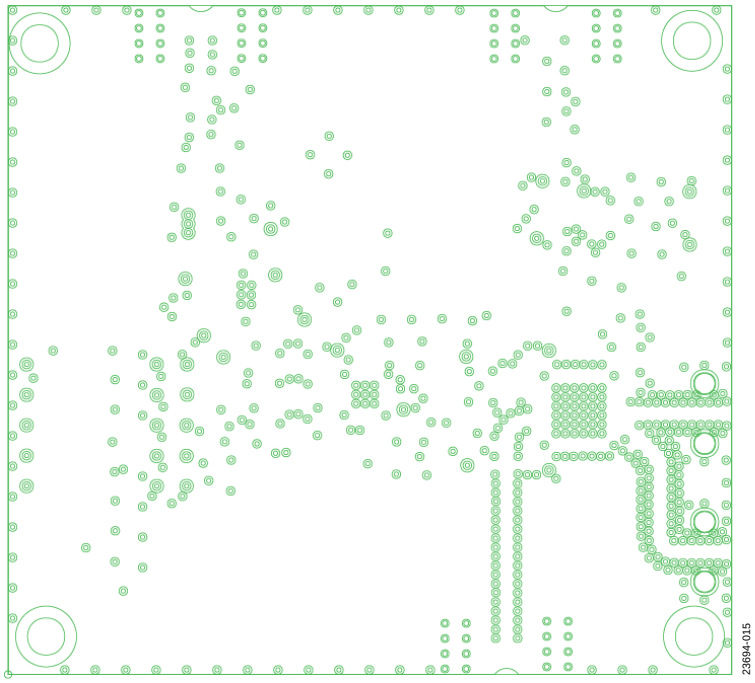

Figure 12. EV1HMC8074LP6G Metal 2, Ground

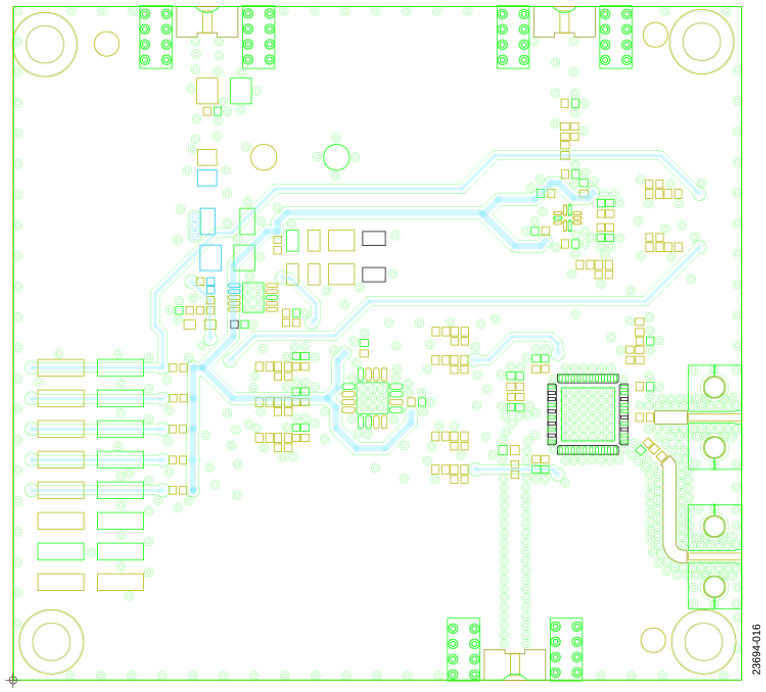

Figure 13. EV1HMC8074LP6G Metal 3, RF and DC

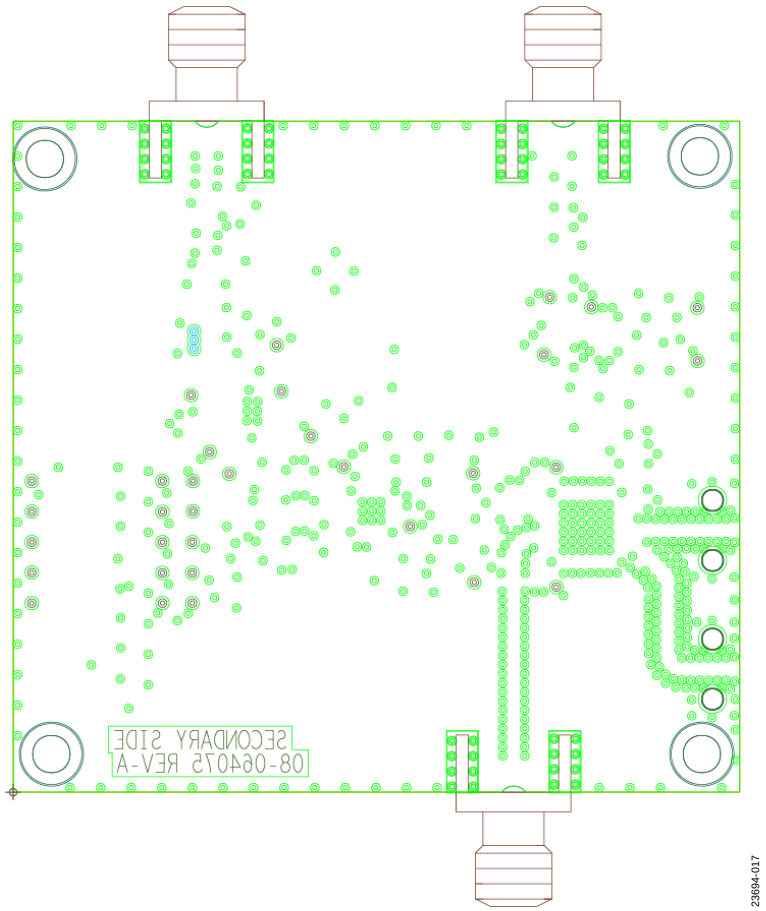

Figure 14. EV1HMC8074LP6G Metal 4, Backside

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Location	Description	Value	Manufacturer	Part Number
C1, C27, C28, C29, C32, C33	Capacitors, ceramic, X7R, automotive grade	0.1 µF	Murata	GCM155R71C104KA55D
C5, C6, C7, C10	Capacitors, ceramic, general-purpose	1000 pF	Murata	GRM1555C1H102JA01
C2, C4, C11	Capacitors, ceramic, X7R	4.7 µF	Kemet	C1206C475K3RACTU
C12	Capacitor, multilayer, ceramic, high temperature	100 pF	TDK	C1005NP01H101J050BA
C15, C17, C18, C20, C26	Capacitors, ceramic, 10 V, 10%, X7S, 0402, automotive grade	0.47 µF	Murata	GCM155C71A474KE36D
C21	Capacitor, ceramic, X7R, 4-pin footprint	10 µF	Murata	GRM32ER71H106KA12L
C23, C24, C25, R29, R30, R31	Capacitors, ceramic, 50 V, 5%, X7R, 0402, automotive grade	0.015 µF	Murata	GCM155R71H153JA55D
C22, R28	Capacitors, ceramic, general-purpose, X7R, 0402	6.8 nF	Samsung	CL05B682KB5NNNC
C3	Capacitor, ceramic, 25 V, 10%, X7R	22 µF	Samsung	CL32B226KAJNNNE
C30, C31	Capacitors, ceramic, 200 V, C0G, 0402	8.2 pF	American Technical Ceramics	600L8R2BT200T
C9	Capacitor, ceramic, 50 V, 10%, X7R, 0402, AEC-Q200	2200 pF	Murata	GCM155R71H222KA37D
D1	Diode fast switching	Not applicable	Diodes, Inc.	1N4148WT
E1	Inductor chip ferrite bead, multilayer, 0.5 A, 0.280 Ω maximum dc resistance	1 kΩ at 100 MHz	Murata	BLM21AG102SN1D
E2, E4 to E14	Inductor chip ferrite bead, 0.7 Ω, 0.3 A	220 Ω at 100 MHz	Murata	BLM15GG221SN1D
J1, J2, J5	SMA, 50 Ω, end launch jack	Not applicable	Cinch	142-0701-851
J3, J4	2.92 mm coaxial for frequency test measurements, 50 Ω, 40 GHz	Not applicable	Hirose Electric Co.	HK-LR-SR2(12)
L20	Resistor, surface-mount device (SMD), 0402	9.1 Ω	Panasonic	ERJ-2GEJ9R1X
L18, L19, L21, L25	SMD, 1%, 1/16 W, 0402	3.3 Ω	Yageo	RC0402FR-073R3L
L2, L3, L5, L6, L23, R1, R32, R37, R14	Resistors, surface-mount jumper	0 Ω	Panasonic	ERJ-2GE0R00X
L1, L22	Resistors, thick film chip	5.6 Ω	Panasonic	ERJ-2GEJ5R6X
P3	16 position male header double row	Not applicable	Samtec Inc.	TSM-108-01-L-DV
R9 to R13	Resistors, precision thick film chip	10 kΩ	Panasonic	ERJ-2RKF1002X
R3	Resistor, SMD, 1%, 1/4 W, AEC-Q200	49.9 kΩ	Panasonic	ERJ-8ENF4992V
R6	Resistor, SMD, 1%, 1/16 W, 0402	1.24 kΩ	Panasonic	ERJ-2RKF1241X
U1	Quad band, MMIC, VCO, 8.3 GHz to 15.2 GHz	Not applicable	Analog Devices	HMC8074LP6GE
U3	20 V, 200 mA, ultralow noise, ultrahigh power supply rejection ratio (PSRR), RF linear regulator	Not applicable	Analog Devices	LT3042EDD#PBF
U4	3.3 V, 4:1 multiplexer	Not applicable	Analog Devices	ADG1604BCPZ-REEL7
U5	CMOS, SPDT multiplexer	Not applicable	Analog Devices	ADG854BCPZ-REEL7

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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