GMSL2 Hardware Design Guide
Rev 0; 6/23

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1. Purpose and Scope

The GMSL2 Hardware Design and Validation Guide presents industry standard best practices for designing a high-speed system using GMSL2 products. This guide provides various techniques to optimize high-speed hardware design and guidance for hardware validation. Special consideration is given to schematic design and PCB layout to ensure optimized GMSL2 link performance.

The GMSL2 Hardware Design and Validation Guide is not a data sheet. This document describes important system design considerations and should be used as a reference for system development and component evaluation. Specifications for GMSL2 products are only guaranteed by their respective data sheets. Contents of this document are subject to change at any time and without notice. Users are responsible for the evaluation and validation of their systems utilizing GMSL2 devices.

2. GMSL2 Overview

The GMSL2 devices use Analog Devices, Inc.'s proprietary second-generation Gigabit Multimedia Serial Link (GMSL2) technology to transport high-speed serialized data over coax or shielded twisted pair (STP) cable for automotive camera and display applications. The GMSL2 links operate at fixed data rates: 3Gbps or 6Gbps on the forward channel and 187Mbps or 1.5Gbps on the reverse channel (depending on device capabilities and configuration). A block diagram of a typical GMSL2 system is shown in Figure 2.1.A.

*Note: The forward channel is defined as serializer-to-deserializer transmission; the reverse channel is defined as deserializer-to-serializer transmission.

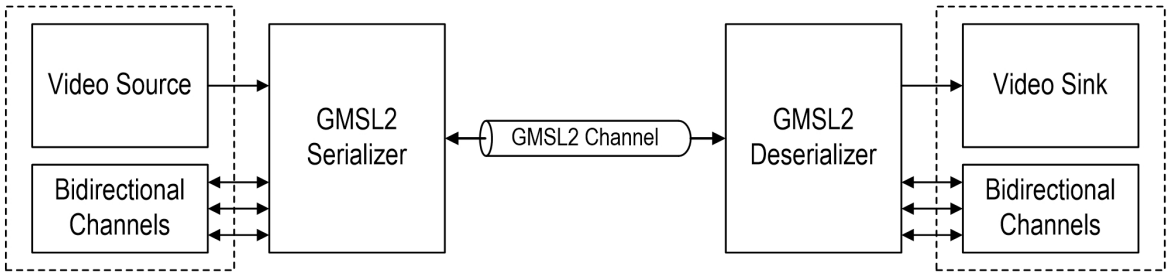


Figure 2.1.A. GMSL2 System Block Diagram

3. Hardware Recommendations and Best Practices

This section provides schematic and layout guidance for designing PCBs with GMSL2 serializers or deserializers.

3.1 Schematic Entry

This section provides schematic design entry guidance.

3.1.1 Schematic Checklist

- All power pins have the recommended decoupling capacitors with correct voltage tolerance.
- Single-ended links have proper termination on (-) pin.
- Correct series AC coupling capacitor is selected for GMSL2.
- Pull-up resistors on I^2C/UART lines are used and appropriately sized.
- General-purpose output (GPO) pins with open-drain drives have pull-up resistors.
- Crystal or oscillator is properly connected.
- XRES resistor is 402Ω with 1% tolerance.
- Correct CFG pin resistor-divider values are used for desired power-up mode.
- Input/output video interface is correctly connected.
- Check application requirement for Automotive Electronics Council AEC-Q level.
- Use a recommended power over coax (PoC) circuit or verify new PoC circuit. See the *Power over Coax* section for additional details.
- PoC minimum and maximum voltage should meet all system requirements.

3.1.2 AC Coupling and Termination

Any active PHY needs to have both outputs terminated and/or matched to 50Ωs (and AC coupled). This is because the output is differential, and if one side is terminated and the other is not, there is a common mode shift that can potentially cause electromagnetic interference (EMI) issues and link performance degradation. Detailed termination recommendations are shown below.

For the serializer, in order to minimize the reflection effect, it is recommended to have AC capacitor as close as possible to the pin, usually less than half of a bit rate distance from the transmitter. Note that ½ UI for 6Gbps signal is approximately a half inch / 500 mil, which is the maximum distance from the IC Analog Devices recommend the AC capacitor placement.

Coax Application

- In coax application, positive (+) side should be used as the default path.
- Use appropriately sized AC capacitors (Table 1).
- Negative (-) side should be terminated with 100nF capacitor and 50Ω to ground.
- It is recommended to use a 0402 Capacitor. Larger capacitors can cause impedance mismatches that degrades performance.
- Select an AC capacitor rated above the PoC-desired voltage to ensure the applied voltage and capacitor tolerance do not affect link integrity.

STP Application

- In Shielded Twisted Pair (STP) application both positive (+) and negative (-) pins should be used.
- The 100nF AC coupling capacitors should be used on both traces.
- See Table 1 for other configurations.

Table 1. AC Coupling Capacitor Sizing for Various Link Modes

Configuration	PoC	AC Coupling Capacitor
GMSL2	X	100nF

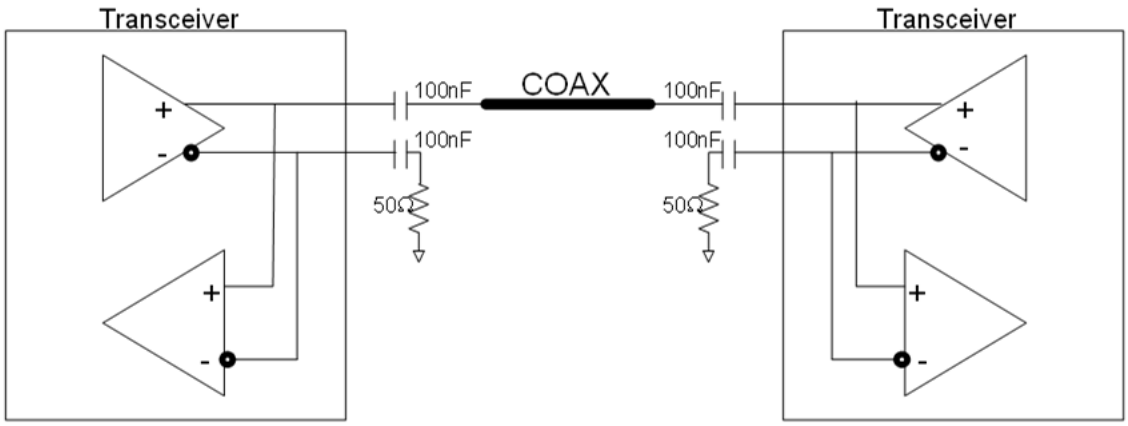


Figure 3.1.A. Coax Termination

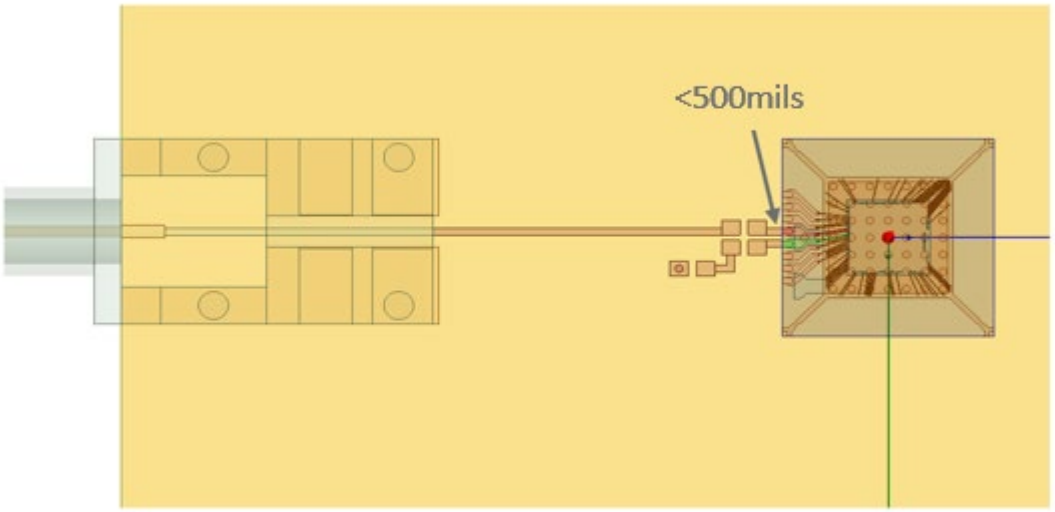


Figure 3.1.B. Coax Layout Example: Edge Connector, 1-inch Trace, Capacitor and TQFN Package

*Note: Place AC capacitors as close to pins as possible (see Figure 3.1.B).

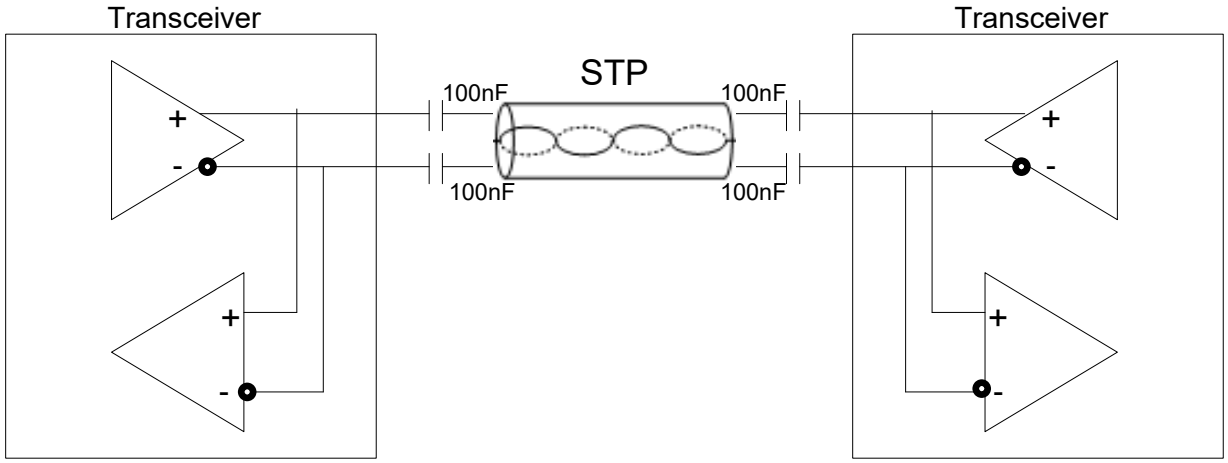


Figure 3.1.C. STP Termination

Unused PHY Termination

If a PHY, SIOA, or SIOB is not being used, it can be left floating only if the PHY is turned off through register configuration. This is done through register CTRL0, bitfield LINK_CFG[1:0]. With this proper register configuration, both +/- pins of the unused PHY can be left floating, thus reducing BOM costs.

If an unused PHY is not configured off through the CTRL0 register, both +/- pins should be terminated through a capacitor and resistor to GND.

3.2 PCB Layout Recommendations

This section provides PCB layout design guidance.

3.2.1 Key PCB Requirements

- Minimize trace length. Traces should be less than 2 inches (5cm) or less than 1.2dB Insertion Loss.
- Minimize impedance discontinuities and the number of components on high-speed traces.
- Use GND cutouts where necessary.
- Simulate and measure PCB performance to ensure a robust link.
- Maintain characteristic impedance.

3.2.2 Proper Layout Techniques

Proper high-speed PCB layout is required to meet the GMSL2 PCB channel specification to ensure robust GMSL2 link operation. The layout of the serial link traces must be carefully designed to provide optimal signal integrity by minimizing impedance discontinuities and noise coupling. The layout of the serial link trace must follow high-speed layout practices, which are as follows:

- Route the serial link trace as a microstrip on the top layer or as a stripline in a middle layer (if EMI/EMC is a concern).
- Use 100Ω differential or 50Ω single-ended trace routing with impedance control of ±5%.
- Minimize impedance discontinuities by using proven design and simulation practices.
- Place IC as close as possible to the connectors to minimize trace length. Traces should be less than 2 inches (5cm) to meet the GMSL2 PCB channel specification.
- Minimize vias. If vias are required, eliminate via stubs by using back drilled vias and add ground transition vias next to signal vias.
- Place AC coupling capacitors on the top layer as close to the IC as possible (within 500mils ensures it is less than 0.5UI from the transmitter). Route signal differentially to the AC coupling capacitors, even in Coax mode. Ensure 100Ω impedance and length matching to the AC capacitors.
- In Coax mode, terminate the SION trace with an AC coupling capacitor and 50Ω resistor to ground.
- In STP mode, ensure length matching and consistent coupling distance between traces.
- Eliminate stubs by placing component pads directly on the high-speed trace, including line fault, PoC, and ESD components.
- Use cutouts in the reference layer under the pads of components on the high-speed trace. The size of these cutouts depends on the specific PCB stackup. For example, the cutouts are 1.35x the pad size in the EV kits.
- Follow connector vendor layout footprint recommendations.
- For through-hole connectors, use topside mounting of IC and bottom-side mounting of connector to minimize connector pin stubs to improve return loss.
- Avoid 90-degree bends on high-speed lines.
- Maintain a continuous reference plane under high-speed trace. There should be no split ground or power planes under the serial link trace (except ground cutouts).
- The ESD protection should be placed near the RF connector if required for application (and PoC is not used).
- Use an array of ground vias in the exposed ground pad (EP) for thermal management.
- High-speed video interfaces (e.g., CSI C-PHY, CSI D-PHY) and other high-speed interfaces (e.g., SPI) all have their own layout requirements and impedance specifications, length matching tolerances, and maximum trace lengths. Follow the guidance given in each specification.
- Maintain pair-to-pair and signal-to-signal distances for high-speed signals to reduce crosstalk.
- Differential pair-to-pair distance should be at least 2xSeparation away.
- Single-ended signals should be at least 3xTrace width away or isolate on a different layer.

3.2.3 Layout Examples

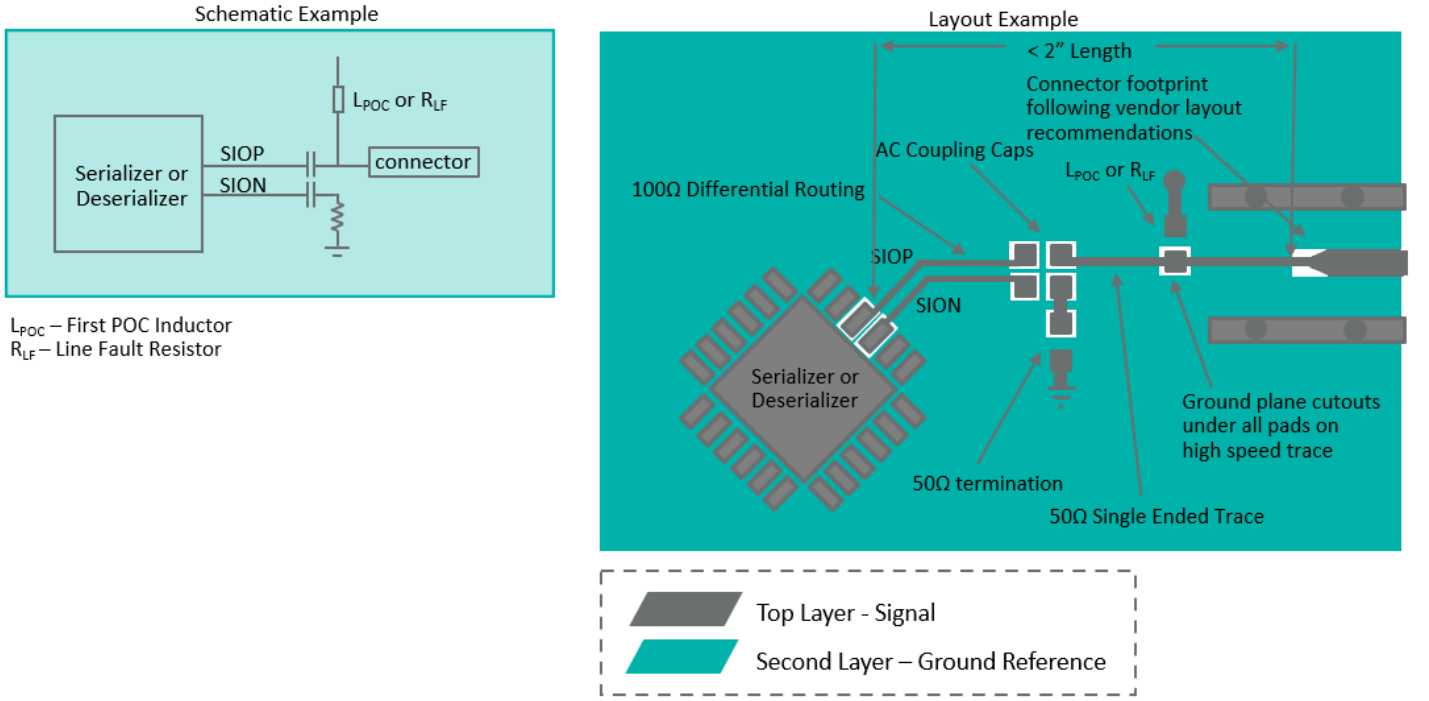


Figure 3.2.A. Schematic and Layout Example for Single-Ended (Coax) Operation

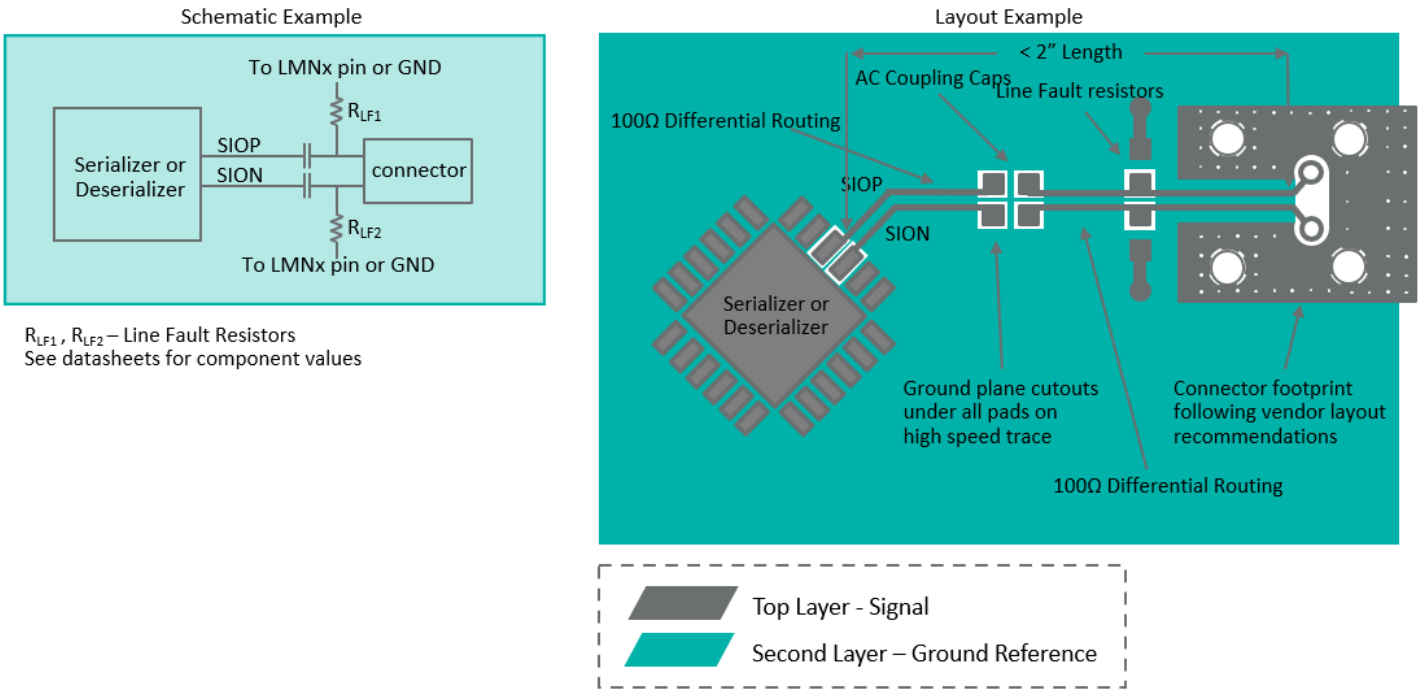


Figure 3.2.B. Schematic and Layout Example for STP Operation

3.2.4 Skew Management

Skew management is a critical part of high-speed signal PCB layout. Propagation delay between differential pairs can significantly degrade the signal integrity and increase common mode noise and EMI. Delay skews between clock and data signals need to be carefully controlled for optimal signal integrity. Differential twisted pair GMSL2 links are recommended to have less than +/- 5mils of skew. Note that for different cables and connectors there may be intra-pair skews already introduced in the cable and connector, which needs to be taken into consideration when calculating the overall channel skew. (Check the vendors for detail for specific connectors. An example of this can be seen in the HSD footprint recommendation in the connector section.) For video interfaces, such as CSI, it is strongly recommended to limit length differences to +/- 5mils for inter-pairs (between separate differential pairs) and intra-pairs (within a single differential pair).

3.2.4.1 Differential EMI Improvements

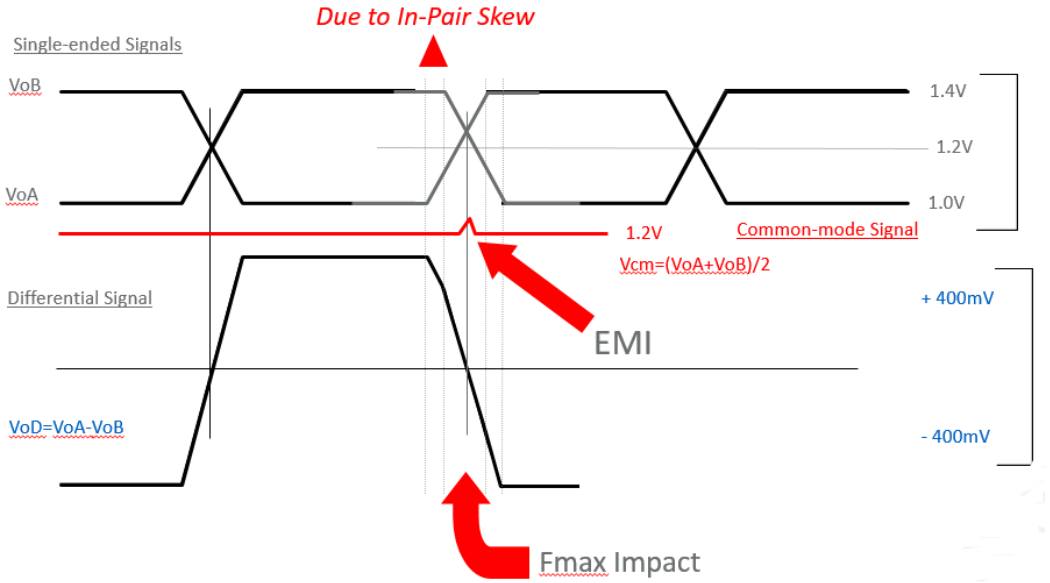


Figure 3.2.C. Maintaining Differential Signal Integrity

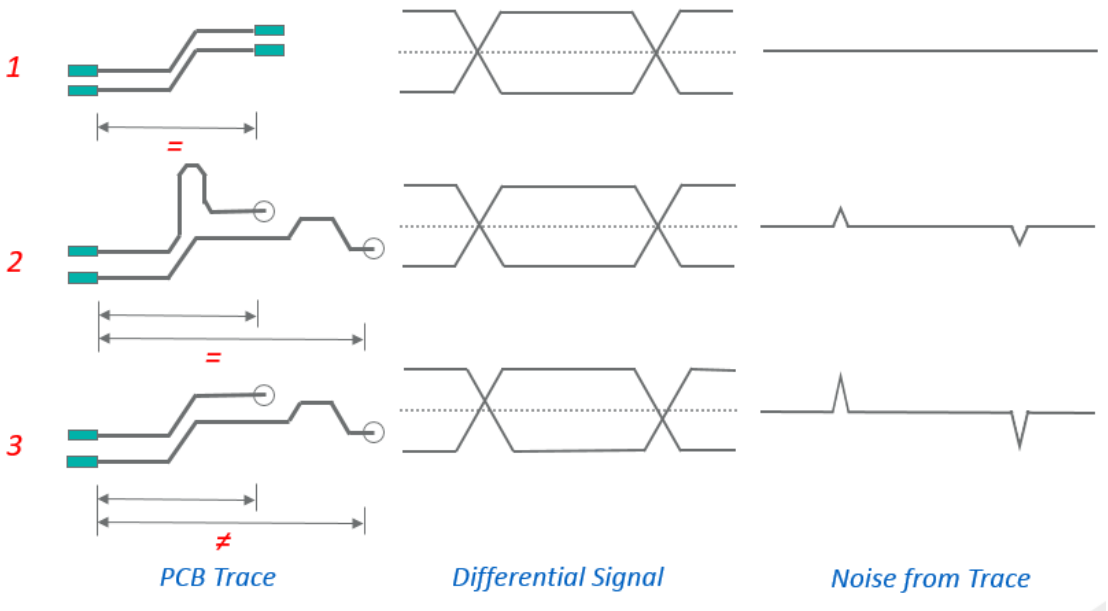


Figure 3.2.D. Connector Skew Effects on Differential Signals

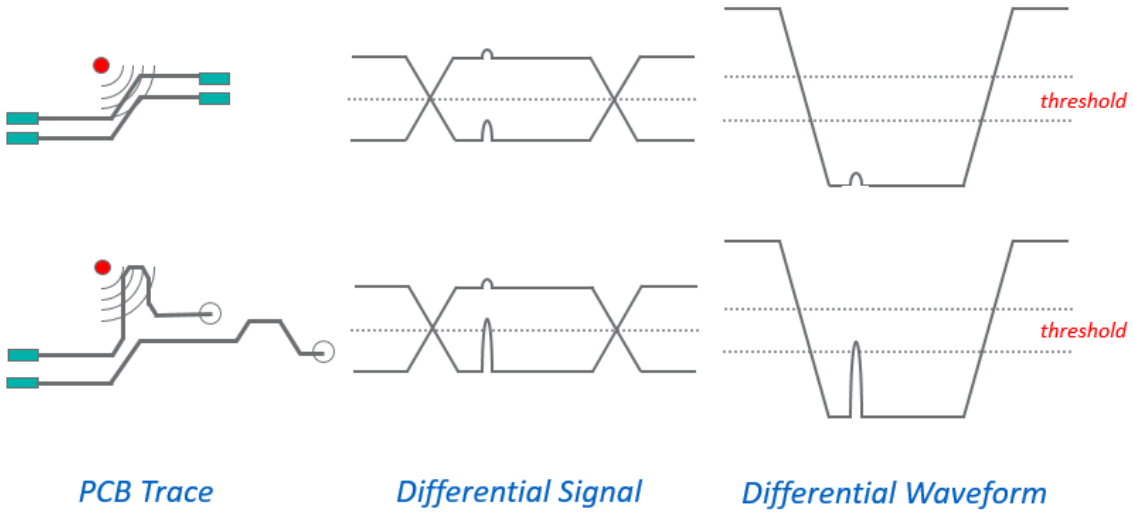


Figure 3.2.E. Differential Signal Coupling and EMI

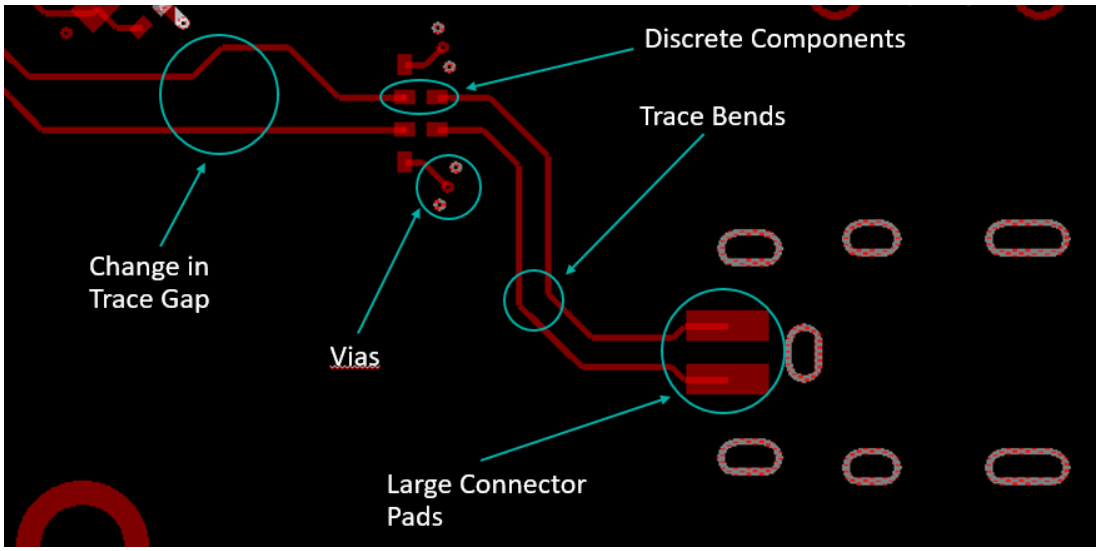


Figure 3.2.F. Location of Impedance Mismatch

3.2.4.2 Tightly Coupled Differential Pair

A tightly coupled differential pair provides better EMI performance.

The characteristic impedance is highly dependent on gap width.

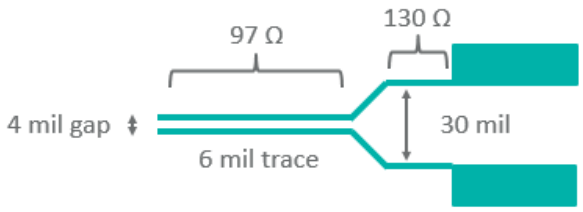


Figure 3.2.G. Tightly Coupled Differential Pair

3.2.4.3 Loosely Coupled Differential Pair

There is better S-parameter performance due to impedance not changing with trace spacing.

It is important for twisted pair connectors that have a wide footprint.

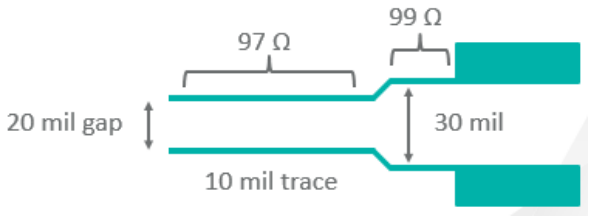


Figure 3.2.H. Loosely Coupled Differential Pair

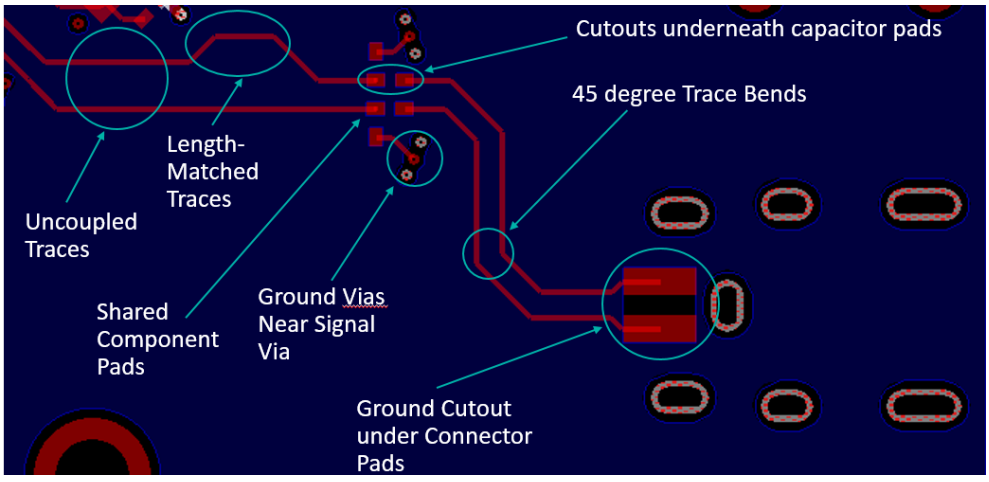


Figure 3.2.I. Optimized Layout

3.2.5 Layout Recommendations for Other Interfaces

Following are examples of good layout practices for MIPI (C-PHY/D-PHY).

3.2.5.1 MIPI PCB Layout Guidelines for GMSL2

3.2.5.1.1 Recommended PCB Routing for C-PHY

CSI-2 C-PHY data and clock lines should be routed with best high-speed practices. Unlike D-PHY, there should be little to no coupling between C-PHY lines. C-PHY traces should be impedance-controlled 50Ω single-ended length-matched traces corners. Additional information is available from the MIPI Alliance.

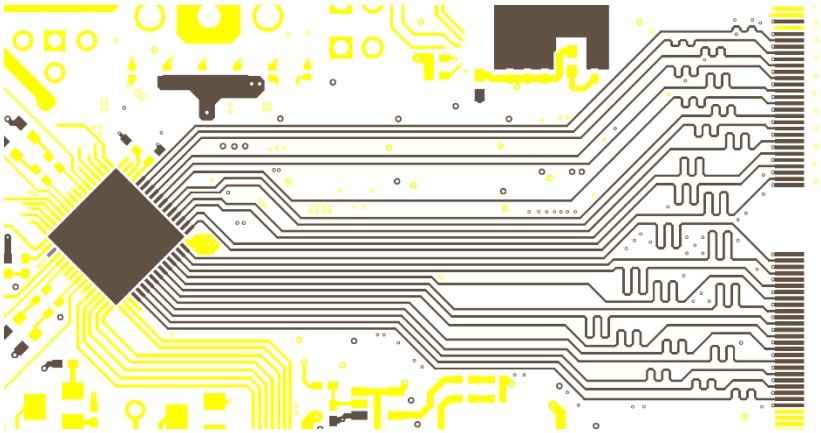


Figure 3.2.J. Example C-PHY Routing Taken from the Analog Devices Deserializer EV Kits

3.2.5.1.2 Recommended PCB Routing for D-PHY

CSI-2 D-PHY data and clock lines operate up to 1.25GHz (2.5Gbps) and should be routed with best practices. They should be impedance-controlled 100Ω differential length-matched traces that avoid any 90-degree corners. Additional information is available from the MIPI Alliance.

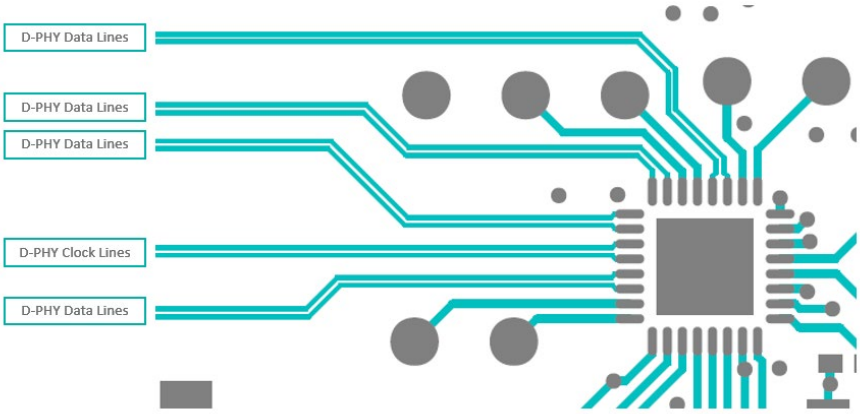


Figure 3.2.K. Example D-PHY Routing Taken from the Analog Devices Serializer EV Kits

3.2.6 Crystal Recommendations

Proper selection of load capacitors is critical to the proper operation of the crystal. A crystal's Equivalent Series Resistance (ESR) is an important consideration as it relates to crystal startup time. Crystals that have high ESR may not even start at all because of low margin between negative resistance (see Calculate Oscillator Negative Resistance section) and the ESR. Other considerations such as crystal drive level (power dissipation) are important as well. Operation of a crystal outside of the drive level can result in unpredictable change in frequency, ESR, and reliability.

3.2.6.1 Crystal Selection

When selecting an automotive grade 25MHz crystal, consider the following parameters.

3.2.6.2 Calculate Load Capacitance Needed

The crystal circuit is shown in the figure below. Note that R_{LIMIT} and $R_{FEEDBACK}$ are integrated into the IC and should not be added externally.

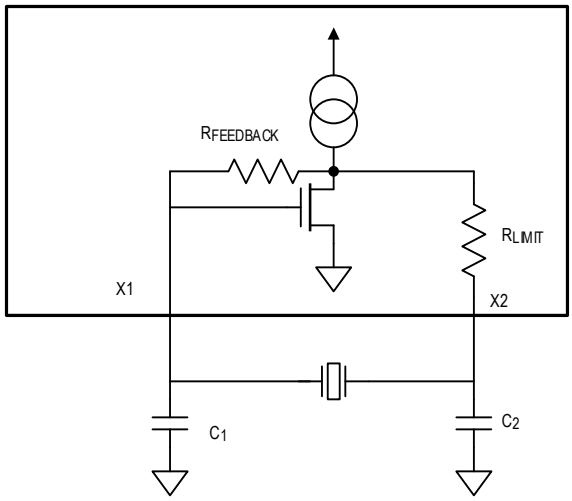


Figure 3.2.L. Recommended Crystal Schematic for GMSL2

The following example summarizes the process of selecting the required load capacitance for optimal frequency precision. First, confirm the required load capacitance (CL) from the crystal data sheet. Then, determine the external load capacitor values (CL1 and CL2) to achieve the proper total CL as specified in the crystal data sheet. This process is detailed as follows:

$$C_{X1\_total} = C_{IN\_X1} + C_{L1} + C_{X1\_trace}$$

$$C_{X2\_total} = C_{IN\_X2} + C_{L2} + C_{X2\_trace}$$

$$C_L = \frac{C_{X1\_total} \times C_{X2\_total}}{C_{X1\_total} + C_{X2\_total}}$$

where:

C_{IN_X1} = X1/OSC input capacitance from GMSL2 device data sheet

C_{X1_trace} = X1/OSC trace capacitance from layout

C_{L1} = X1/OSC external load capacitor

C_{IN_X2} = X2 input capacitance from GMSL2 device data sheet

C_{X2_trace} = X2 trace capacitance from layout

C_{L2} = X2 external load capacitor

C_L = total load capacitance specified in crystal data sheet

3.2.6.2.1 Example Load Capacitor Calculation

Assume the following:

C_L = 18pF (from crystal data sheet)

C_{IN_X1} = 3pF (from GMSL2 data sheet)

C_{X1_trace} = 2pF (estimated PCB capacitance)

C_{IN_X2} = 1pF (from GMSL2 data sheet)

C_{X2_trace} = 2pF (estimated PCB capacitance)

The external load capacitor value is approximately twice the specified load capacitance of 18pF. A commonly available capacitor value that is consistent with this requirement is 33pF. Assuming that CL1 = CL2 = 33pF, the total CL can be calculated to be around 18.5pF, which is in good agreement with the requirements.

Assume CL1 = CL2 = 33pF and calculate CL.

C_{X1_total} = 38pF

C_{X2_total} = 36pF

$C_L \approx$ 18.5pF

3.2.6.3 Calculate Oscillator Negative Resistance

Calculate the circuit's negative resistance. Generally to allow sufficient margin to component variation, it is desirable that negative resistance magnitude is greater than ~5x ESR.

Calculate the oscillator's negative resistance as follows:

$$R_{OSC}(\Omega) = -\frac{g_M \times C_1 \times C_2}{\omega^2 \times (C_1 \times C_2 + C_1 \times C_{SHUNT} + C_2 \times C_{SHUNT})^2 + (g_M \times C_{SHUNT})^2}$$

where:

$$C_1, C_2 = Total\ load\ capacitance\ at\ X1, X2\ in\ Farad\ (Calculated)$$

$$g_M = Crystal\ Oscillator\ Transconductance\ in\ A/V\ (GMSL\ Data\ sheet)$$

$$C_{SHUNT} = Crystal\ Shunt\ Capacitance\ in\ Farad\ (Crystal\ Data\ sheet)$$

$$\omega = angular\ frequency\ = 2\pi * 25{,}000{,}000Hz$$

3.2.6.3.1 Example Oscillator Negative Resistance Calculation

As an example, with $C_1, C_2 = 20pF, g_M = 28mA/V, C_{SHUNT} = 7pF$

$$R_{OSC}(\Omega) = -\frac{28E-3 \times 20E-12 \times 20E-12}{(2\pi * 25E6)^2 \times (20E-12 \times 20E-12 + 20E-12 \times 7E-12 + 20E-12 \times 7E-12)^2 + (28E-3 \times 7E-12)^2}$$

$$R_{OSC}(\Omega) = -225\Omega$$

Ensure that 5x ESR is less than $|R_{OSC}|$. Thus, ESR should be 45Ω or less.

3.2.6.4 Calculate Crystal Drive Level

Next, calculate the power dissipated in the crystal (crystal drive level) to check if it is within the limits of the crystal data sheet.

- Power dissipated by the crystal is: $P_{DRIVE} = \left(I_{DRIVE(RMS)}\right)^2 \times ESR$. This can be found by measuring the crystal current through a current probe.
- If a current measurement cannot be done, the crystal current can be calculated ≈ current through C1 (current through pin X1 is negligible).

  Current through C1 is: $I_{DRIVE(RMS)} = I_{C1(RMS)} = \left|\frac{V_{C1(RMS)}}{Z_{C1}}\right| = V_{C1(RMS)} \times 2\pi f \times C_1$
- Power dissipated by the crystal is now: $P_{DRIVE} = \left(V_{C1(RMS)} \times 2\pi f \times C_1\right)^2 \times ESR$

3.2.6.4.1 Example Crystal Drive Level Calculation

If V_{C1} is a sine wave, then $P_{DRIVE} = \frac{1}{2}\left(V_{C1(P-P)} \times 2\pi f \times C_1\right)^2 \times ESR$

For example, a measured 600mVpp sine wave at 25MHz and ESR = 40Ω and C1 = 20pF:

$$P_{DRIVE} = \frac{1}{2}(0.6 \times 2\pi \times 25E6 \times 20E - 12)^2 \times 40 = 71\mu W$$

3.2.6.5 Crystal Layout Recommendations

- Use load capacitors as recommended by the crystal manufacturer. Capacitance seen by the crystal is a summation of:
  - Load capacitor C_{load},
  - PCB trace capacitance, and
  - Input capacitance of the X1 and X2 pins as given in the relevant GMSL2 data sheet.
- Do not add an external feedback resistor or limit resistor, these are internal to GMSL2 devices. The value of the internal feedback resistor and limit resistor is given in the data sheet. *Some designs require an external feedback resistor. On GMSL2, the feedback resistor is built internal to the IC, so an external feedback resistor is not required.*
- Place crystal as close as possible to X1 and X2 to reduce parasitic capacitance. Length matching of X1 and X2 traces is not required. Trace width is not critical but affects capacitance. Fifty-ohm traces are not required.
- X1 and X2 traces should be shielded from aggressors such as GMSL2 lines and GPIO. Trace length should be minimal to prevent possibility of aggressor noise.
- If necessary, crystal can be on the board backside to minimize trace length.
- Ground pour can be used to improve shielding from aggressor noise if space permits.
- Crystal's case ground should be well connected to the ground plane with minimal trace.

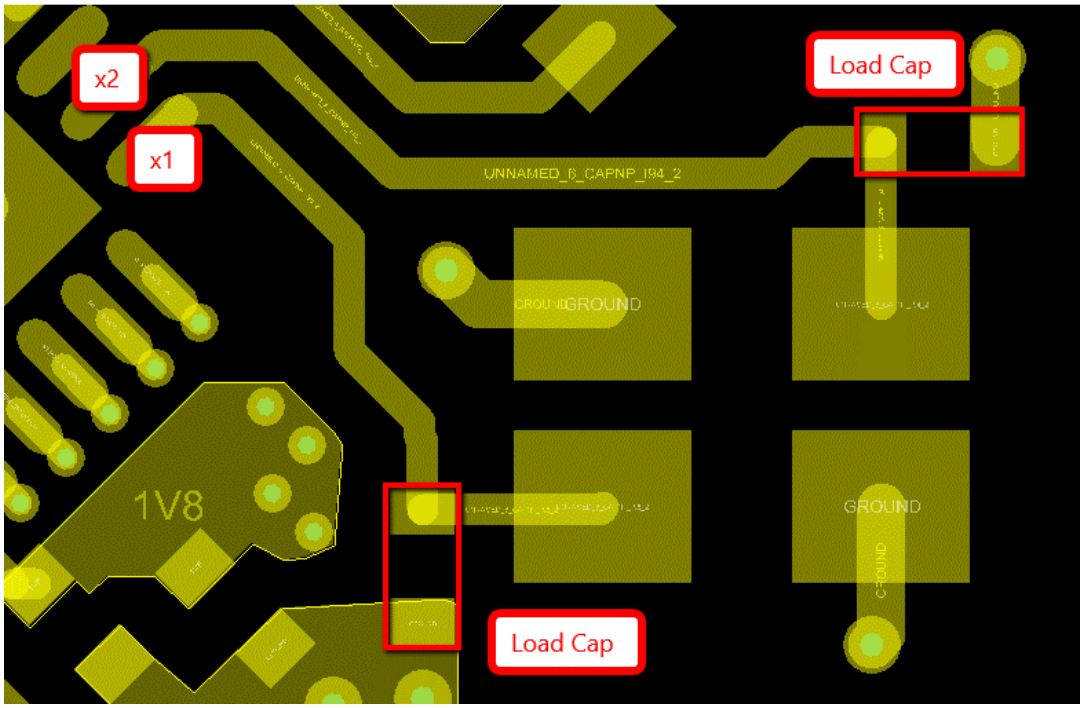


Figure 3.2.M. Example Crystal Layout for GMSL2 Designs

3.2.7 DC Bypass Capacitors

- Place the smallest capacitor closest to the SerDes power pin.
- Orientate DC bypass capacitors so that the GND is common, and there are no separate GND islands.

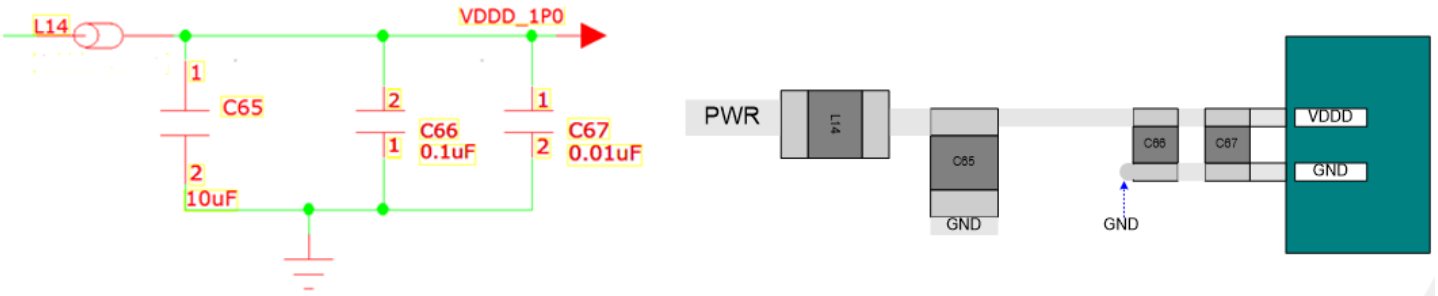


Figure 3.2.N. Bypass Capacitor Placement Example

3.2.8 Thermal Considerations

GMSL2 SerDes products are intended to operate within a specific temperature range as measured at a P-N junction in the die. Operation outside of this range could result in poor performance or shortened life of the product. Analog Devices recommends a thermal simulation of the system when possible and later, measuring component temperature using on-chip diodes or voltage references.

Board design stackup, proximity to other heat-generating components, airflow, heat sinks, ground planes, etc., all affect the operating temperature of the device.

Temperature parameters for integrated circuits are typically specified in one or more of the following terms:

- T_J (Junction Temperature),
- Θ_{JC} (Thermal Resistance, Junction to Case in degrees C per Watt), or
- Θ_{JA} (Thermal Resistance, Junction to Ambient in degrees C per Watt).

Please refer to Tutorial 4083 for an overview of Thermal Characterization of IC Packages (https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html).

The integrated circuit die is attached to the package lead frame with a conductive adhesive and covered in a plastic package. Each component has a thermal resistance to the ambient environment.

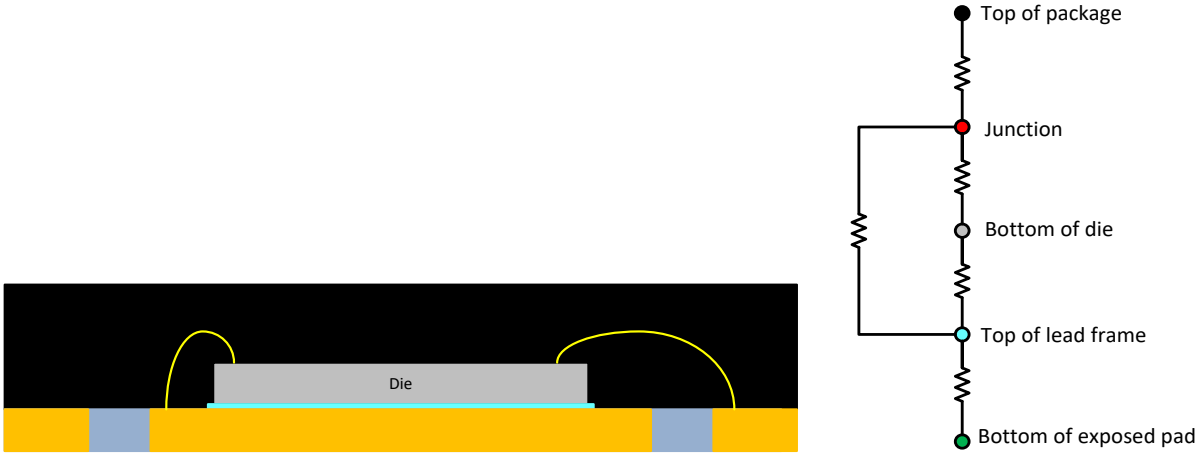


Figure 3.2.O: Die and Package Diagram of Typical Device and Typical Thermal Resistances of Integrated Circuit Packages

The top of the package can dissipate heat from the die to the surrounding air. The lead frame can dissipate heat to the printed circuit board through a metal pad and, to a much lesser extent, through the package pins.

Thermal specifications for each GMSL2 device are given in their relevent data sheets.

3.2.8.1 Layout Recommendations

To help with thermal performance, Analog Devices recommends at least a 5 × 5 array of vias in the exposed pad (EP), with additional vias close to the high-speed ports. If possible, more vias should be used, and especially on the display SerDes a 7 × 7 array should be used if possible.

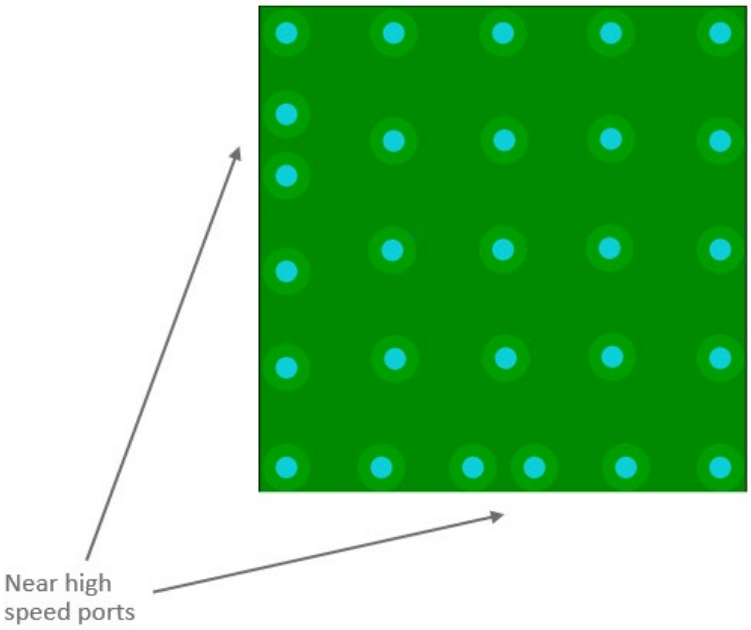


Figure 3.2.P: Thermal Vias in the EP of the IC

3.3 Connectors and Cables

3.3.1 Cabling

Cabling is an important component of the GMSL2 channel. Different cabling has different characteristics that play an important role in the channel specification. Typically, lightweight, flexible cabling with small bend radius is low-cost because the size of the center conductor(s) is small, so less copper. It is up to the system designer to select the appropriate cable that meets the GMSL2 channel specification. Cabling with thicker center conductor often has better insertion loss and return loss characteristics that allow for longer links while still meeting the channel specification. Different cables can be used to utilize their different properties. For example, the areas that are difficult to route to and bend many times throughout the lifespan of a vehicle, such as a trunk or mirrors, can use a short segment of more flexible cable. The segment that uses the longer cable run can use the thicker cable with better insertion loss characteristics.

Differential cabling should have 100Ω characteristic impedance while Coax cabling should have 50Ω characteristic impedance. Typical DC resistance of the center conductors is approximately 0.1Ω to 0.2Ω per meter.

The STP cabling is differential cabling, which is two conductors that are twisted, wrapped in a single-shielded overbraid. The shielded twisted quad (STQ) cabling is four center conductors that are twisted together typically in a star-quad configuration wrapped in a single-shielded overbraid. Star-quad cabling uses the differential output of the GMSL2 PHY and offers a benefit over true STP for applications that require a differential pair plus power and GND. Another type of cabling is shielded parallel pair. This type of cabling is two center conductors parallel to each other, and each center conductor is individually shielded. This is a relatively new cable and connector technology that has promising data sheet specifications but has not been field tested.

For the price, Coax cabling offers a better insertion loss per meter and often provides the best solution for reliable link performance, flexibility, and weight versus STP cabling. A Coax cable can often cost less than a comparable STQ cable while offering as much as 50% longer cable runs in a channel.

Table 2. Cables to Consider

Name	Manufacture	Type
Dacar 686-3	Leoni	STP
Dacar 535-2	Leoni	STQ
Dacar 636-3	Leoni	STP
Dacar 462	Leoni	Coax
Dacar 302	Leoni	Coax
102969	GG	Coax
GG X9305	GG	STP

3.3.2 Connectors

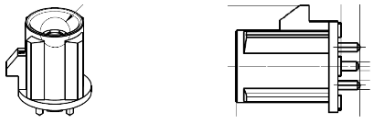
Connectors are arguably just as important as the cabling. Connector insertion loss is typically less than 0.5dB at frequencies of interest. The return loss of connectors is what needs to be watched out for. Proper layout techniques are required for the connector. It is strongly recommended to simulate the connector based on board stackup using a 3D simulation tool. Connector vendors should be able to facilitate this request.

Table 3. Connectors to Consider

Name	Manufacture	Link Configuration
FAKRA	Molex	Single Coax
FAKRA	Molex	Single Coax
HSAL2	Molex	Quad+
FAKRA	Rosenberger	Single Coax
FAKRA	Rosenberger	Single Coax
FAKRA	Rosenberger	Dual Coax
HFM (mini Fakra)	Rosenberger	Single Coax
HFM (mini Fakra)	Rosenberger	Dual Coax
HFM (mini Fakra)	Rosenberger	Quad Coax
Mini-FAKRA	Molex	Single Coax
HSD	Rosenberger	Quad (dual twisted pair or STQ)
FAKRA	TE	Dual Coax
FAKRA	TE	Single Coax
H-MTD	Rosenberger	Single/Dual/Quad Differential

3.3.3 Connector Modeling

> Rosenberger 59S10K-40MT5-Y Connector



> Rosenberger 59S2AQ-40MT5-Y_1 Connector

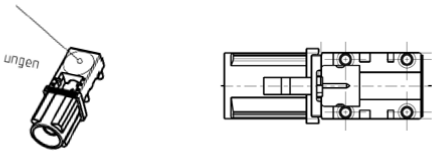


Figure 3.3.A: Straight PCB Plug vs. Right Angle Plug

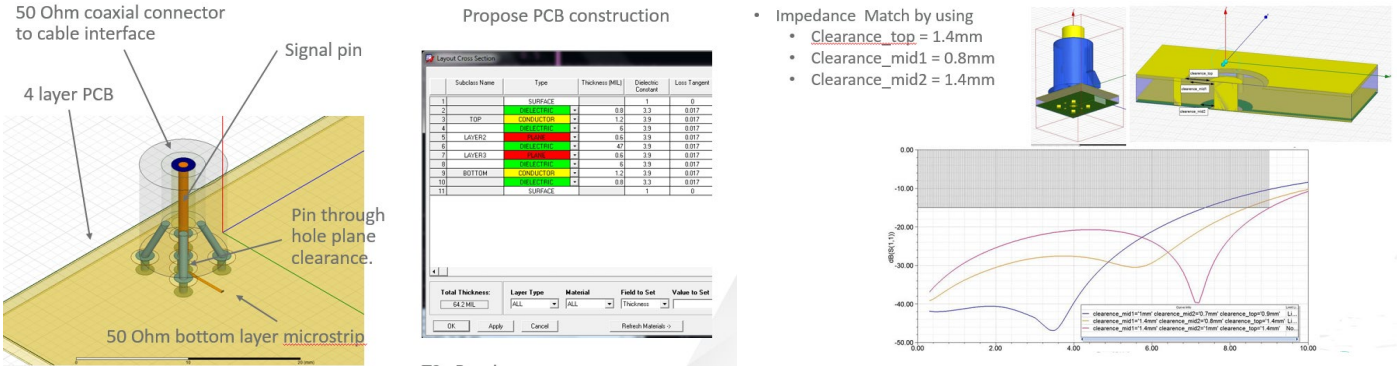


Figure 3.3.B: 59S10K-40MT5Y Connector

3.4 Line Fault

3.4.1 Line Fault Summary

The GMSL2 Line Fault Detection scheme requires only a single external resistor on each end of the serial link to detect various application fault conditions such as follows:

- Short to battery
- Short to GND
- Open line
- Line-to-line short

*Note: Line fault cannot be used with PoC as this does not provide accurate line detection measurements.

3.4.2 Coax Mode (Single-Ended) Hardware Requirements

The local side detecting the line fault requires a single 48.7kΩ connected directly from an LMNx pin to the serial link. The remote side of the serial link requires a 49.9kΩ connected to GND. All line fault resistors should be +/-3% accurate or better to ensure proper operation.

*Note: Line fault detection can be done in the serializer or deserializer, depending on where the microcontroller is located.

The following figures show the two options for line fault detection. Configuration 1 is typically used for display links and Configuration 2 is typically used for camera links; however, either configuration can be used on any device.

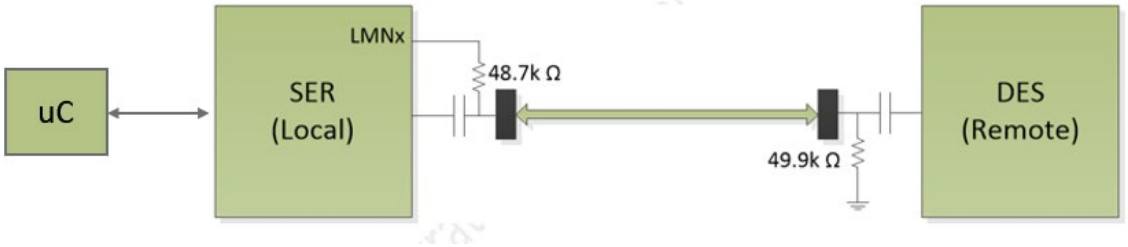


Figure 3.4.A. Line Fault Configuration (Example 1)

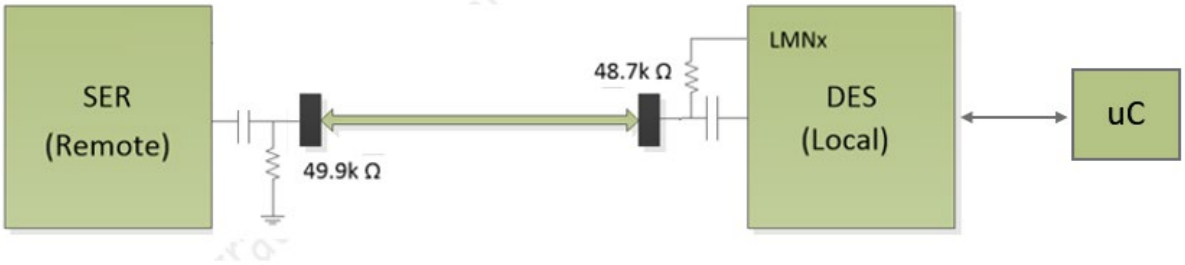


Figure 3.4.B. Line Fault Configuration (Example 2)

The LMNx pins (LMN0–LMN3) are typically mapped to different multifunctional pins on each unique part and package option. Some parts may have up to four line fault detectors depending on package and pin availability.

3.4.3 Twisted Pair Mode (Differential) Hardware Requirements

If operating in twisted pair mode, it is required to connect one line to an even-numbered LMNx pin and the other line to an odd-numbered LMNx pin. The even-numbered pins (LMN0 and LMN2) must be connected using a 42.2kΩ resistor; the odd-numbered pins (LMN1 and LMN3) must use a 48.7kΩ resistor. Line-to-line shorts can only be detected if LMN0 is paired with LMN1, or LMN2 is paired with LMN3, so for twisted pair applications ensure LMN0/1 or LMN2/3 are used for full operation.

The resistor values are critical for reliable line detection in the twisted pair mode and should be +/-3% accurate or better.

An example for twisted pair line fault operation is shown as follows:

Table 4. Line Fault Signals, Pin Pairs, and Resistors in Twisted Pair Mode

Signal	SIOA+	SIOA-
Ideal Line Fault Pair #1	LMN0, 42.2kΩ	LMN1, 48.7kΩ
Ideal Line Fault Pair #2	LMN2, 42.2kΩ	LMN3, 48.7kΩ

See example of the twisted pair line monitoring configuration in the Figure 3.4.C

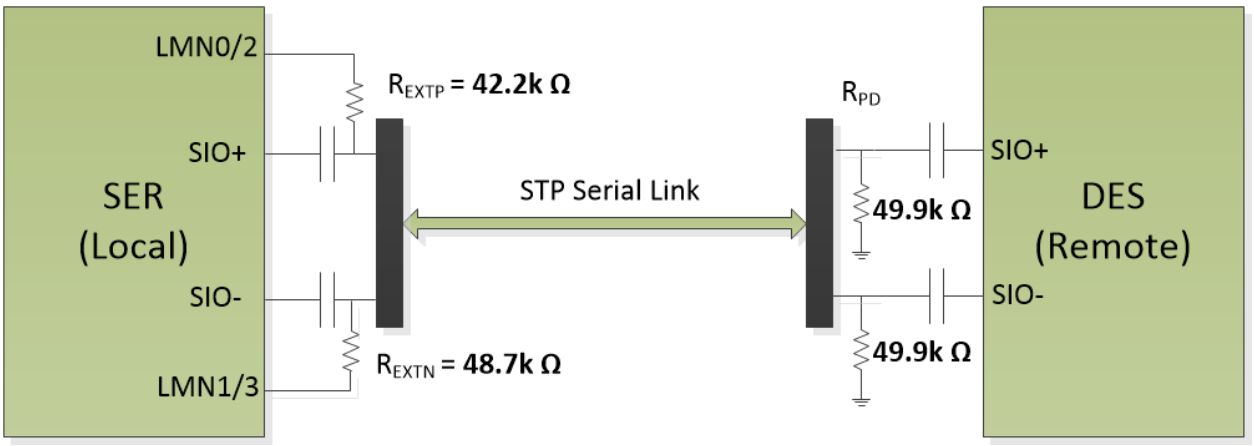


Figure 3.4.C. STP Line Fault Example

3.4.4 Simultaneous PoC and Line Fault

Line Fault cannot be used simultaneously with PoC

3.4.5 Layout for the Line Fault Resistor

The line fault resistor should be placed with the pad on the high-speed trace such that there is no stub on the serial trace. As described in the PCB layout section, ground cutouts are recommended for impedance matching. A layout for the line fault resistor can be seen as follows:

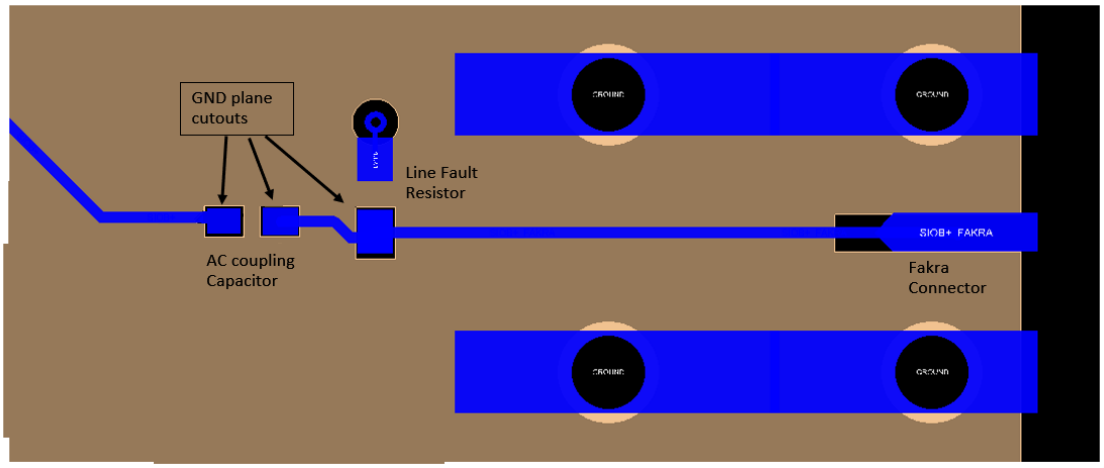


Figure 3.4.D. Line Fault Layout

3.5 Power over Coax

A well-designed GMSL2 or GMSL2 BC PoC filter should cover the forward and reverse channel frequency band, have great performance at lower frequencies and upper frequencies, and be optimized for size, cost, and current. It is important to verify that the channel is compliant with the addition of PoC, as the PoC filter introduces additional insertion loss and return loss to the channel. This document covers GMSL2 and GMSL2 PoC filter designs.

Power over Coax is a technique of sending power as well as data over a single coax cable, thus enabling the power of remote devices such as automotive cameras without the need for extra wiring or power circuitry. The PoC technique is desirable for camera applications because it reduces cabling in the vehicle. The PoC filters on a high-speed channel present a challenge due to the need to pass large amounts of current while functioning alongside a high-speed, large-bandwidth serial link. The basic implementation of a PoC is shown in Figure 3.5.A.

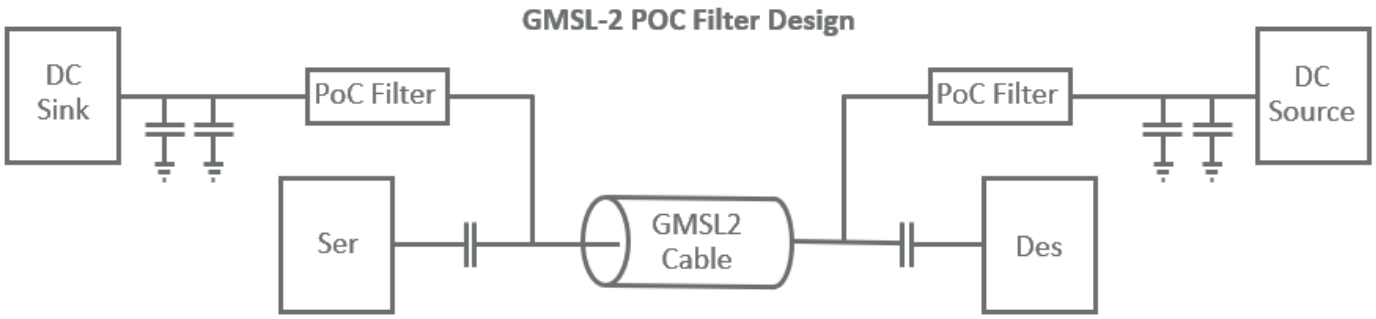


Figure 3.5.A. PoC System Design Block Diagram

3.5.1 Theory of Operation

A PoC filter is a notch filter which uses inductors to block the high-frequency signals on the channel from entering the power line while allowing direct current to pass. The AC coupling capacitors in the channel on the serializer and deserializer PCBs allow the high-frequency signals to pass from the transmitter to the receiver, while blocking DC power from entering the device.

The PoC design is a combination of RF and power electronics. Techniques from both fields must be utilized to effectively design a high-performance PoC circuit. Figure 3.5.B demonstrates the broad frequency band that a PoC filter must attenuate to not influence the high-speed data on the serial link.

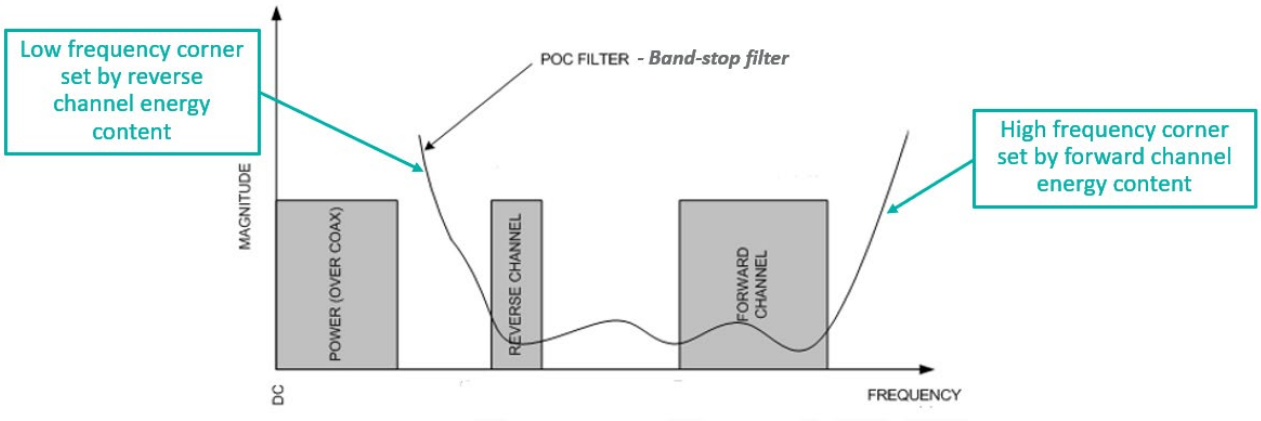


Figure 3.5.B. Transfer Function for PoC Circuit Showing the Frequency Bands of the Power Delivery, Reverse Channel, Forward Channel, and Attenuation of the PoC Filter

3.5.1.1 PoC Design: Self-Resonance Necessitates Multiple Inductors

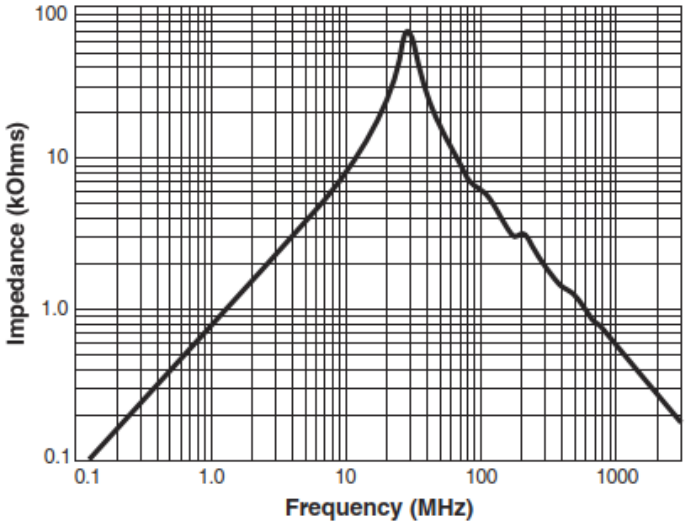


Figure 3.5.C. Inductance vs. Frequency for Typical Chip Inductor Showing Self-Resonant Frequency at 30MHz and Decay Above 30MHz

The inductors used in a PoC circuit are often wire-wound devices with ferrite compound cores and have high impedance and Q value at the self-resonant frequency. These types of power inductors have higher parasitic capacitance, while non-RF chip inductors have low self-resonant frequencies (SRF). Above the SRF, the inductor begins to act like a capacitor.

$$f_{SRF} = \frac{1}{2\pi\sqrt{LC_{par}}}$$

Equation 1. Self-resonant frequency (Hz) for inductor with inductance L and parasitic capacitance C_{par}

A PoC circuit is constructed from multiple inductors used to create a filter that attenuates a large frequency band that covers the full spectrum used by the GMSL2 forward and reverse channels, as a single inductor does not attenuate across a large enough frequency band. The inductors must be carefully chosen such that their combined frequency response provides enough attenuation across the full stopband frequency range, as shown in Figure 3.5.D.

The PoC network impedance is the sum of the impedances of the individual components. Note that due to complex impedance of each component, the total impedance may be less than the impedance of an individual component at a particular frequency.

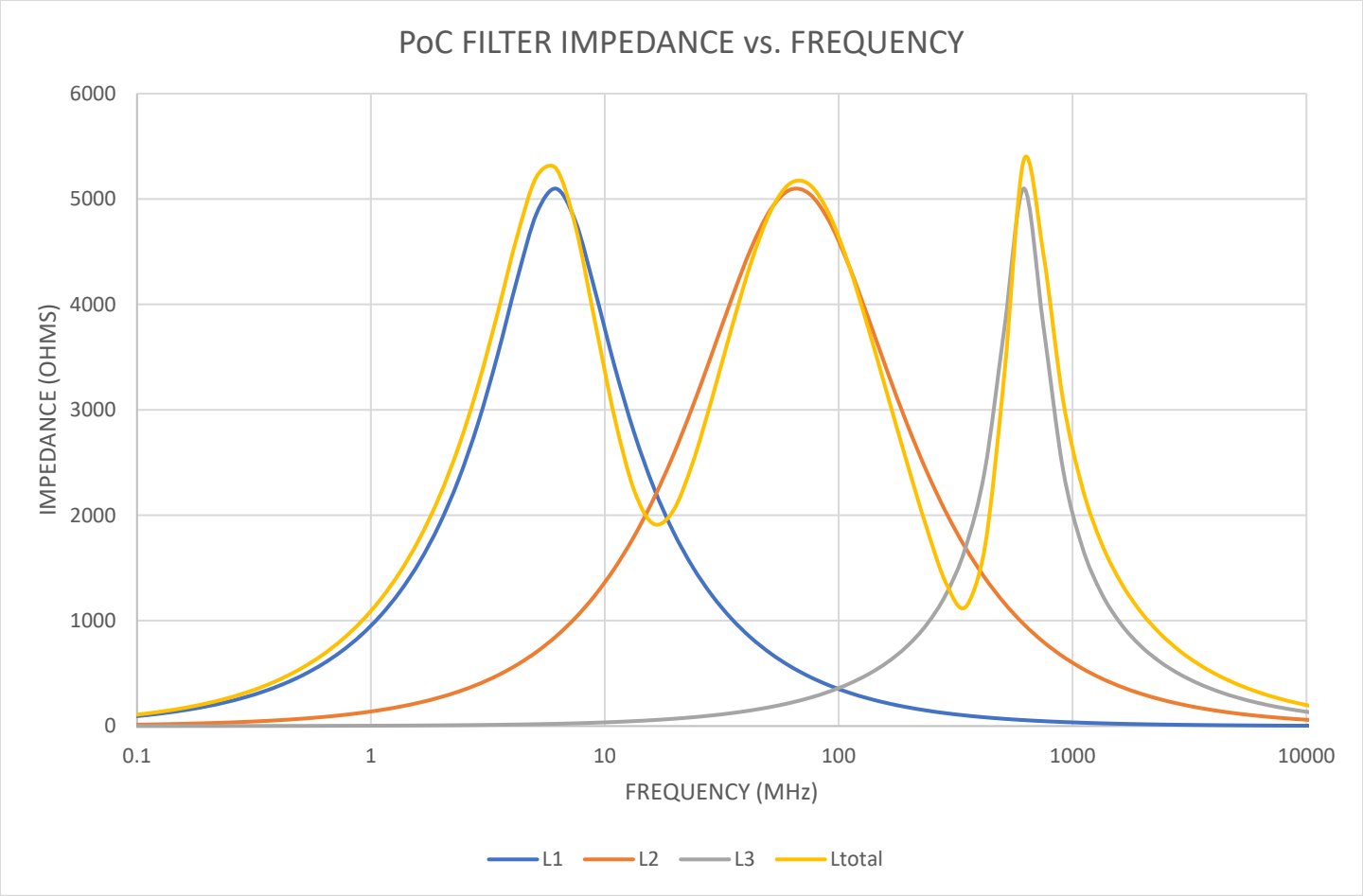


Figure 3.5.D. Frequency Response of a Three-Inductor PoC Network Composed of Inductors L1, L2, and L3 in Series. The Purple Line is the Overall PoC Frequency Response.

3.5.1.2 PoC Design: Effect of Bias Current

When selecting a combination of inductors based on data sheet specifications, special consideration is required. The values provided in inductor data sheets of impedance and inductance over frequency are typically measured with no applied current; however, **the DC bias current substantially affects the performance of inductors.** The effects of bias current include the following:

- Increased heat dissipation due to series resistance. Prolonged heating beyond typical values breaks down the inductor.
- Inductors function well in the linear region, but above a certain magnetic field, the flux density saturates. This corresponds to a decrease in effective inductance.
- The ferrite core of the inductor saturates thus decreasing its inductance. Air-core inductors do not saturate but are affected less by added DC.
- In ferrite-core inductors, past a certain current level, the effective inductance of the component becomes negligible.

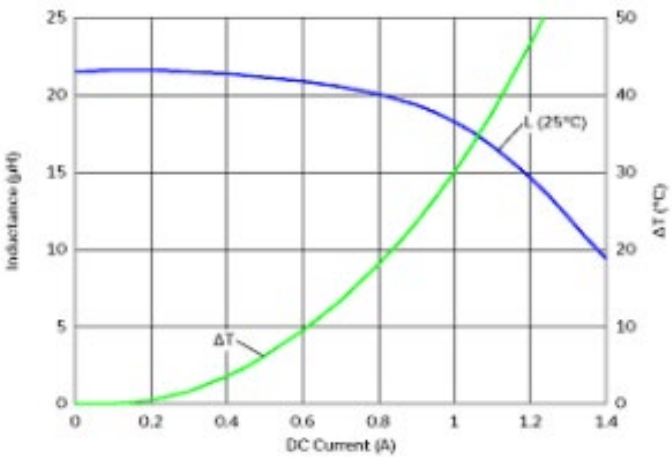


Figure 3.5.E. Effective Inductance of Chip Inductor and Temperature Rise vs. Current

Due to these effects, the inductance and impedance curves provided in inductor data sheets may not accurately describe how the inductor performs in a PoC network.

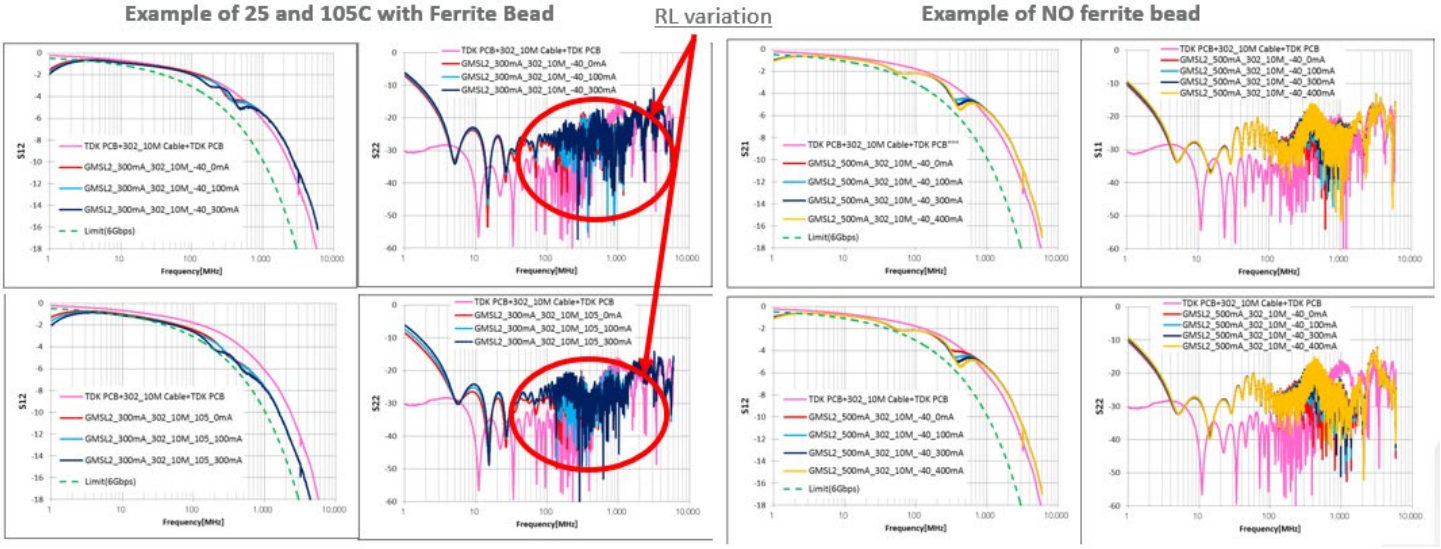


Figure 3.5.F: Ferrite Bead vs. Wire-Wound Inductor Comparison

In the case of PoC circuits under varying current conditions, the transfer function is not ideal. This is mainly because as current varies, the effective inductance decreases. In turn, the self-resonant frequency increases

(as parasitic capacitance is unaffected). The transfer function shifts right to a higher frequency and the impedance at a higher frequency is generally lower due to the decreased effective inductance. The shift in the impedance transfer function can be particularly detrimental when trying to filter a relatively narrow band, such as the reverse channel on GMSL2, as the transfer function may be shifted out of the band altogether and stop filtering the reverse channel.

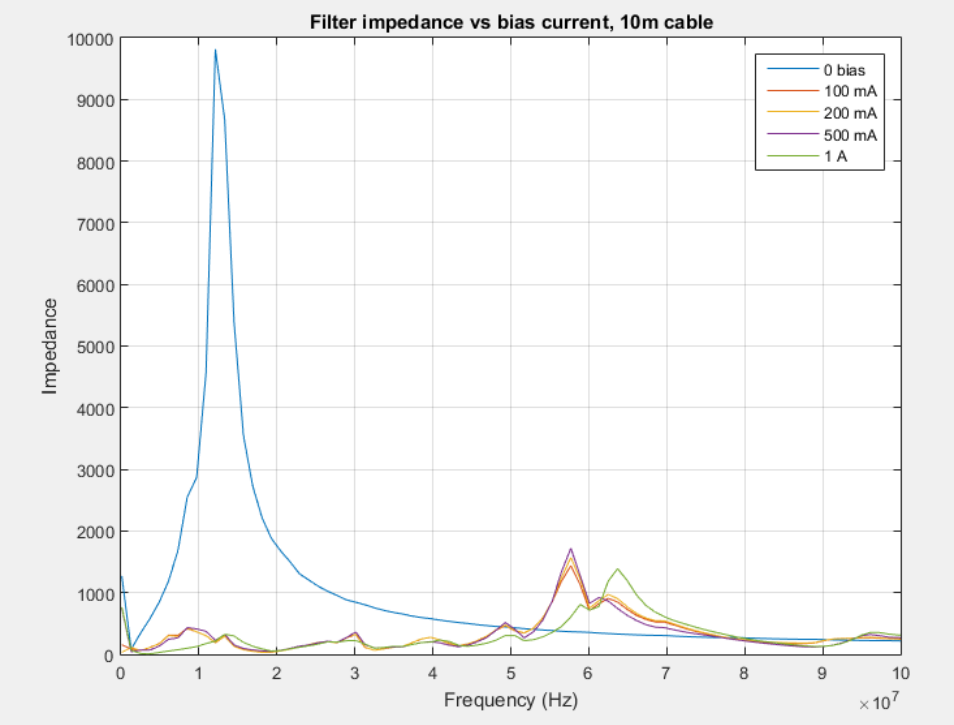


Figure 3.5.G. Impedance of PoC Filter with Applied Bias Currents

Figure 3.5.G characterizes the PoC filter with an applied bias current from 0A to 1A. The peak impedance decreases due to a decrease in effective inductance. As the inductor material breaks down with increased current there is a shift to the right due to change in the self-resonant frequency.

Analog Devices is no longer recommending ferrite beads for PoC designs due to their performance sensitivity to increases in temperature and current.

3.5.2 PoC Design and Validation Process

Analog Devices requires PoC filter to fully pass GMSL channel specification insertion and return loss parameters and maintaining a minimum 1kΩ impedance from 7MHz to 3GHz is recommended. The following outlined steps can be used to validate a PoC filter.

3.5.2.1 Selection of Inductors

Select inductors to cover the frequency band stated above. Consider the following effects:

1. Inductor Saturation Current
    a. Inductance drops as DC increases. This saturation current level is also temperature-dependent. A rule of thumb is to have the saturation current affect the inductance by no more than 10% from the zero-current value.
2. Inductor DC Resistance
    a. The DC resistance should be kept low. The DC resistance affects the PoC circuit in the following two ways:
        i. Voltage drops across the filter which affects power supply headroom and noise rejection.
        ii. Power dissipation inside the inductor which limits load current/operation temperature.
3. Inductor Q and Parallel Resistances
    a. The impedance of an inductor is often very large at one frequency and quickly tapers off away from the self-resonant frequency. Addition of a large parallel resistor increases its Q which broadens the frequency range of the inductor impedance, at the expense of the maximum possible impedance.

3.5.2.2 Selection of AC Coupling Caps

Choose 0.1uF (GMSL2) capacitors to block the PoC voltage from the high-speed GMSL2 pins. Consider that DC biasing of the capacitors affect the capacitance value. A general rule is to select capacitors that have a DC voltage rating at 2x-3x the expected DC bias.

3.5.2.2.1 Inductor Saturation Current

Inductance drops as DC increases. A rule of thumb is to have the saturation current affect the inductance by no more than 10% from the zero-current value.

3.5.2.3 Simulate the System with PoC Networks

Simulate the PoC network to see if the network is a candidate for bench testing.

3.5.2.3.1 Prepare Individual Component S-Parameters

Inductor vendors typically supply S-parameters or lumped-element circuit models, so that the inductor can be simulated with a tool such as Simplis or ADS. This can be useful for initial PoC circuit design; however, there are limitations with using a simulation model, specifically that inductor models are not typically provided for various current loads or different temperatures. Contact the component suppliers to get S-parameters for worst-case conditions due to bias current and temperature.

As stated, current and temperature effects are critical to PoC performance and usually need to be characterized on the bench.

3.5.2.3.2 Simulate the PoC Filter

Simulate the PoC filter and check for a minimum 1kΩ impedance from 7MHz to 3GHz (50kHz to 3GHz for GMSL2).

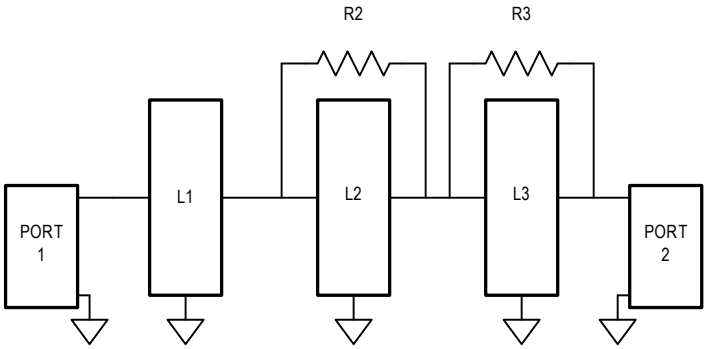


Figure 3.5.H: Example Simulation Schematic for PoC Impedance

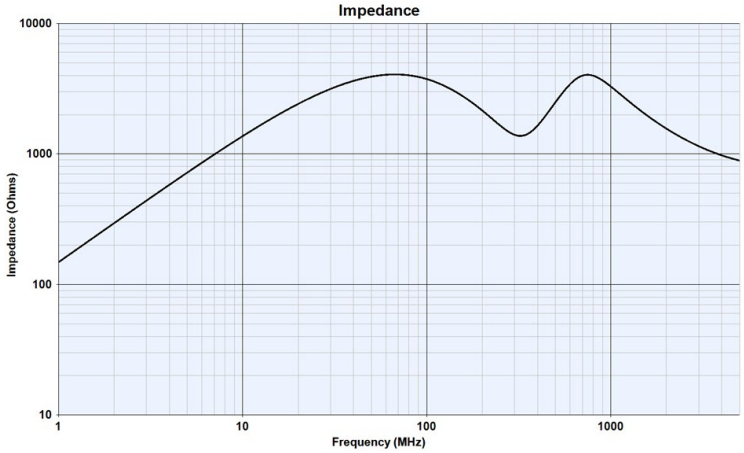


Figure 3.5.I: Example Simulation Result PoC Impedance

3.5.2.3.3 Prepare Board/Cable S-Parameters

Layout the board and get an estimate for the S-parameters of the board. Simulation of the boards differ than simulation of the components due to the traces/vias and ground planes.

3.5.2.3.4 Simulate Board/Cable System

With all the S-parameters, simulate the entire system. Ensure that the simulated results pass the channel specifications. Note that a GMSL2 link should pass both the GMSL2 and GSML1 channel specifications.

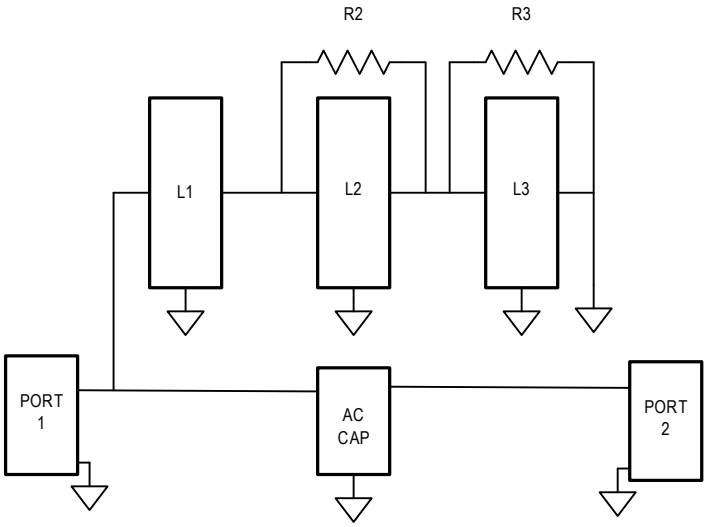


Figure 3.5.J: S-Parameter Simulation Using S-Parameter Data Measured on Each Board

3.5.3 PoC Bench Verification

Validate the simulations on the bench for the components and cables.

3.5.3.1 Measure Cables and Inline Connectors

Use a Vector network analyzer to measure the S-parameters of the cable and inline connectors. These should ideally be tested with “aged cables” to simulate the worst-case cable conditions.

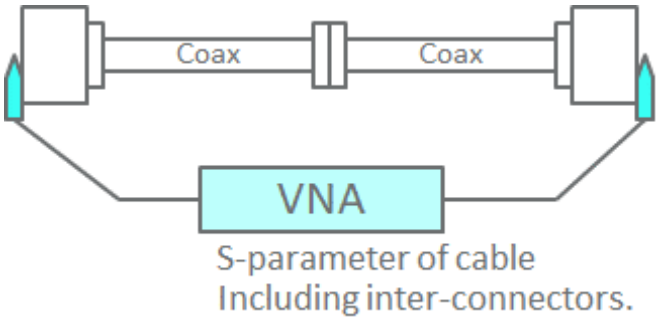


Figure 3.5.K. S-Parameter Measurement of Cable/Inline Connector

3.5.3.2 Measure PoC Circuit S-Parameters

Construct the PoC circuits on small PCB “coupon boards” (Figure 3.5.L). This allows for quick evaluation of different PoC components with the target cables without the need to layout and build an entire system. It is recommended to use the same board material and stackup as is planned for production design, as it allows both the PoC network and the layout to be characterized. Connector layout and PoC component placement and layout can significantly affect S-parameters.

Figure 3.5.L: An Analog Devices PoC Coupon Board Consisting of the DC Bias Input/Output, the VNA Port Connection, and a Fakra Connector to Connect a Cable and Second Coupon Board to Evaluate a Complete Link

To verify the components, use one board to represent the serializer and a second board to represent the deserializer (Figure 3.5.M). Test the boards over temperature, max current, and max cable length (Figure 3.5.N). S-parameters are captured over all the system corners and are required to pass the GMSL channel specifications with enough margin to cover the additional losses and mismatch of the final PCB.

*Note: Many Vector Network Analyzers (VNAs) do not allow DC bias voltage. A DC block (calibrated out through VNA calibration) may be needed to protect the VNA.

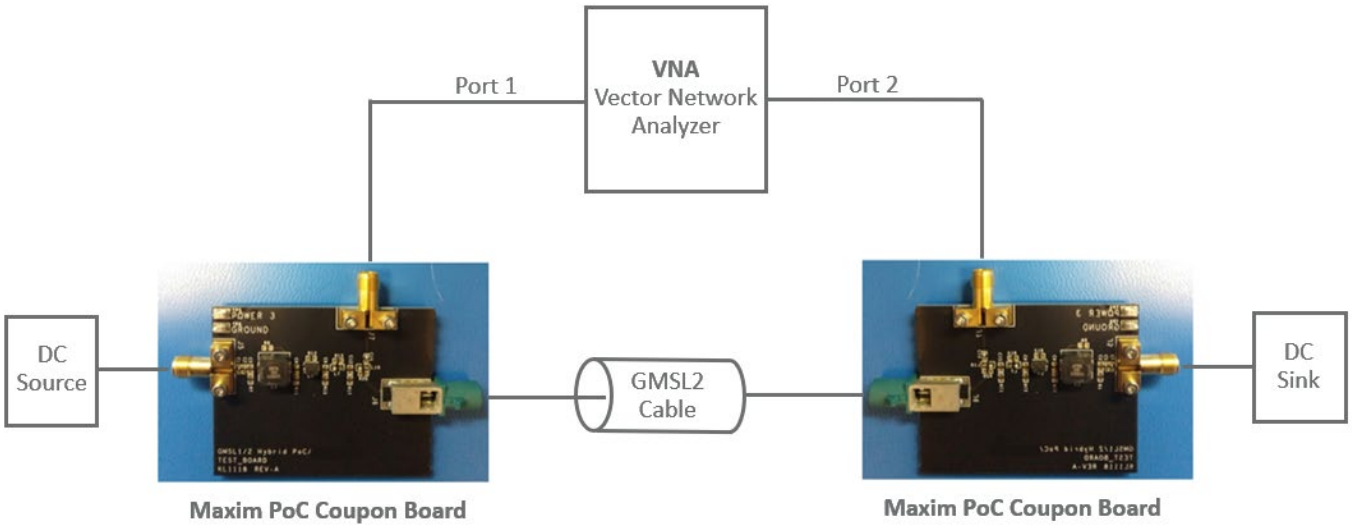


Figure 3.5.M. Block Diagram of How a Coupon Board is Used to Capture PoC S-Parameters under Varying Channels, Current Loads, and Temperatures

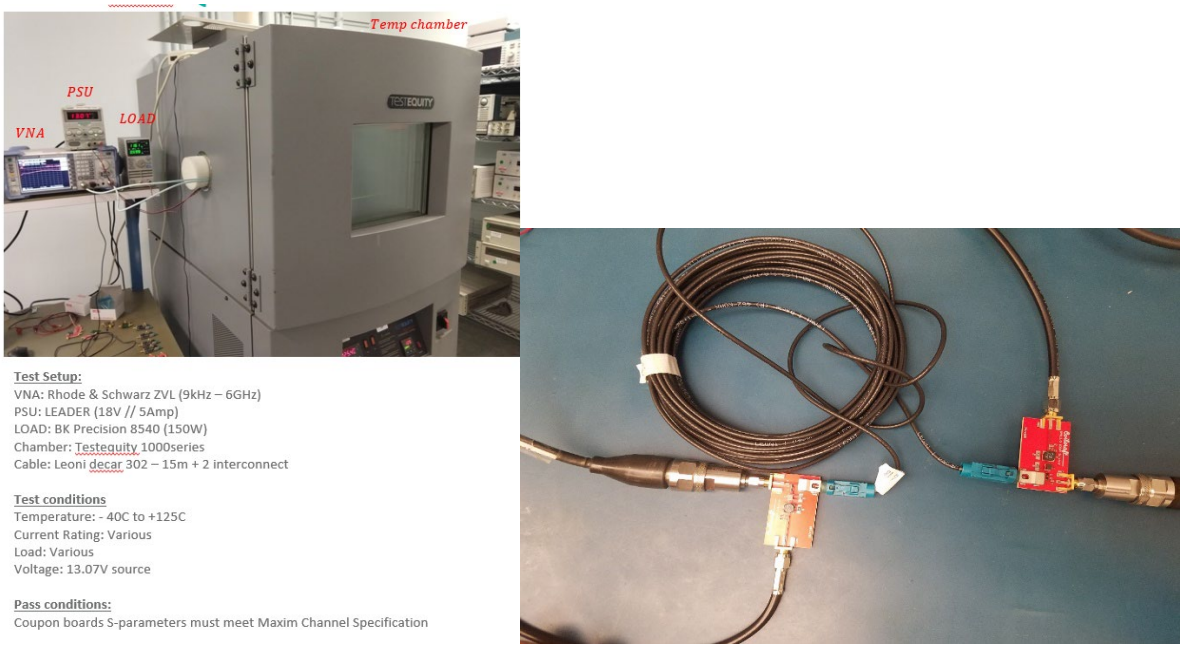


Figure 3.5.N: Coupon Boards and 15m Cable (left) and Test Setup with DC Load, VNA, and Temp Chamber (right)

3.5.3.3 Measure System S-Parameters

Measure the S-parameters of the final system PCBs with the following modifications (Figure 3.5.O):

- Remove the GMSL2 ICs from the PCBs and replace with a SubMiniature version A (SMA) connector pigtail. This allows a test of the full high-speed GMSL2 trace.
- Disconnect the PoC load and replace with an equivalent load of the maximum power draw of the system. This guarantees that the maximum load (worst-case inductor performance) is seen.
- Disconnect the Power IC and replace with an external power supply. This ensures that the maximum bias voltage (capacitor stress) and maximum current can be supplied.

Measure the S-parameters over temp, voltage, and cable length to ensure that the link meets the channel specifications.

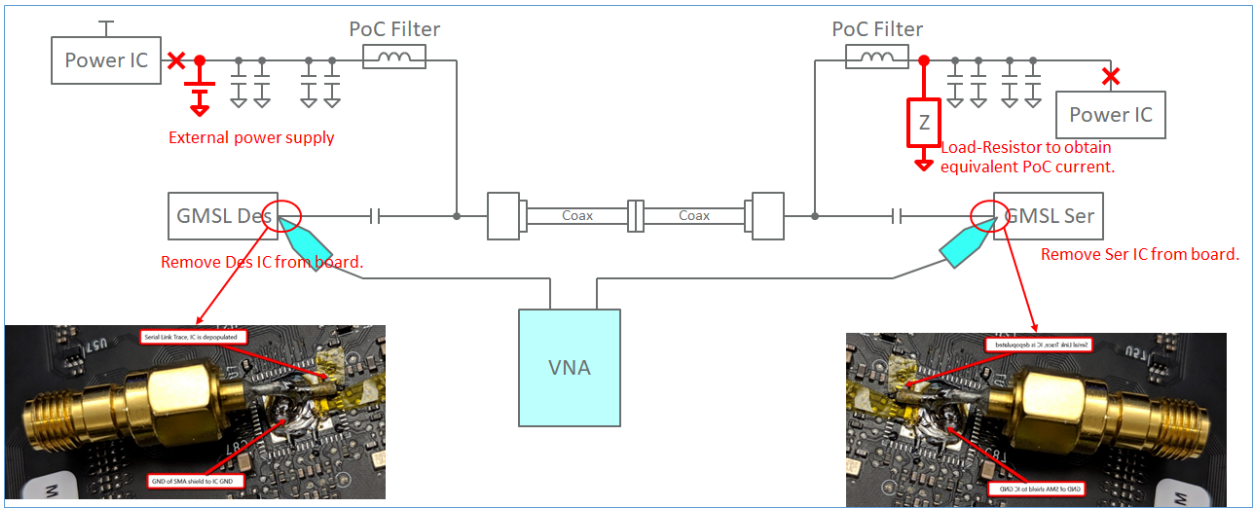


Figure 3.5.O. S-Parameter Measurement on Entire System

3.5.3.4 Measure Serializer/Deserializer S-Parameters (Alternate)

If the full system is not available, the S-parameters of a single board can be taken instead (Figure 3.5.P).

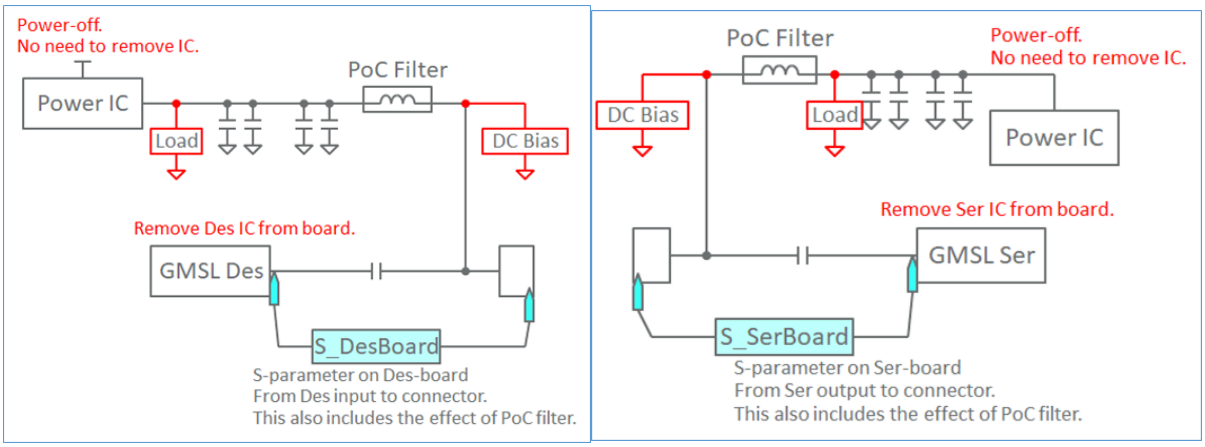


Figure 3.5.P: S-Parameter Measurement on Serializer or Deserializer

Disconnect the GMSL2 IC and the power supplies in a similar manner to the full system case. The measured board S-parameter return loss needs to match the GMSL2 specifications. The S-parameter insertion loss needs to have enough margin to account for the cable, and a second board. For example, assuming an insertion loss specification of 20dB and a cable loss of 8dB, the board's insertion loss would need to be no greater than about 5dB so that the combined insertion loss (5 + 5 + 8 = 18dB) is less than the channel specification of 20dB.

3.5.4 PoC Layout Recommendations

The PoC component placement and routing is shown below to reduce the amount of capacitance:

- If the GMSL2 trace is longer than 2in, it is suggested to place the PoC within a couple of inches of the IC.
- Routing highest to lowest SRF inductor on the GMSL2 line is critical. Highest value should be placed directly on the GMSL2 serial link trace followed by the next highest, and so on. See Figure 3.5.Rfor a placement example.
- Place first component orthogonal to high-speed trace.
- Remove necessary ground beneath inline inductor to serial link trace to match the impedance to 50Ω.
- Minimize the distance between IC, PoC, and connector.
- Place all PoC components on the same layer. Do not add vias as the added inductance may create unwanted filter response.
- Cut out the ground on open coil inductors where the coil is exposed.

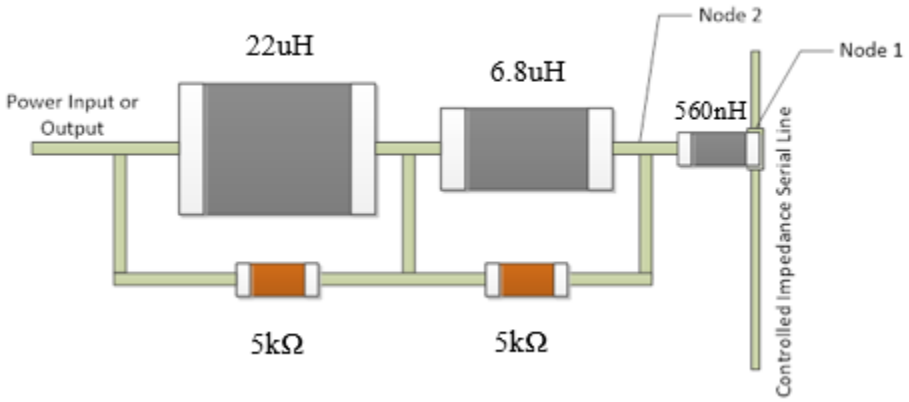


Figure 3.5.Q. PoC Placement Strategy

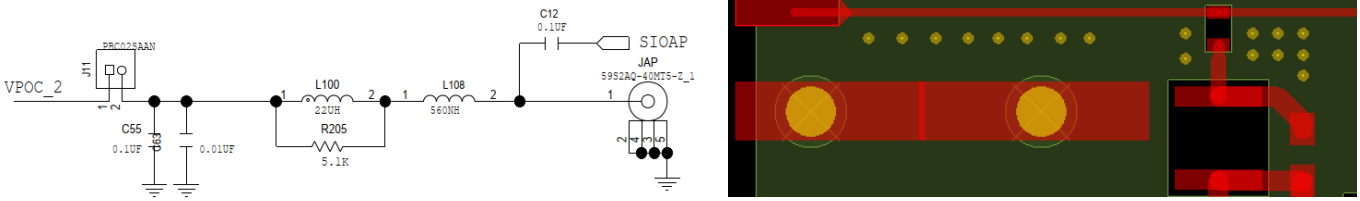


Figure 3.5.R: PoC Placement and Routing Example

3.5.4.1 Ground Cutout on 50Ω GMSL2 Trace

To avoid ground cutouts, it is recommended to try to select a stackup such that the trace width for the target impedance (50Ω single-ended or 100Ω differential) matches the largest component pad size. This would eliminate the need to have ground cuts around the components. In many cases, this is not possible due to certain design constraints, so it is recommended to follow the guidelines (as mentioned) to help minimize impedance mismatches.

When a component's pad is larger than the serial link trace, a ground cutout is needed. The size of the ground cutout depends on the board stackup and the size of the component pad. For example, in the following layout a 0402 component is used with a 1.35X cutout and ~0.3mm spacing to the adjacent ground. This design is using a 12mil ~0.305mm trace for a 50Ω match with an adjacent ground layer spaced approximately 6mils from the trace.

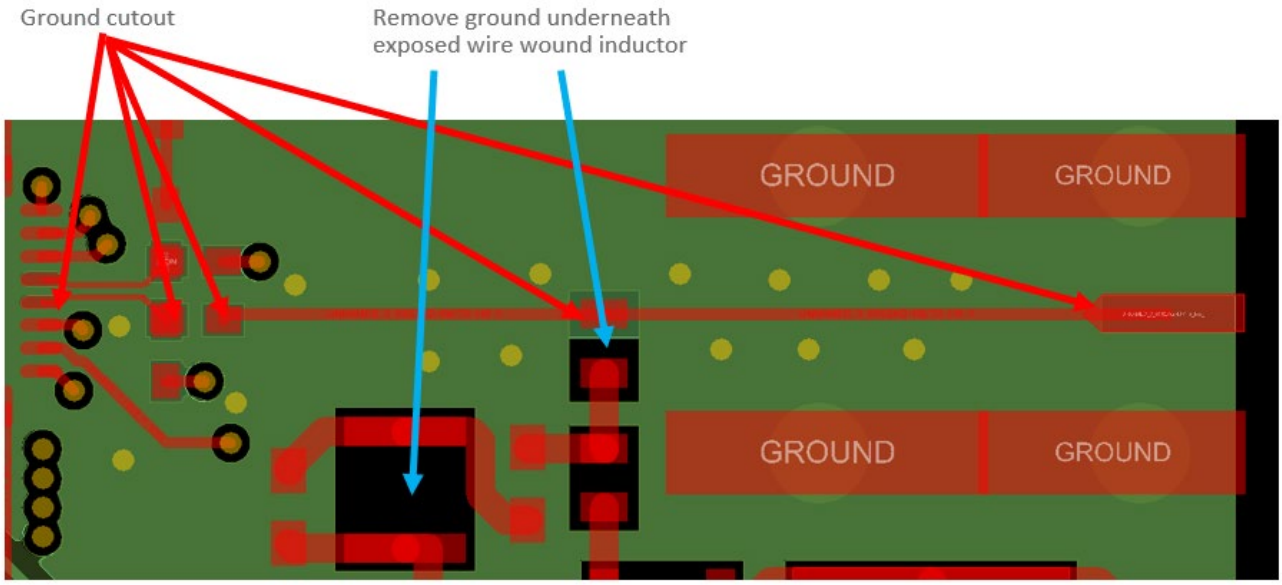


Figure 3.5.S: PoC Layout Example Showing Single-Layer Ground Cutouts under the IC Pad, AC Coupling Cap, First PoC Component, and Fakra Connector Pad. Full Board Cutout is Shown Under the Wire-Wound Inductors

Proper impedance matching requires ground cutouts below components that have a bigger pad size than the matched 50Ω trace. It is highly recommended to perform a high-speed simulation to determine the proper depth and width of the ground cutout for the design.

3.5.4.2 Determining Ground Cutout Depth

When matching a 50Ω trace to a dense PCB stackup, a small trace size is typically needed, which creates a discontinuity when the matched trace reaches the large component pad. To compensate for this mismatch in impedance, it is recommended to remove adjacent ground layers to effectively lower the capacitance below the component pad. To confirm the ideal distance Analog Devices recommends running a simulation to confirm.

3.5.5 PoC Reference Circuits

The following tables contain reference PoC circuits that have been evaluated but are not guaranteed to meet all customer use cases. Customers must ensure and evaluate that their chosen components meet the channel specification for their given system.

The PoC circuits Rev11, Hybrid2, and T2 are no longer recommended by Analog Devices due to unreliable results across temperature and inductor component corners. These previous solutions do not achieve high-link margin with variations that can occur in production designs. If the design is in production or late development

phases, Analog Devices recommends using the “drop-in” replacement solutions to help achieve better link performance. It is important to note that the components below may not be a direct drop-in replacement, and each customer design needs to be evaluated.

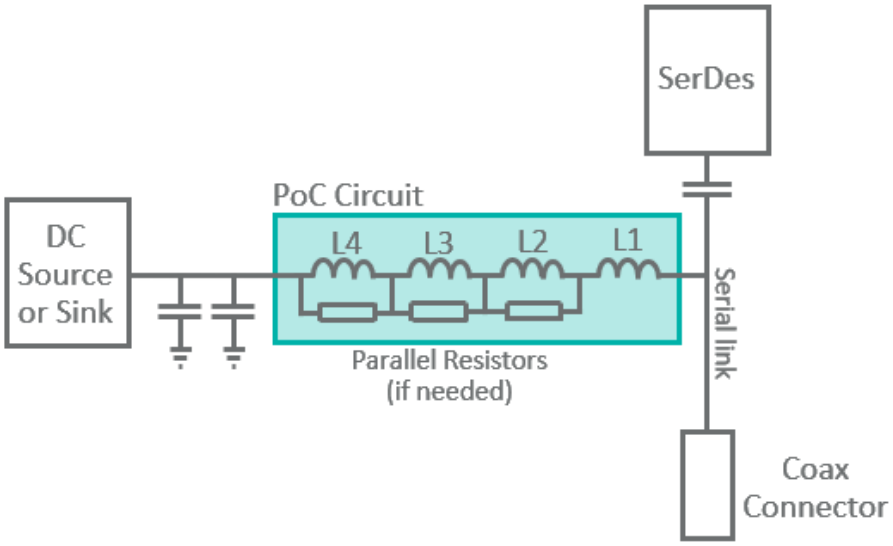


Figure 3.5.T. Schematic for PoC Reference Circuits

*Note the order of the inductors in Figure 3.5.T where L1 is placed on the serial link trace. Inductors should be arranged with the lowest inductance component on the serial link and highest inductance on the DC side of the filter. Also note the placement of parallel resistors, which are denoted in the following tables as “inductor || resistance value.”

Table 5. Recommended PoC Networks for GMSL2 and GMSL2/1 Links

#	Circuit Name/ Manufacturer	GMSL Version	Components	Inductance-SRF	Rated Current @ 12V	Current Rating at Maximum Insertion Loss for 6G/187M	Notes
1	C-2L-300 Coilcraft	2	L1: PFL1005-561 L2: 1210POC-223 || 5.1kΩ	560nH – 620MHz 22uH – 66MHz	440mA – 20% 520mA – 105C	***300 mA @ 105C***	Verified on EV kits
2	C-3L-280 Coilcraft	1/2	L1: PFL1005-561 L2: 1210POC-223 || 5.1kΩ L3: LPS4040-154	560nH – 620MHz 22uH – 66MHz 150uH – 6.1MHz	440mA – 20% 520mA – 105C 280mA – 10%	***280 mA @ 105C***	S-parameters have not been evaluated
3	C-2L-500 Coilcraft	2	L1: PFL1609-561 L2: 1210POC-223 || 5.1kΩ	560nH – 600MHz 22uH – 66MHz	780mA – 20% 520mA – 105C	***500 mA @ 105C***	Verified on EV kits
4	C-4L-1000 Coilcraft	2	L1: PFL1609-471 L2: PFL1609-471 L3: 1210POC-682 || 5.1kΩ L4: MSS6132T-223 ||5.1kΩ	470nH – 650MHz 470nH – 650MHz 6.8uH – 114MHz 22uH – 21MHz	990mA – 20% 990mA – 20% 1000mA – 105C 1120mA – 20%	***1000mA @ 85C*** ***800mA @ 105C*** ***600mA @ 125C***	Verified on EV kits
5	C-6L-2000 Coilcraft	2	L1: PFL1609-47N L2: PFL1609-47N L3: PFL1609-47N L4: 1812PS-22 L5: MSS6132T-682||5.1kΩ L6: XAL4040-153||5.1kΩ	47nH – 2250MHz 47nH – 2250MHz 47nH – 2250MHz 2.2uH – 270MHz 6.8uH – 47MHz 15uH – 20MHz	2.8A – 20% 2.8A – 20% 2.8A – 20% 3.0A – 30% 2.3A – 30% 2.8A – 30%	***2000 mA @ 85C***	
6	T1-450 TDK	1	L1: ADL2012-1R5M L2: ADL3225VT-100M || 1k L3: CLF6045NIT-101M-D || 1k	1.5uH – 450MHz 10uH – 100MHz 100uH – 10MHz	700mA – 105C 1300mA – 105C 800mA – 105C	***450mA @ 105C***	GMSL 1 solution – only verified with solutions "T-2L-400" and "T-3L-500"
7	T-2L-400 TDK	1/2	L1: ADL2012-2R2M L2: VLS5045EX-151M-H || 1k	2.2uH – 360MHz 150uH – 5MHz	400mA – 105C 490mA – 105C	***400mA @ 105C***	
8	T-3L-500 TDK	1/2	L1: ADL2012-1R5M L2: VLS3015CX-4R7M-H || 1k L3: VLS6045EX-151M-H || 1k	1.5uH – 450MHz 4.7uH – 55MHz 150uH – 4MHz	700mA – 105C 1260mA – 105C 510mA – 105C	***500mA @ 105C***	
9	T-2L-600 TDK	2	L1: ADL2012-1R5M L2: ADL3225VHC-150M || 1.5k	1.5uH – 450MHz 15uH – 90MHz	700mA – 105C 620mA – 105C	***600mA @ 105C***	
10	T-3L-600 TDK	2	L1: ADL3225VM-2R2M L2: ADL3225VM-2R2M || 1.5k L3: ADM32FSC-220M || 1.5k	2.2µH – 300MHz 2.2µH – 300MHz 22uH – 30MHz	1005mA – 105C 1005mA – 105C 630mA – 105C	***600 mA @ 125C*** ***600mA @ 105C***	Has not been verified at 125C
11	T-2L-300 TDK	2	L1: ADL2012S-1R2M L2: ADL3225VM – 150M || 1.5k	1.2µH – 500MHz 15uH – 80MHz	400mA – 105C 350mA – 105C	***300 mA @ 105C***	
12	T-3L-1000-01 TDK	2	L1: ADL3225VM-2R2M L2: ADL3225VM-2R2M || 1.5k L3: CLF5030NIT-220M-D || 1.5k	2.2uH – 300MHz 2.2uH – 300MHz 22uH – 28MHz	1005mA – 105C 1005mA – 105C 1150mA – 105C	***1000 mA @ 105C*** ***800mA @ 125C***	NOT recommneded for new designs. For new designs see "T-3L-1000-02" below. Not verified at 125C
13	T-3L-1000-02 TDK	2	L1: ADL3225VM-2R2M L2: ADL3225VM-2R2M || 1.5k L3: VLS5030EX-220M-D || 1.5k	2.2uH – 300MHz 2.2uH – 300MHz 22uH – 10MHz	1005mA – 105C 1005mA – 105C 1360mA – 105C	***1000 mA @ 105C*** ***800mA @ 125C***	Has not been verified at 125C

14	M-2L-300-01 Murata	2	L1: LQW18CNR65 L2: LQW32FT470 || 1.5k	650nH – 510MHz 47uH – 30MHz	320mA – 105C 300mA – 105C	***300 mA @ 105C***	
15	M-3L-600 Murata	2	L1: LQW18CNR21J0Z L2: LQW32FT2R2M0H || 1.5k L3: LQH3NPH150MME || 1.5k	210nH – 720MHz 2.2uH – 200MHz 15uH – 15MHz	800mA – 105C 600mA – 105C 620mA – 105C	***600 mA @ 105C***	
16	M-2L-300-02 Murata	2	L1: LQW21FT1R5 L2: LQW32FT220M0H	1.5uH – 260MHz 22uH – 50MHz	550mA – 105C 500mA – 105C	***300 mA @ 115C***	
17	M-3L-280 Murata	1/2	L1: LQW18CNR65 L2: LQW32FT470 || 1.5k L3: LQH44PH101 || 1.5k	650nH – 510MHz 47uH – 30MHz 100uH – 6MHz	320mA – 105C 300mA – 105C 320mA – 105C	***280 mA @ 105C***	
18	M-2L-1000 Murata	2	L1: LQW21FTR47 L2: LQW43FT100	470nH – 470MHz 10uH – 60MHz	1100mA – 105C 1000mA – 105C	***1000 mA @ 85C***	
19	M-2L-500-02 Murata	2	L1: LQW21FT1R0 L2: LQW32FT100 || 1k	1uH – 320MHz 10uH – 100MHz	700mA – 105C 620mA – 105C	***500mA @ 105C***	

*Note: Customers are responsible for testing and validating PoC solutions in their own system.

3.5.6 PoC Return Loss Measurements

The following plots are some reference PoC filters.

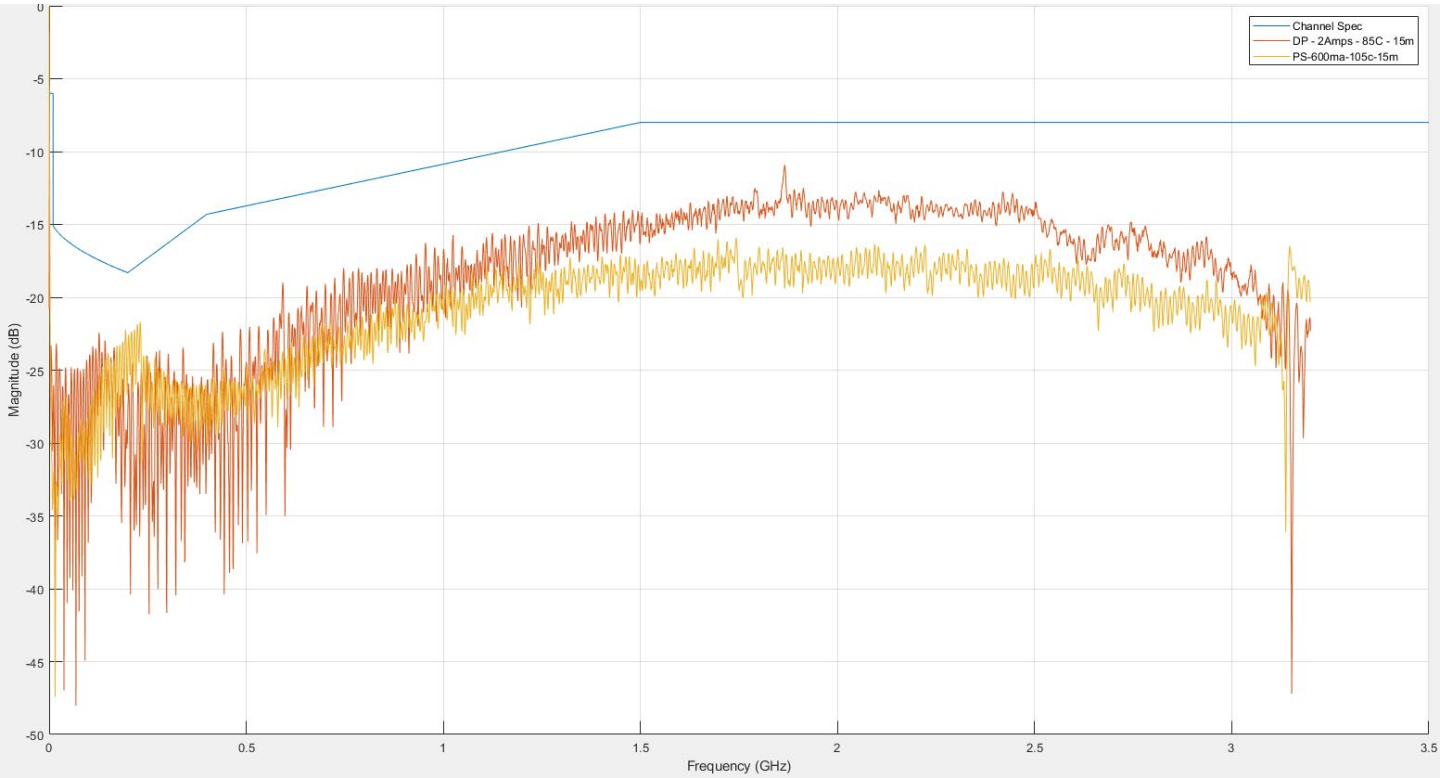


Figure 3.5.U: New Reference PoC Solutions—Coilcraft

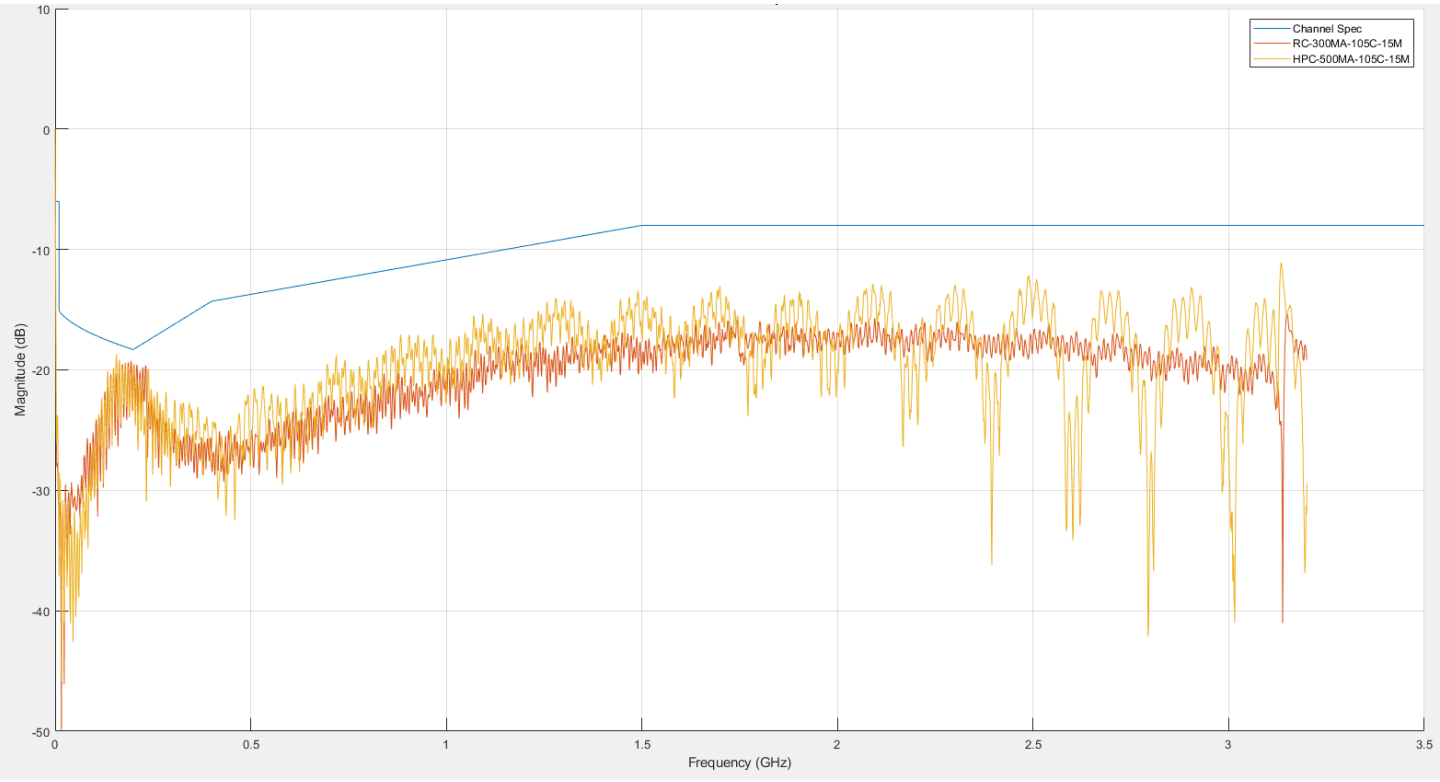


Figure 3.5.V: New Reference PoC Solutions—Coilcraft

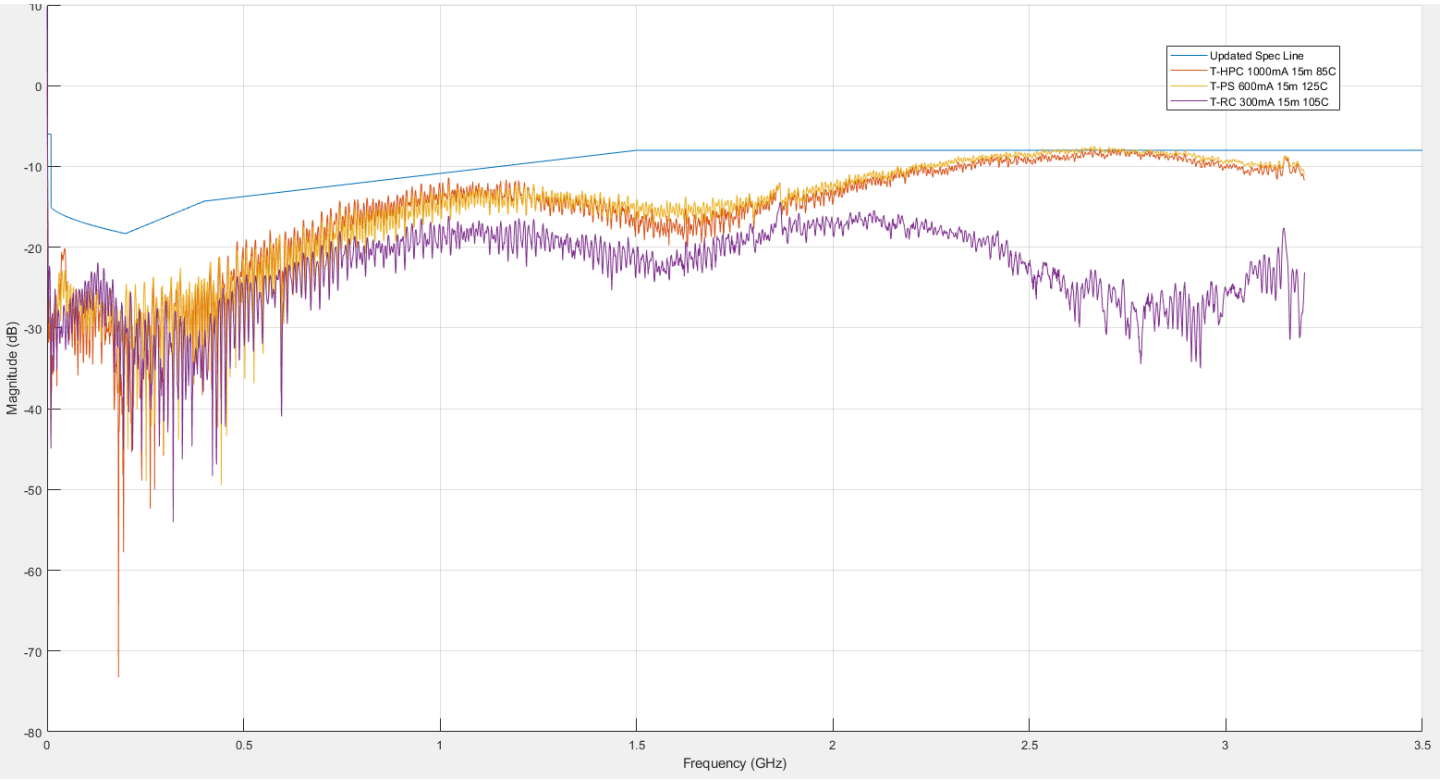


Figure 3.5.W: New Reference PoC Solutions—TDK

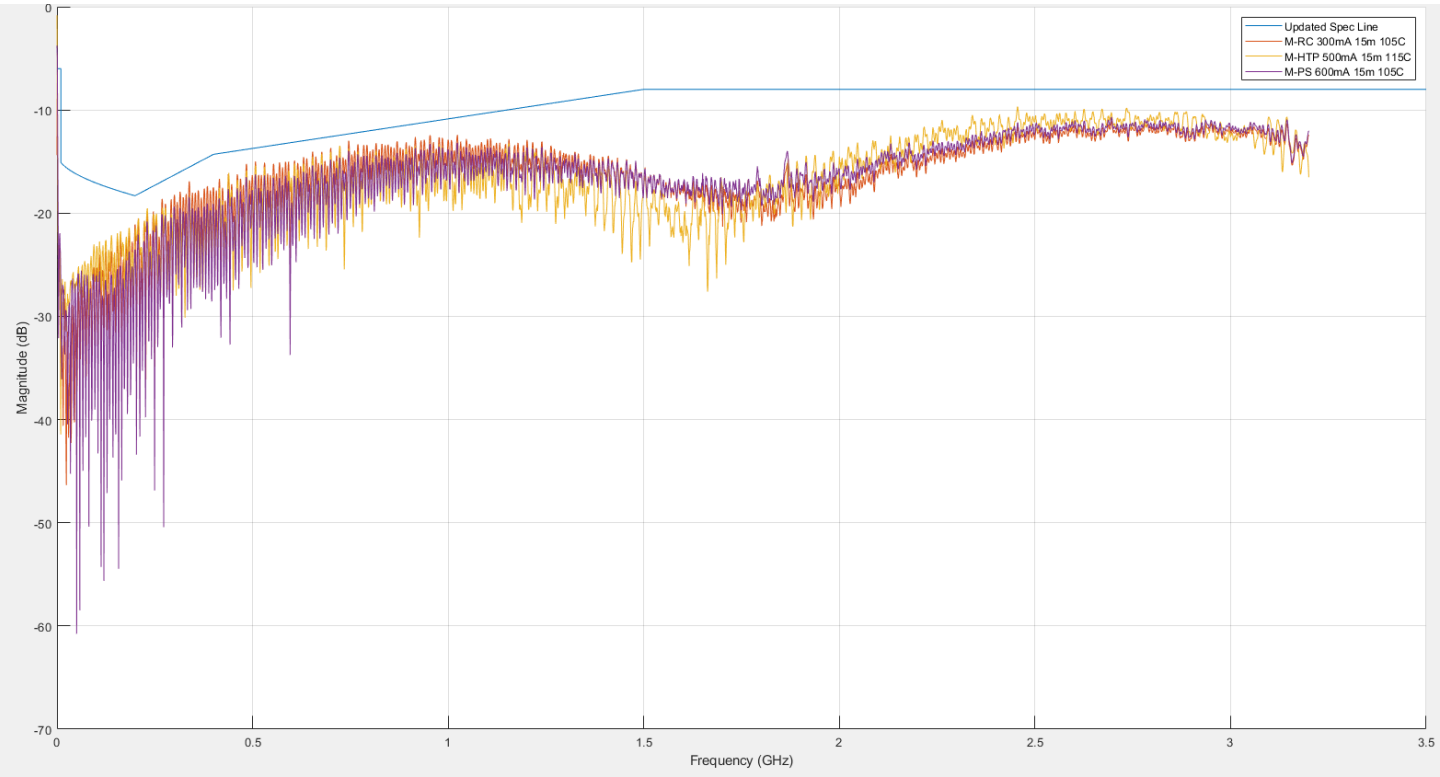


Figure 3.5.X: New Reference PoC Solutions—Murata

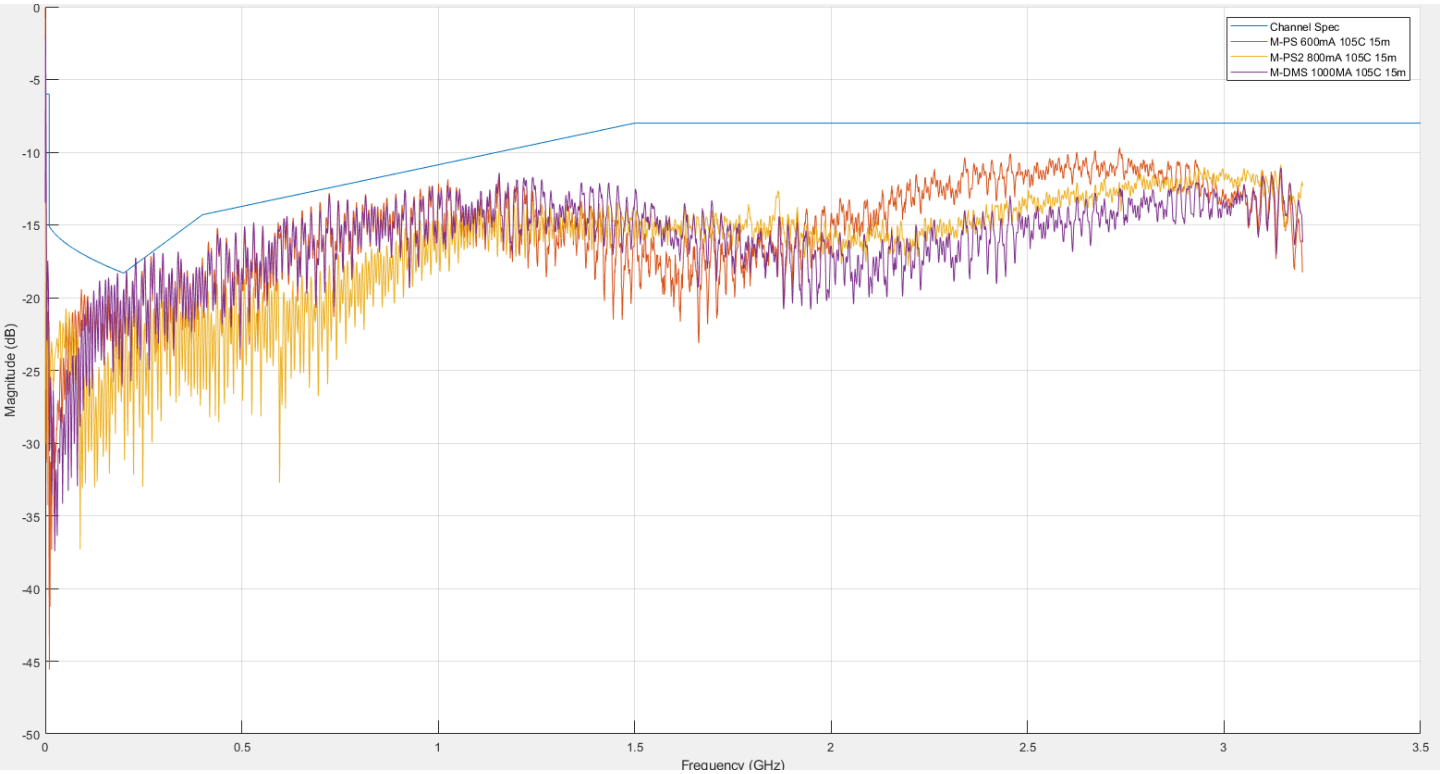


Figure 3.5.Y: New Reference PoC Solutions—Murata

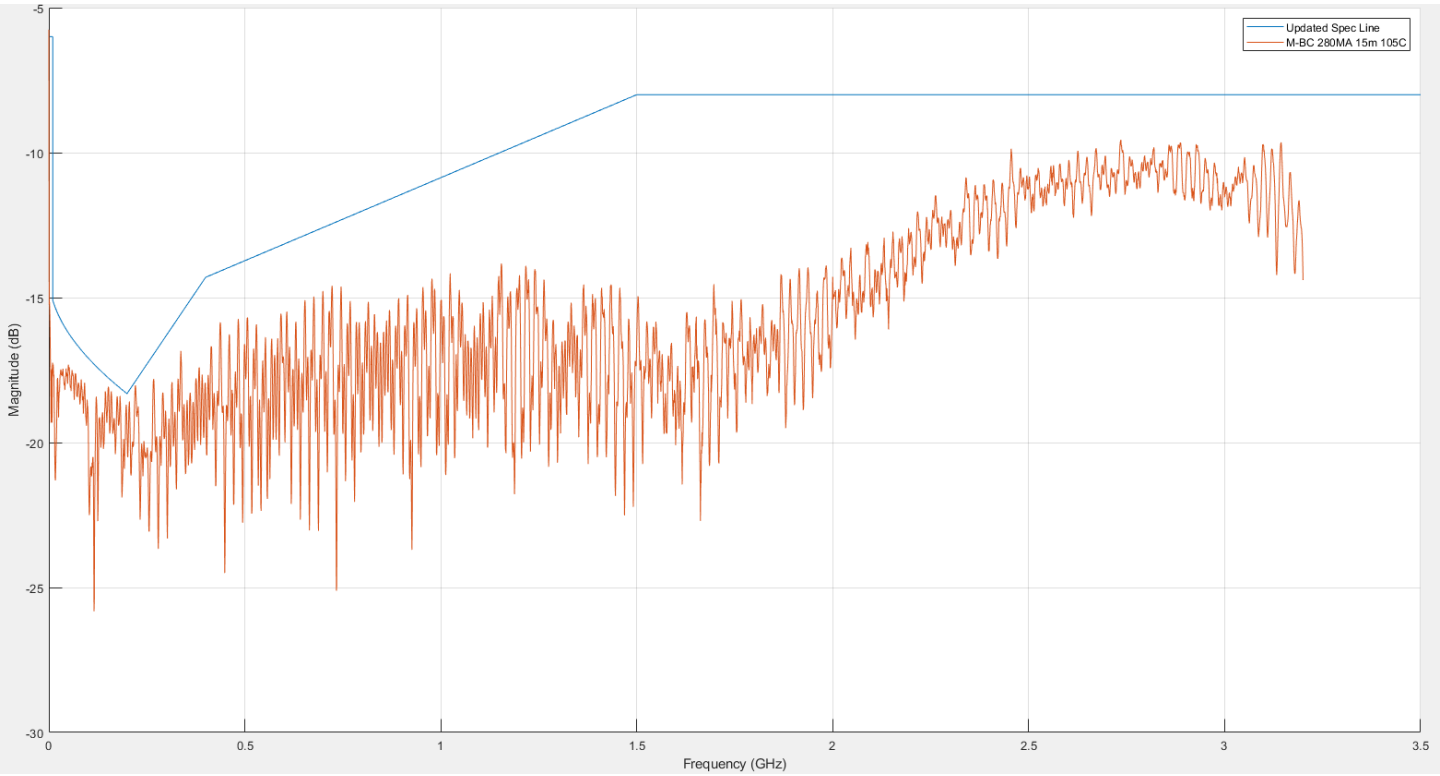


Figure 3.5.Z: M-BC Loss Coupon Board Measurements—Murata

3.6 ESD Guide

3.6.1 Overview

Electrostatic discharge (ESD) is the buildup of charge that may catastrophically damage electronics in a powered or unpowered system. Understanding and preparing for such events is critical for automotive systems.

This document covers system-level electrostatic discharge-related topics for GMSL2.

External ESD device recommendations can be seen in External Components section.

Figure 3.6.A shows basic GMSL2 PHY output and recommended ESD structures.

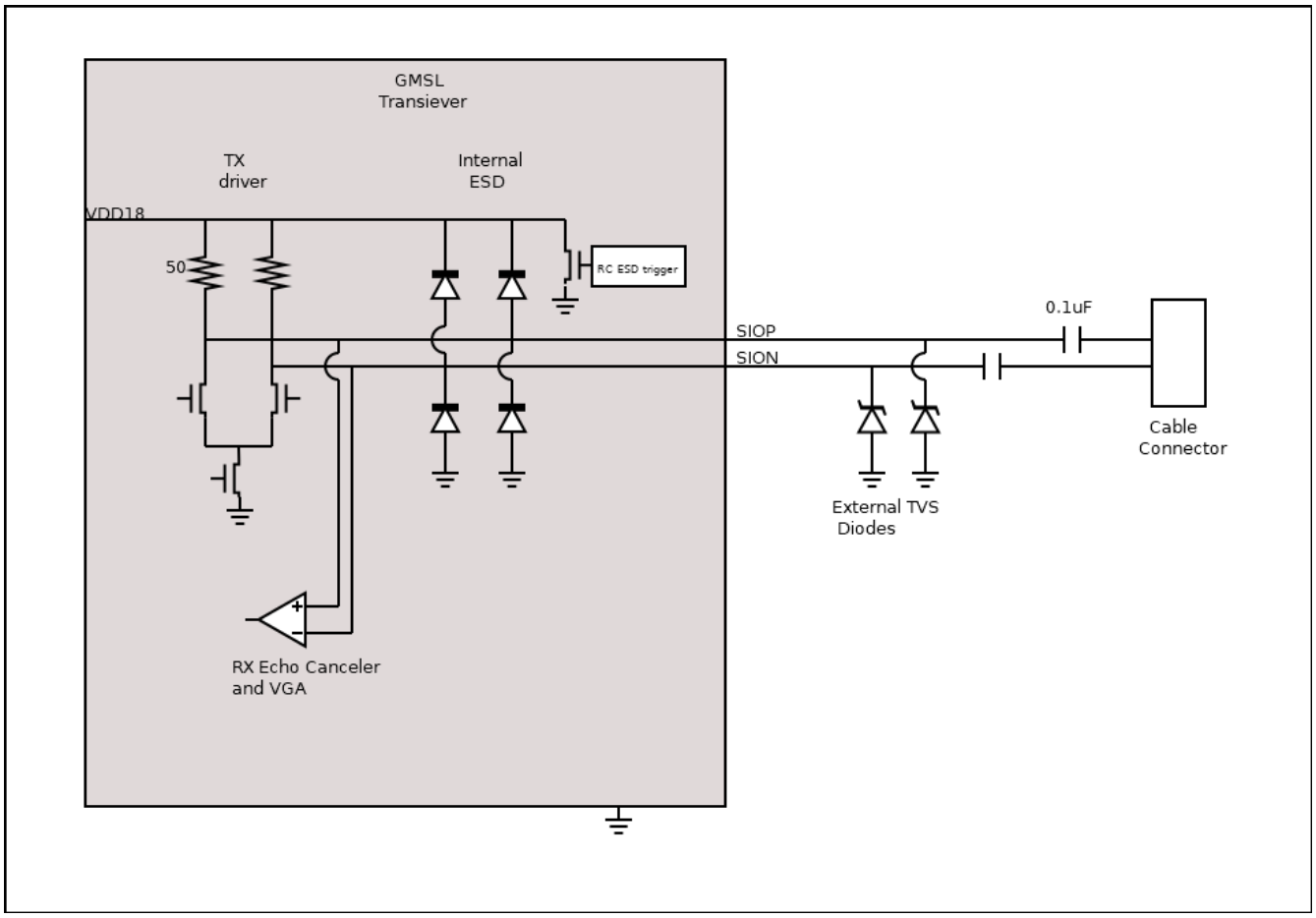


Figure 3.6.A: GMSL2 Serializer and Deserializer PHY Output Structure with ESD Devices

3.6.2 ISO 10605 ESD Standard

The system designer may choose to qualify their system by different ESD standards. Many different ESD specifications evolve from a baseline ESD specification, such as the ISO 10605. The Analog Devices current specifications system shows ESD passing levels using the ISO 10605 automotive test standard (https://www.iso.org/standard/41937.html).

Within the ISO 10605, many tests are outlined. Analog Devices primarily focuses on the component packaging and handling test method (unpowered test).

3.6.3 Test Setup

Within the ISO 10605 test standard, the unpowered test section outlines all details of the test, such as the required ESD RC networks, stress points, methods to access stress points, distances between test structures, GND connections, etc.

ESD Gun RC Network: 330Ω/150pF

Figure 3.6.D outlines a typical bench setup for an unpowered device ISO 10605 test. Figure 3.6.D shows a typical bench setup.

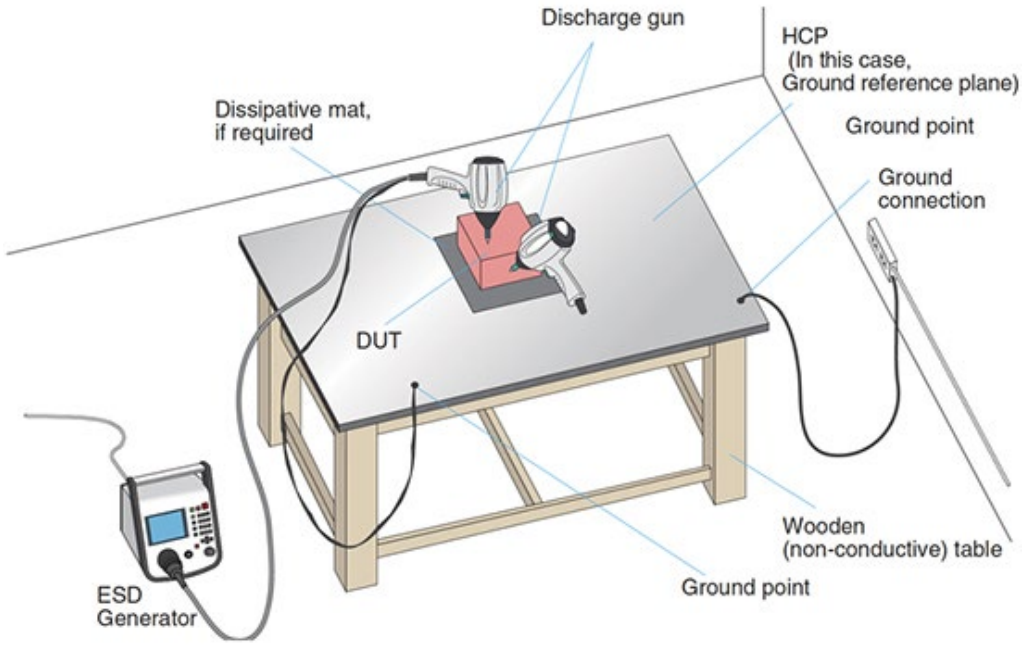


Figure 3.6.B. Typical Setup for Unpowered ISO 10605 Test

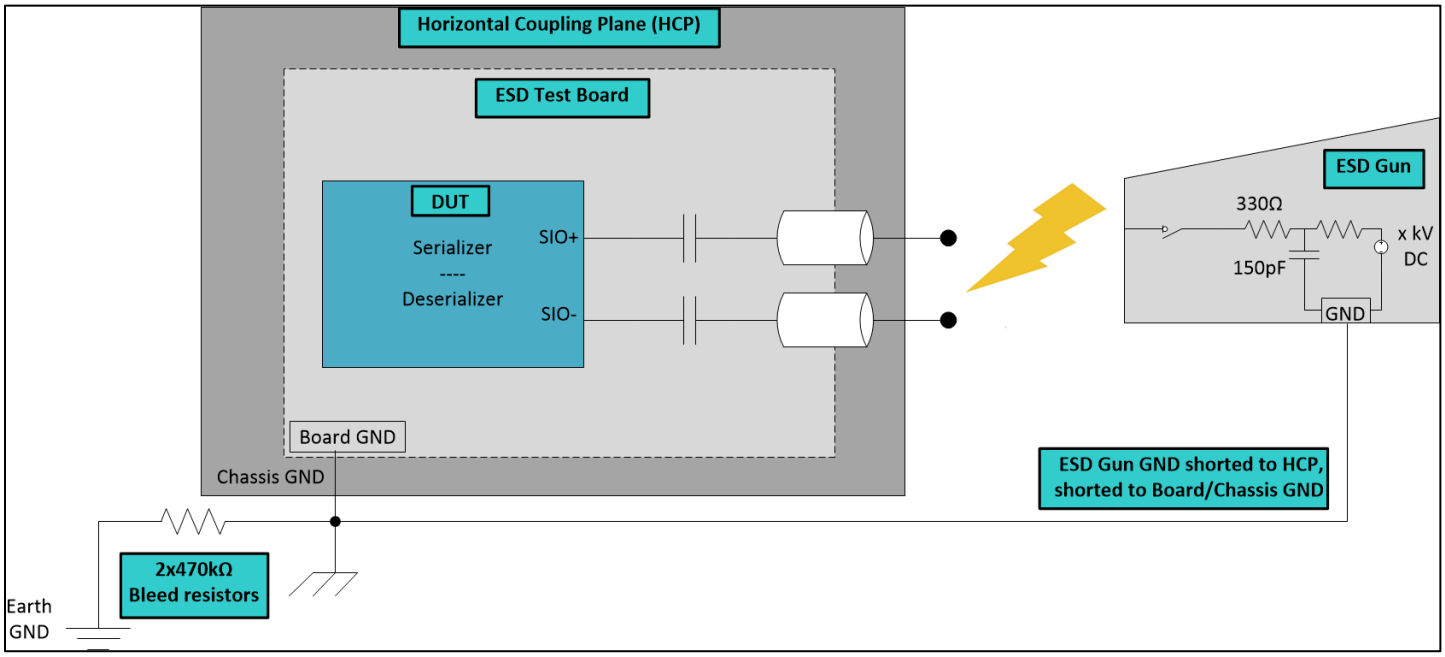


Figure 3.6.C. Setup for Unpowered ISO10605 Test

3.6.4 External Components

Analog Devices's proprietary GMSL2 serial link is a robust gateway built to efficiently transmit and receive video data, control data, peripheral data, and any other supported interfaces. Considering the high-speed bidirectional nature of the serial link, the system designer must delicately balance their requirements of ESD protection to desired link performance.

Analog Devices's GMSL2 device data sheets specify nominal ESD passing levels without additional external ESD protection. If the system designer requires better ESD protection, external transient voltage suppression (TVS) diodes can be used to sacrifice slight link performance for vastly improved ESD passing levels.

Ideal external TVS diodes should have the following properties:

- Capacitance of <0.5pF or less to prevent degradation of high-speed GMSL2 signal
- Small package footprint to minimize capacitance
- Low breakdown voltage and low clamping voltage
- Unidirectional, reverse-biased onto the link
- Two-port component to minimize lane-lane crosstalk

The external TVS is required to have less than 10V breakdown/clamping voltage due to the internal structure of the ESD diodes. If the external TVS diodes have greater than 10V breakdown/clamping voltage, during an ESD event, the internal diodes may conduct first and damage the internal circuitry before the external diodes can assist with diverting the high currents.

Unidirectional TVS diodes should be used. External bidirectional diodes are not recommended due to the internal structure of the SerDes ESD protection. While the bidirectional diodes may help with the positive polarity ESD events, most often the protection in the negative polarity does not become active before damaging the internal driver.

3.6.4.1 Diode Placement by Use Case

For customers utilizing line fault or power-over-cable GMSL2 features, it is recommended to place the unidirectional TVS diode on the chip-side of the AC series coupling capacitor.

*Note: Line fault cannot be used simultaneously with PoC in GMSL2 applications.

The PoC cannot be used in conjunction with TVS diodes placed on the connector side. For a stable system using PoC with a TVS diode on the serial link, the diode must have a higher breakdown voltage than the PoC voltage. In a typical 12V PoC system, if the diode has a 13V breakdown voltage, an ESD event damages the internal circuitries of the SerDes devices before the external diode can conduct. With the diode on the chip-side, there is no relation between the PoC and diode breakdown voltage as the AC coupling capacitor protects the diode from the DC voltage.

A line fault short-to-battery condition may damage the TVS diode depending on the duration of the event. A typical ESD event is on the order of microseconds, but depending on the line fault, the external diode might be damaged unless it is protected by the AC coupling capacitor.

Placing the TVS diodes on the chip-side of the AC series coupling capacitor can allow PoC or line fault to be used in a SerDes system.

See Figure 3.6.F for example of placement when using either line fault or PoC.

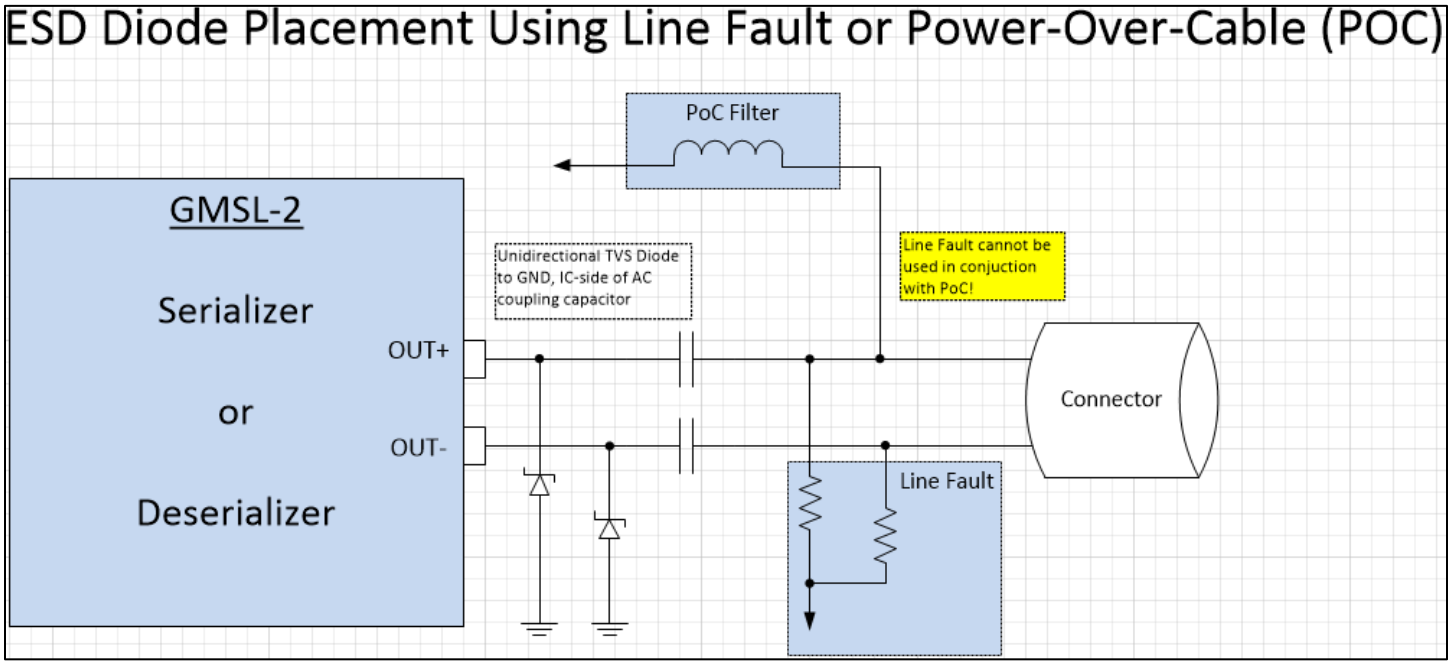


Figure 3.6.D. Recommended ESD Placement with LF or PoC

For customers not using line fault or PoC, ESD placement follows standard practice by placing the component closest to the connector, where the ESD discharge event is most likely to originate from. See Figure 3.6.G.

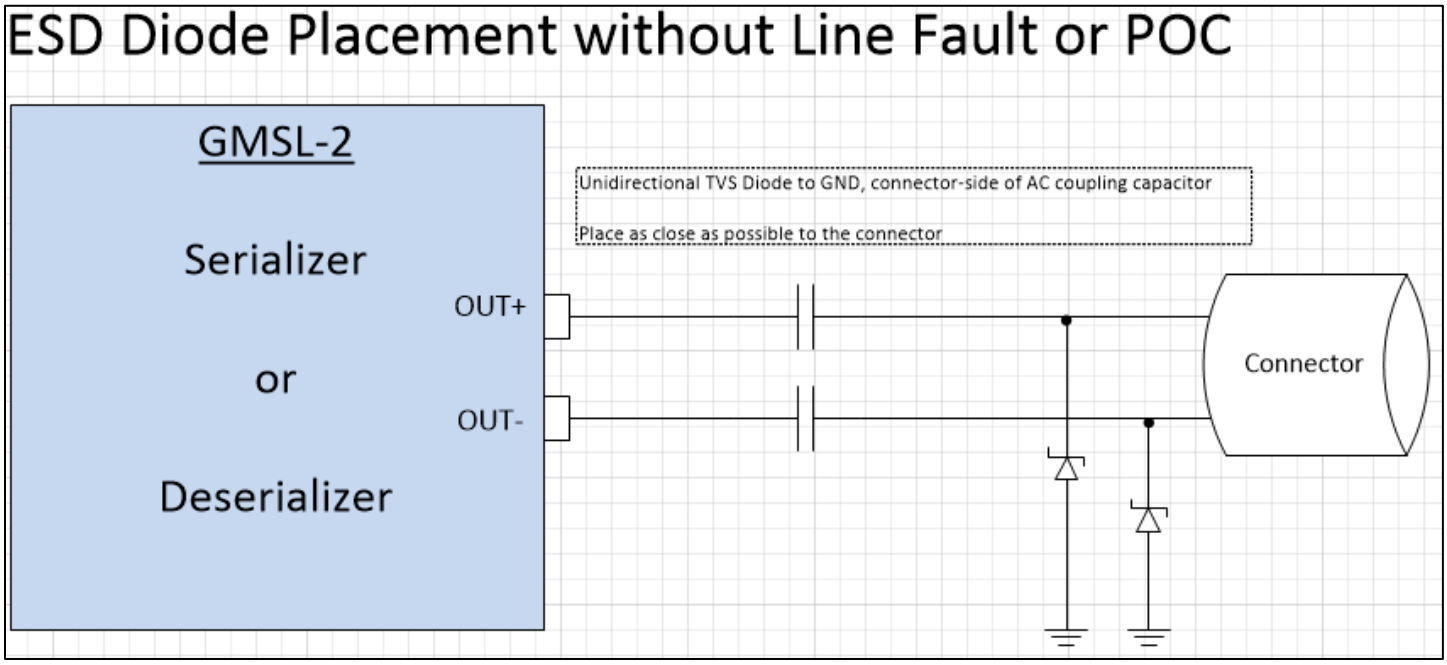


Figure 3.6.E. Recommended ESD Placement Without LF or PoC

3.6.4.2 External Component Layout

The ESD device should be placed directly onto the serial link trace. There should be no stubs from the serial link trace to any component on the net. A 1.35x GND cutout should be implemented on the pad of the ESD diode. The GND path of the ESD diode should be a low-resistance, large plane, with embedded vias for best ESD performance. See Figure 3.6.H for example of this implementation.

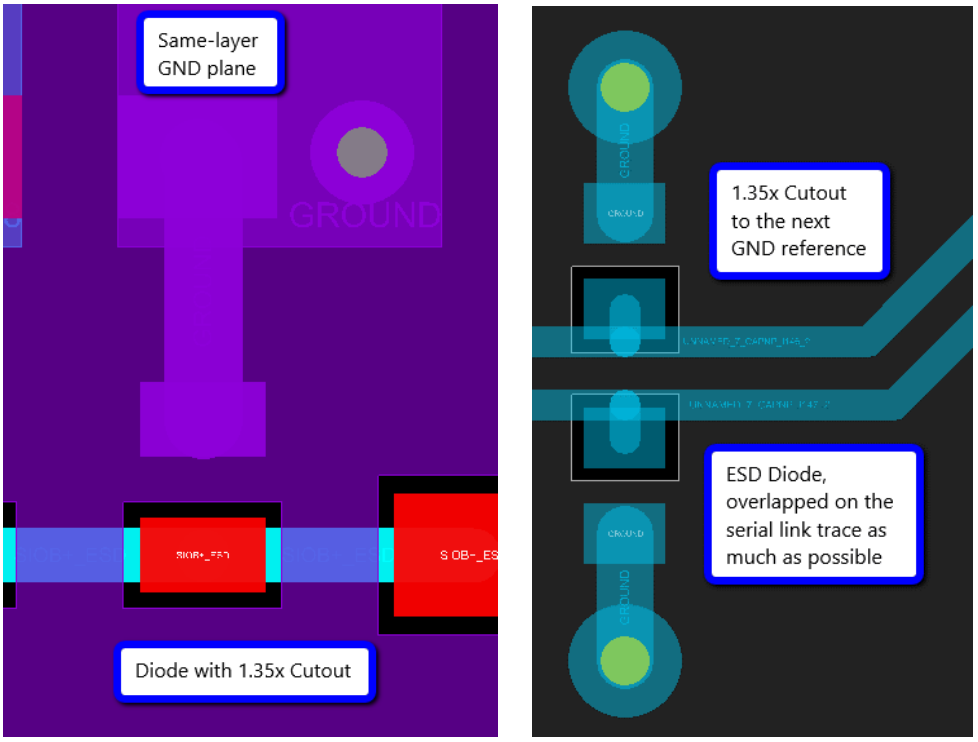


Figure 3.6.F. Layout Placement with Cutout Example

Analog Devices has evaluated various diodes in different configurations and can offer basic recommendations as seen below. The ESD passing levels may differ between different devices, board setup, diode location, and natural variations of all factors in the ESD test setup.

*Note: Analog Devices does not guarantee passing levels for these devices.

See Table 6 for part numbers, passing levels, and notes.

Table 6: External ESD Components

MFG	Part Number	Automotive Qualified	ESD Passing Level Contact/Air	Tested	Note
Littelfuse	**SESD0201X1UN	Yes	>8kV/15kV	Yes	0201 package, 2-pin device
Littelfuse	**SESD0402X1UN	Yes	>8kV/15kV	Yes	0402, larger package than above
ON Semi	ESD7004MUTAG	No	>8kV/15kV	Yes	10-pin device
ON Semi	SZESD7004MUTAG	Yes	--	No	Automotive-qualified version of above, results should be similar
ON Semi	**SZESD9101P2T5G	Yes	>8kV/15kV	Yes	2-pin device

*Analog Devices does not guarantee passing levels for these devices.

**Recommended based on ideal qualities mentioned above.

3.6.5 General Considerations

The ESD events impose high-current situations into operating systems. Whether it is powered or unpowered, ESD can severely damage electronics in a system, and cause functions and features to no longer operate as expected.

The ESD current takes the path of least resistance. The goal of ESD protection is to direct the high instantaneous current into the ESD protection devices instead of the functional electrical devices. Thus, to provide proper transient suppression, system designers should consider the path that a potential ESD strike may take. Creating a low-impedance path through ESD protection devices to ground is largely dictated by board layout and component selections along the ESD path.

The TVS diode placement is a significant factor in ESD protection for GMSL2. Analog Devices recommends setting the device in reverse bias configuration on the IC side of the serial link AC capacitor for benefits such as allowing PoC or line fault monitoring to function simultaneously. The pad of the diode should be set directly onto the serial link to avoid stubs.

In general:

- The IC-to-be-protected should be as far away as possible from the potential ESD event.
- Avoid stubs on the signal path of the TVS.
- Minimize inductances between the TVS and ground.
- Diodes should connect directly to the ground plane.
- If placing the TVS on the connector side of the serial link, place TVS as close as possible to connector.

3.6.6 Summary

The ESD Guide section covers information to establish a robust GMSL2 link with improved ESD protection. The design guide is not all inclusive and is subject to change at any time without notice. For certain applications/features, Analog Devices has specific application notes which address other topics. Certain design recommendations in this guide are based specifically on GMSL2 links. For other questions regarding ESD, please contact Analog Devices Support.

4. Hardware Validation Tools

The GMSL2 includes on-chip signal integrity tools to assess the quality of the GMSL2 link. These tools are available through the Analog Devices GMSL GUI. Alternatively, software support is available for customers who wish to develop their own implementation of these tools in their software. This section begins with a summary of typical results from the tools and then explains each tool in detail.

Table 7. GMSL2 Signal Integrity Tools

Tool	Description
Link Margin	Reduces the transmit amplitude until errors are detected, for both the forward and reverse channels. Indicates the voltage margin of the transmitted signal.
Eye Mapper	Uses the Eye-Opening Monitor (EOM) as an on-chip oscilloscope to display the equalized received signal along with displaying the equalizer coefficients being used.
Forward Error Correction (FEC)	Reports FEC input and output BER, including number of blocks processed and number of bits corrected. Only available on GMSL2 products which support FEC.

4.1 Forward Channel Typical Performance

Typical performance data is provided as a reference to compare to systems under development. Systems that fall within these ranges under nominal conditions are operating as expected. The GMSL2 signal integrity tools allow the user to measure each of these parameters for their system.

Typical operating performance is measured for short (0.9m), medium (7m), and long (15.5m) Coax cables (Leoni Dacar 302 cable with Rosenburger Fakra edge-launch connectors), with insertion loss as shown below.

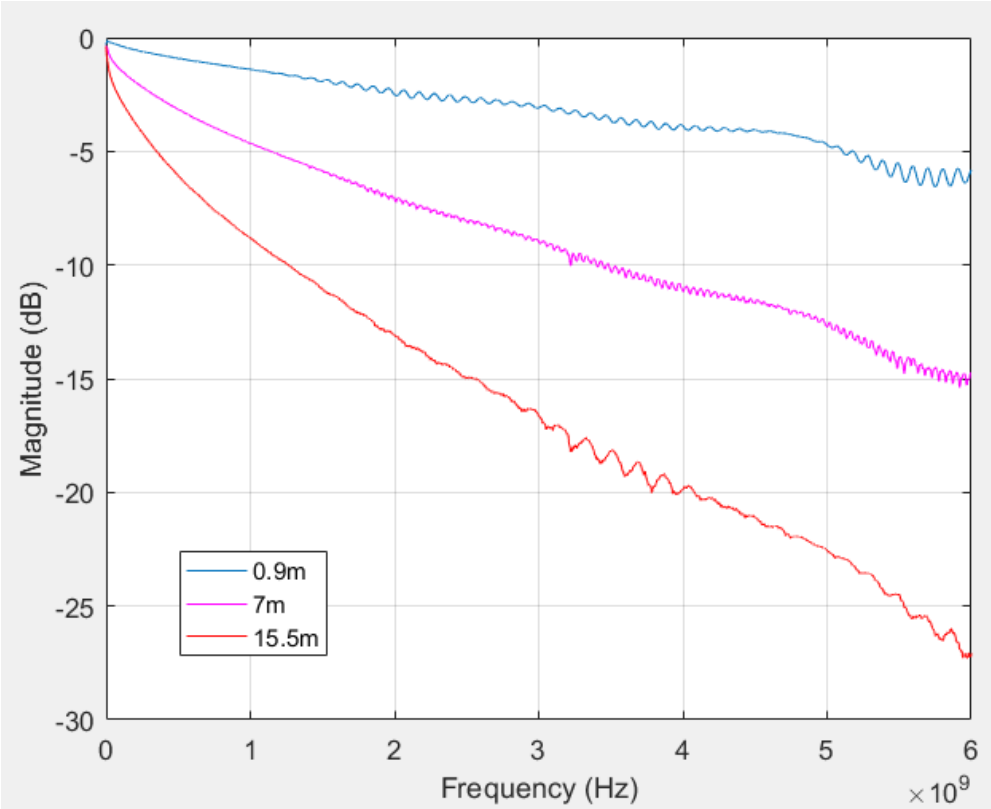


Figure 4.1.A. Insertion Loss of Test Channels

Table 8. Typical Forward Channel Performance

Forward Channel Typical Performance 3GBPS								
Typical Conditions: 25C; Nominal Supplies				3Gbps/187M NRZ				
Coax Length (m) (Note 1)	S21 1.5GHz/3GHz (dB) (Note 2)	Clock	POC (Y/N) (Note 3)	Link Margin (mV) (Note 5)	Boost (Note 4)	Eye Width (UI) (Note 6)	Eye Height (mV) (Note 6)	FEC Input BER
0.9	-1.9/-3.0	XTAL	N	345 to 365	2 to 6	0.7 to 0.85	130 to 175	< 1e-12
7	-5.9/-8.9	XTAL	N	330 to 360	7 to 13	0.7 to 0.85	120 to 180	
		ROR	N	330 to 355		0.7 to 0.85	120 to 180	
		XTAL	Y	330 to 355		0.7 to 0.8	120 to 160	
15.5	-11.1/-16.6	XTAL	N	270 to 345	11 to 19	0.65 to 0.8	110 to 155	
Forward Channel Typical Performance 6GBPS								
Typical Conditions: 25C; Nominal Supplies				6Gbps/187M NRZ				
Coax Length (m) (Note 1)	S21 1.5GHz/3GHz (dB) (Note 2)	Clock	POC (Y/N) (Note 3)	Link Margin (mV) (Note 5)	Boost (Note 4)	Eye Width (UI) (Note 6)	Eye Height (mV) (Note 6)	FEC Input BER
0.9	-1.9/-3.0	XTAL	N	345 to 365	0 to 3	0.35 to 0.5	95 to 170	< 1e-12
7	-5.9/-8.9	XTAL	N	315 to 355	6 to 10	0.35 to 0.5	95 to 155	
		ROR	N	315 to 355		0.35 to 0.5	85 to 145	
		XTAL	Y	290 to 350		0.35 to 0.45	80 to 130	
15.5	-11.1/-16.6	XTAL	N	250 to 315	13 to 18	0.25 to 0.45	65 to 115	

Note 1: The 7m cable comprises 5m and 2m sections. The 15.5m cable comprises 10m, 5m, and 0.5m sections. STP performance is similar to coax performance and can be estimated by comparing S21 to the cases shown.
Note 2: Insertion loss includes the cable, interconnects, and PCB traces on the serializer and deserializer boards.
Note 3: The power over coax filter designation used is "RC - Remote Camera", described in the 3.5 Power-over-Coax (PoC) section of this document.
Note 4: Boost is a receiver equalizer coefficient indicating the amount of peaking being used. It is automatically adapted and ranges from 0 (minimum boost) to 32 (maximum boost). It is displayed as "BST" in the Eye Mapper Tool.
Note 5: Link Margin (LM) is the difference between the default transmitter amplitude and the reduced amplitude at which errors are detected. Larger numbers indicate more margin.
Note 6: Values are at BER = 1e-12, extrapolated from measured BER trajectory. For 6Gbps, eye width is guardbanded for tool accuracy.

4.2 Link Margin Tool

The link margin tool allows quantitative testing of the noise quality of the GMSL2 link. The link margin test starts at the default transmit voltage amplitude for the forward channel and reverse channel. The test decreases the transmit amplitude in 10mV steps, and at each step it performs an error check before proceeding to the next amplitude. When errors are detected, the test is over. Link margin is reported as the difference between the default transmitter amplitude and the amplitude at which an error was detected. The test can be performed for both forward and reverse channels.

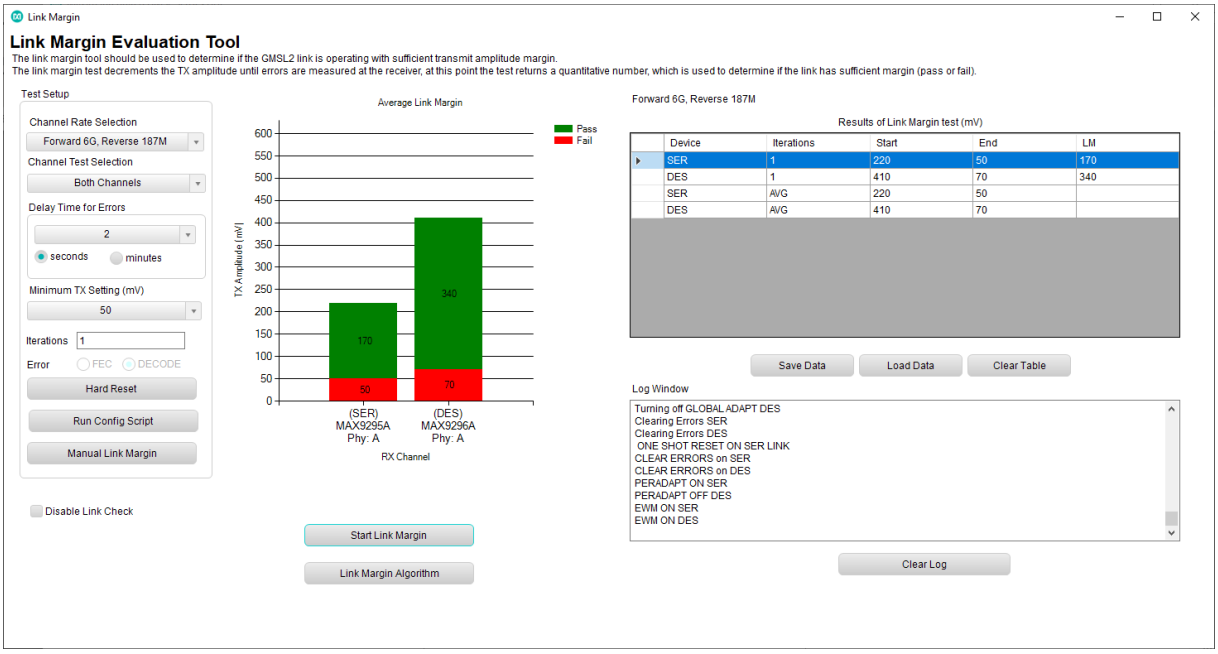


Figure 4.2.A: Link Margin Test (Reverse Channel 170mV Margin, Forward Channel 340mV Margin)

4.3 Eye Mapper Tool

The Eye Mapper Tool uses the on-chip EOM to generate an eye diagram of the equalized received signal. It functions as an on-chip oscilloscope to display the recovered signal and displays the equalizer coefficients being used. The equalizer automatically adjusts to compensate for loss in the channel and ensures best possible BER.

4.3.1 Eye Map Description

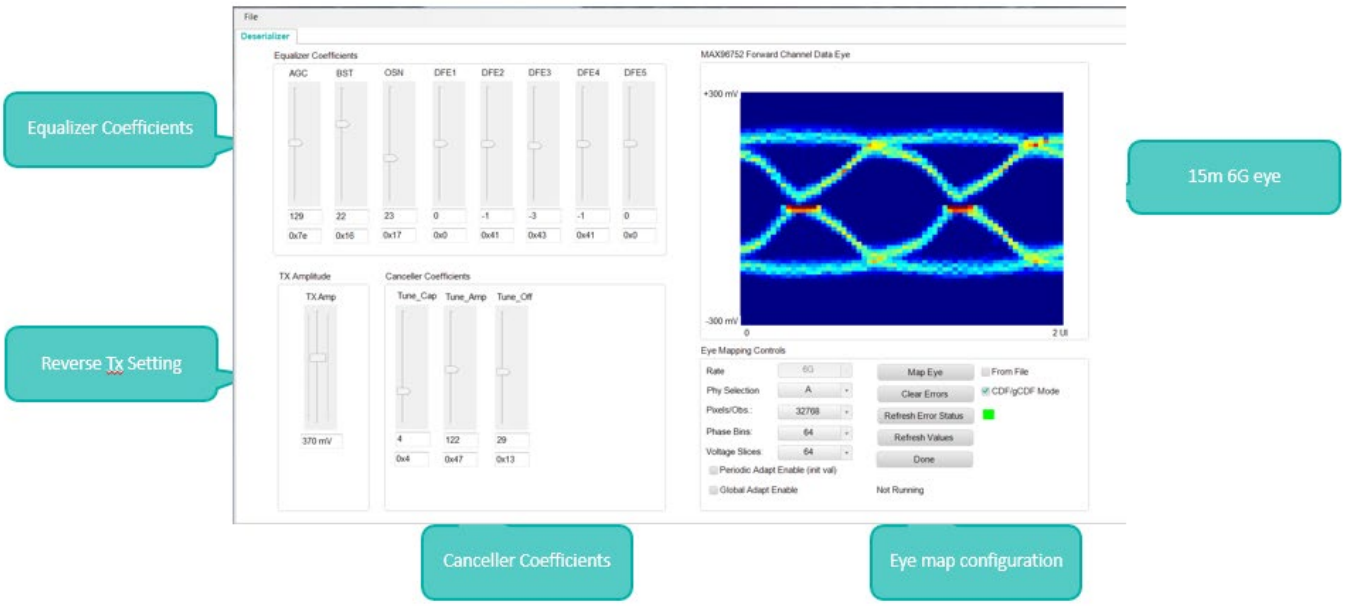


Figure 4.3.A: Eye Mapper Tool in GMSL GUI, 6Gbps Forward

4.3.2 Typical Forward Channel Eye Maps

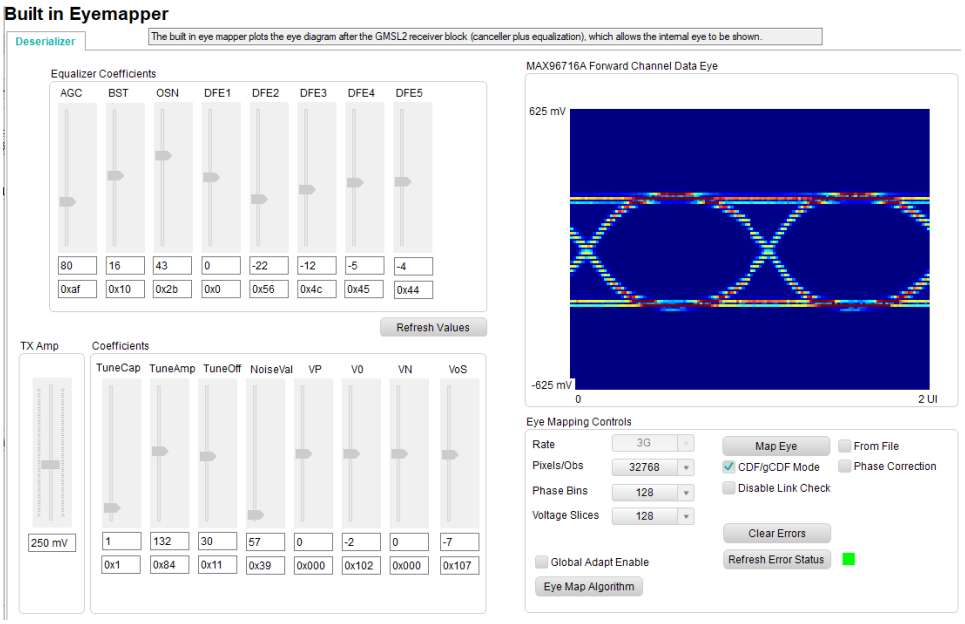


Figure 4.3.B. 15.5m Coax Typical 3Gbps Eye XTAL No PoC

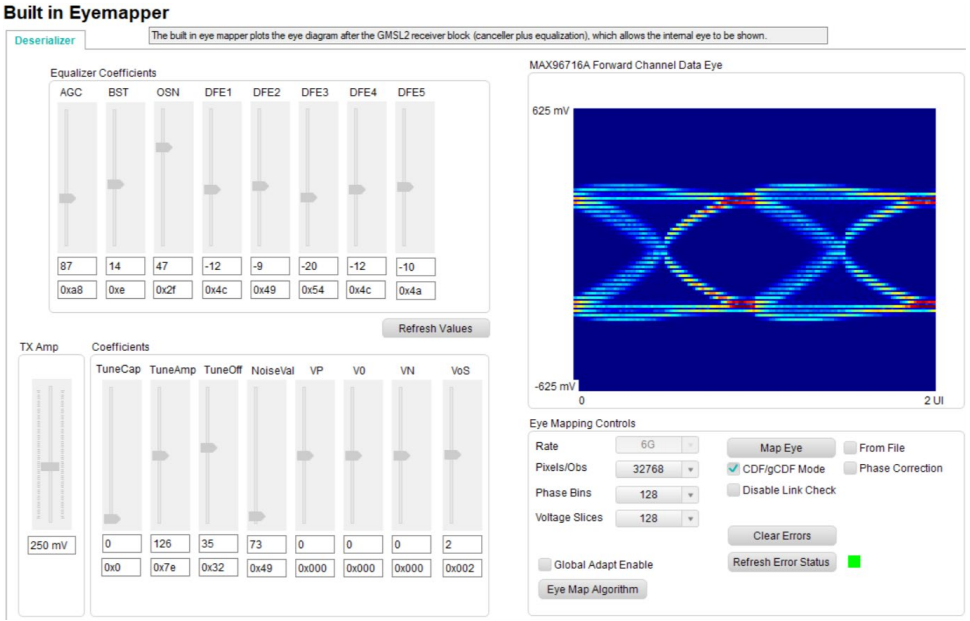


Figure 4.3.C. 15.5m Coax Typical 6Gbps Eye XTAL No PoC

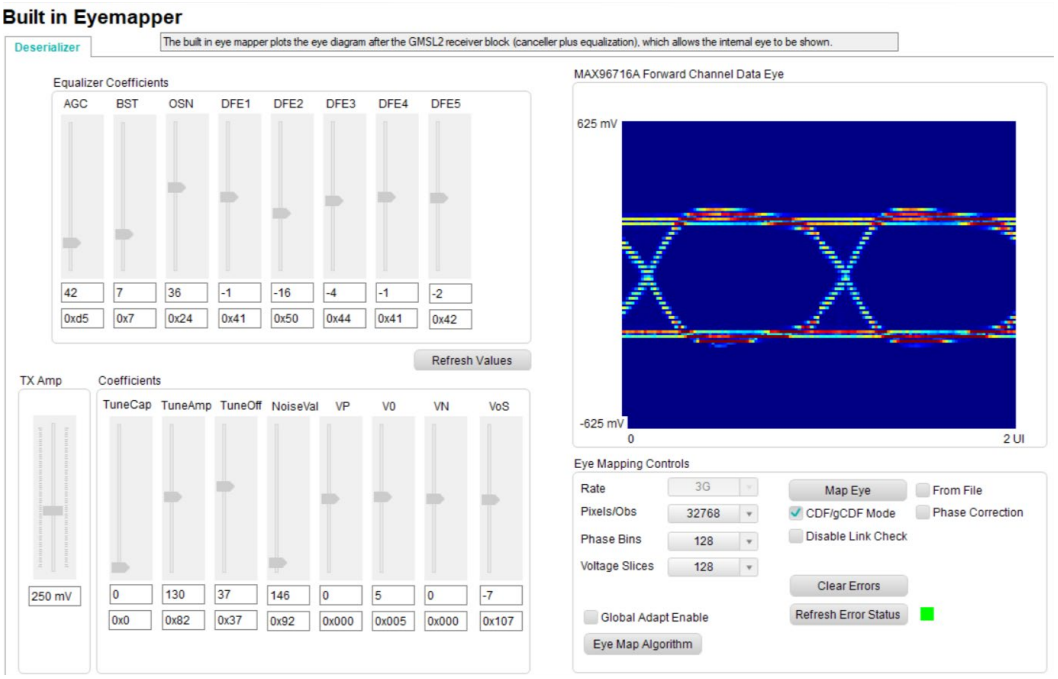


Figure 4.3.D. 7m Coax Typical 3Gbps Eye XTAL No PoC

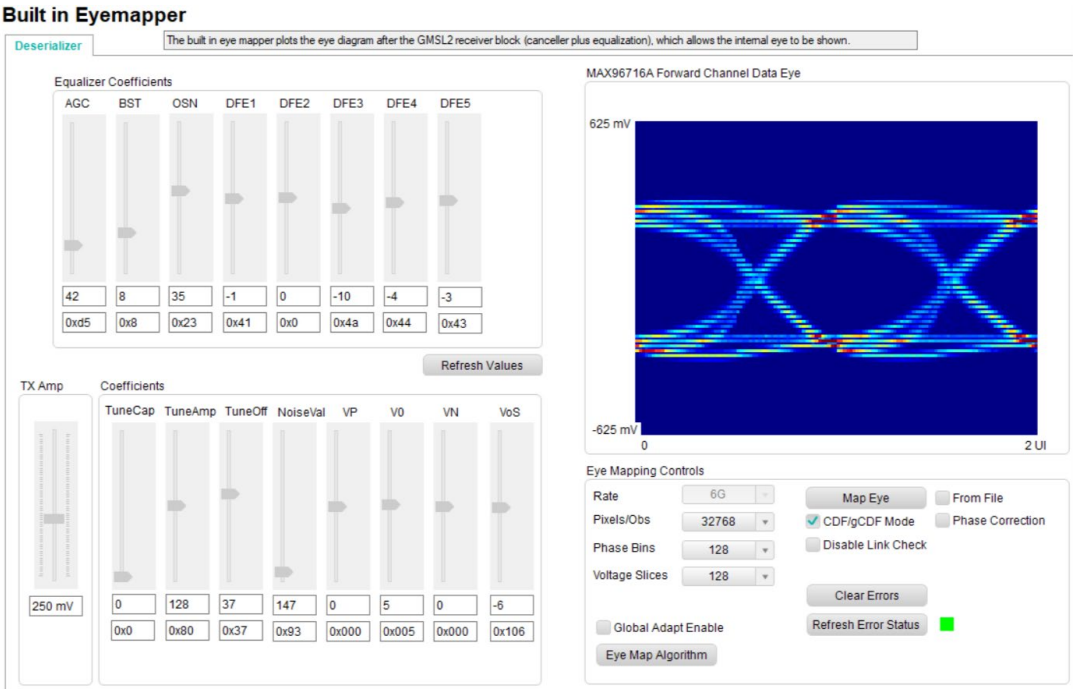


Figure 4.3.E. 7m Coax Typical 6Gbps Eye XTAL No PoC

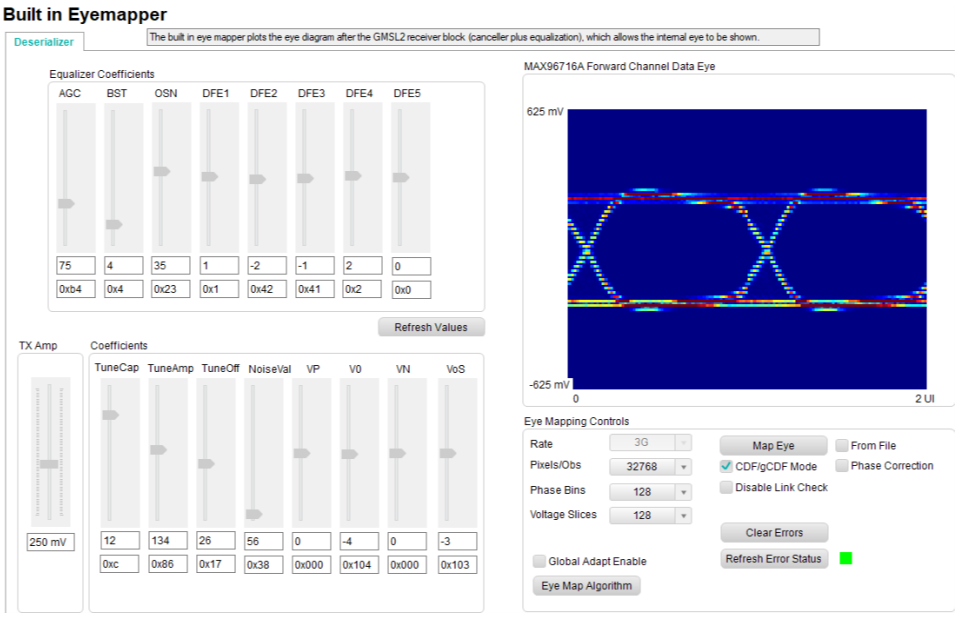


Figure 4.3.F. 0.9m Coax Typical 3Gbps Eye XTAL No PoC

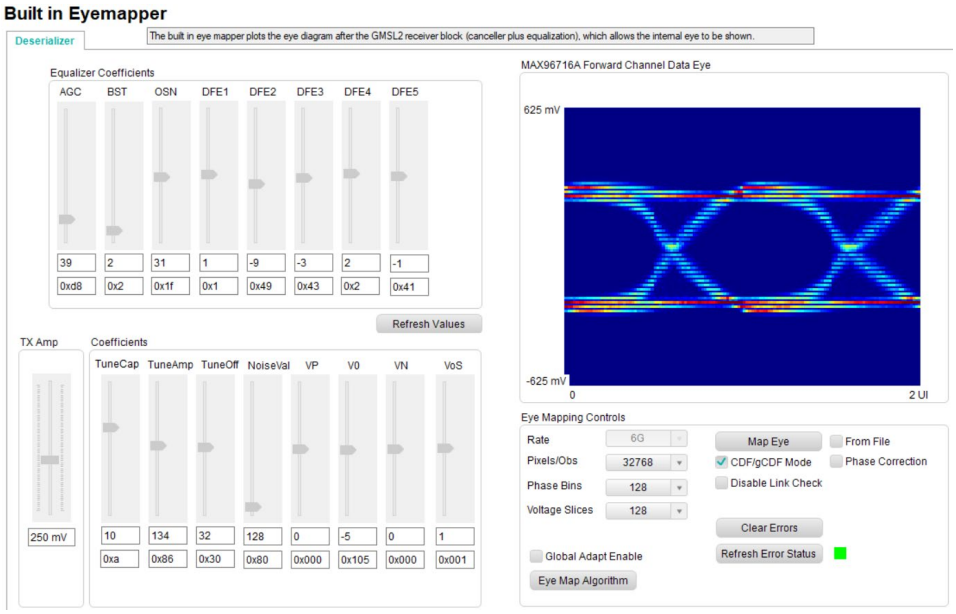


Figure 4.3.G. 0.9m Coax Typical 6Gbps Eye XTAL No PoC

4.4 Forward-Error Correction Statistics

The FEC is available on some Analog Devices serializers and deserializers. The GMSL GUI reports the FEC status,
including:

- Number of blocks processed,
- Number of bits corrected,
- Number of blocks uncorrected,
- Decode Errors,
- Idle Errors,
- FEC input BER,
- FEC Input BER @ 95% Confidence Level, and
- FEC output BER.

Expected FEC input BER is zero in all GMSL2 modes, and thus, enabling FEC is optional in GMSL2 mode. The FEC output BER of zero is required for error-free data transmission. The reported FEC input BER confidence level improves with longer observation times.

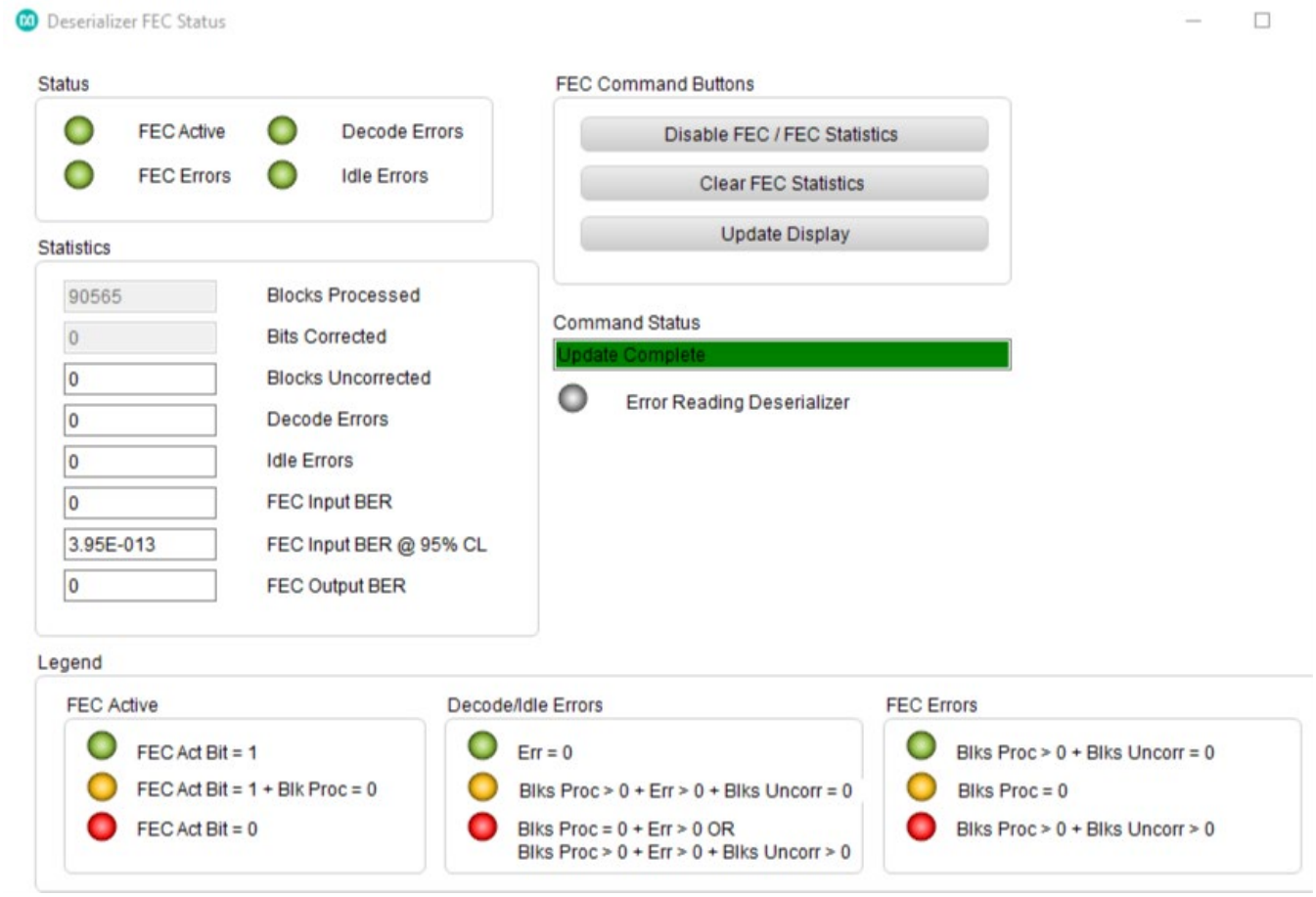


Figure 4.4.A. FEC Status 6Gbps/187 15.5m Typical; XTAL No PoC

4.5 TDR Measurements

While the return loss looks at the impedance matching in the frequency domain, the Time-Domain-Reflectometer (TDR) can evaluate the impedance matching in the time domain. The TDR is a useful tool to evaluate impedance matching and determine the location of board layout issues.

- TDR: sends out a reflected pulse to measure matching and faults in transmission line
- Y-axis: impedance, x-axis: time (and thus position)
- Pulse rise time determines the frequency (and thus resolution)
- Rule of thumb: $Bandwidth = \frac{0.35}{Rise\ time}$

Analog Devices recommends to use a TDR rise time of 100ps, which following the approximation equation above, corresponds to 3.5GHz bandwidth – the upper bandwidth limit of the GMSL2 channel specification. A faster rise-time setting (between 20ps and 50ps) may also be useful to more precisely isolate the location of impedance discontinuities. Slower rise times are less useful as they can mask potential discontinuities that negatively affect GMSL2 channel performance.

Analog Devices's TDR recommendation for GMSL2 is +/- 10% impedance matching (between 45Ω and 55Ω single-ended or 90Ω and 110Ω differential) with a 100ps rise time (10% to90%) setting on the TDR. This is not a specification but is a strong recommendation to ensure that the GMSL2 channel specification IRR and return loss requirements are met.

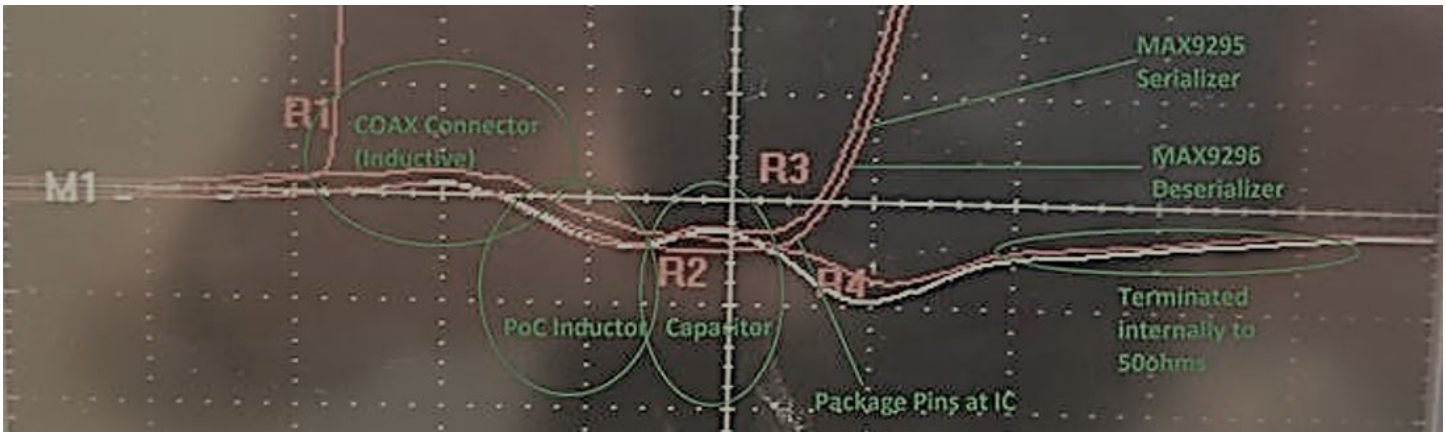


Figure 4.5.A: Example TDR of a PCB that Pass Channel Specifications. This is a Single-Ended Measurement (Coax System) with Rise Time = 100ps, x-axis scale = 200ps/div, y-axis scale = 5Ω/div Centered Around 50Ω

The PCB parasitic inductance increases the magnitude of the impedance while parasitic capacitance lowers the magnitude of the impedance. Using a simulator (such as HFSS), the PCB parasitic can be estimated and layout optimized. For example, Analog Devices uses a 1.35x GND cutout underneath all component pads on the high-speed trace, which offsets the capacitance added by the pads of the components on the high-speed trace, for the PCB stackup used on Analog Devices EV kits. The size of the cutout needed (or the number of layers to cut out) varies with different board stackups and materials.

5. Appendix A: GMSL2 Channel Measurement Guidelines

1. Purpose and Scope

The GMSL2 Channel Specification shows example methods to measure the S-parameters and Crosstalk of a GMSL2 system to compare against the GMSL2 channel specifications.

2. GMSL2 System Channel Specification Measurements

Measurements should be taken with a real system at worst-case conditions to verify that designs are built to specification.

2.1 GMSL2 Pin-to-Pin Channel Measurements

The forward channel is defined as serializer-to-deserializer transmission; the reverse channel is defined as deserializer-to-serializer transmission.

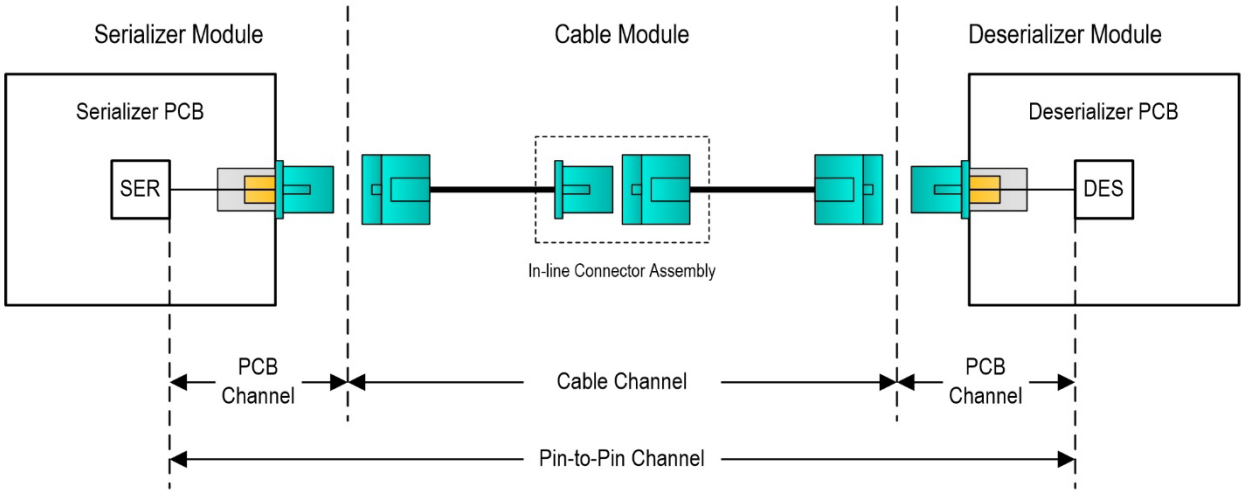


Figure 2.A. GMSL2 Channel Definition

*Note: AC-coupling capacitors and optional PPoC or line-fault components are not depicted in Figure 2.A.

*Note: The PCB and Cable Channels comprising a compliant GMSL2 System Channel may not meet the standards required for GMSL2 Module Compliance. Modules must be independently evaluated for module compliance. See GMSL2 Channel Specifications section for additional information.

2.1.1 Measurements for Insertion Loss and Return Loss

Full two-port S-parameters should be taken from the serializer SIO_ pin to the deserializer SIO_ pin. Start with a Replica system consisting of the cable and two replica boards. Connect both ends to a Vector Network Analyzer (VNA). Coax systems should use a two-port VNA, while STP applications should use a four-port VNA. For Insertion Loss, select S_{21}/S_{DD21} and/or S_{12}/S_{DD12} depending on which direction you wish to measure. For Return Loss, select S_{11}/S_{DD11} and/or S_{22}/S_{DD22} depending on which port you wish to measure.

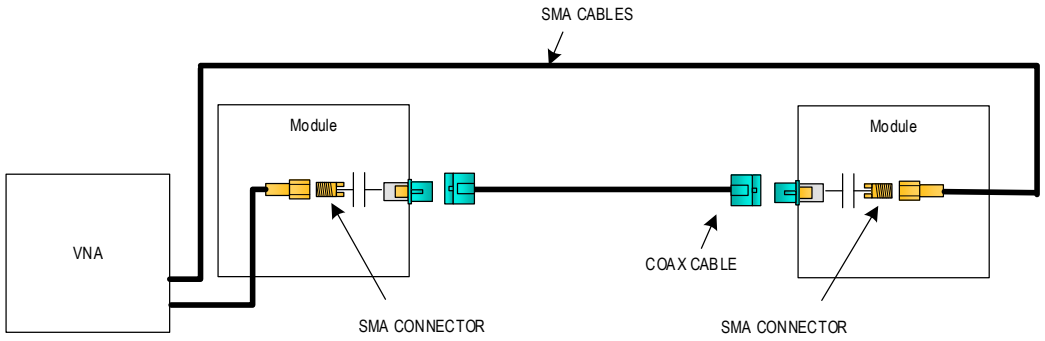


Figure 2.B. Coax 2-Port VNA Connection

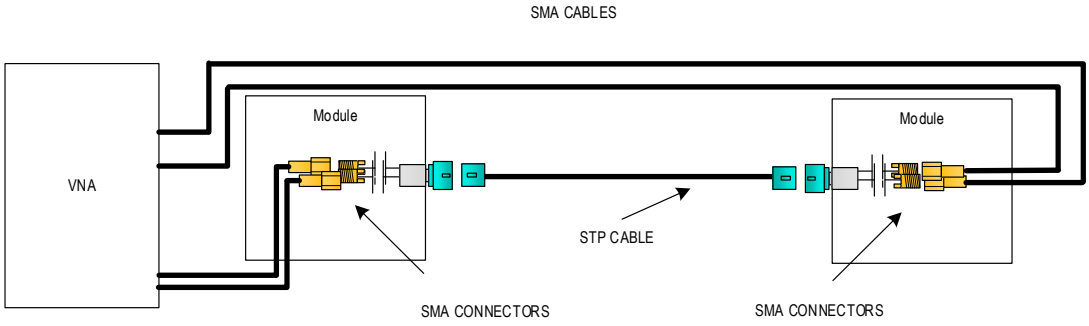


Figure 2.C. STP 4-Port VNA Connection

Set up the VNA with the following parameters:

- Start Frequency: Minimum of 2MHz or lower
- Stop Frequency: 10GHz
- Step size: 1MHz
- Sweep: Linear sweep
- Power Level: 0dBm

*Note: STP cables for differential measurements must be phased matched.

2.1.2 GMSL2 Crosstalk at Device Under Test (DUT)

Crosstalk is specified at a module level, reference module measurement guidelines below.

2.2 GMSL2 Channel Specifications

The GMSL2 Module Channels are defined as the individual subchannels within the GMS2L System Channel.

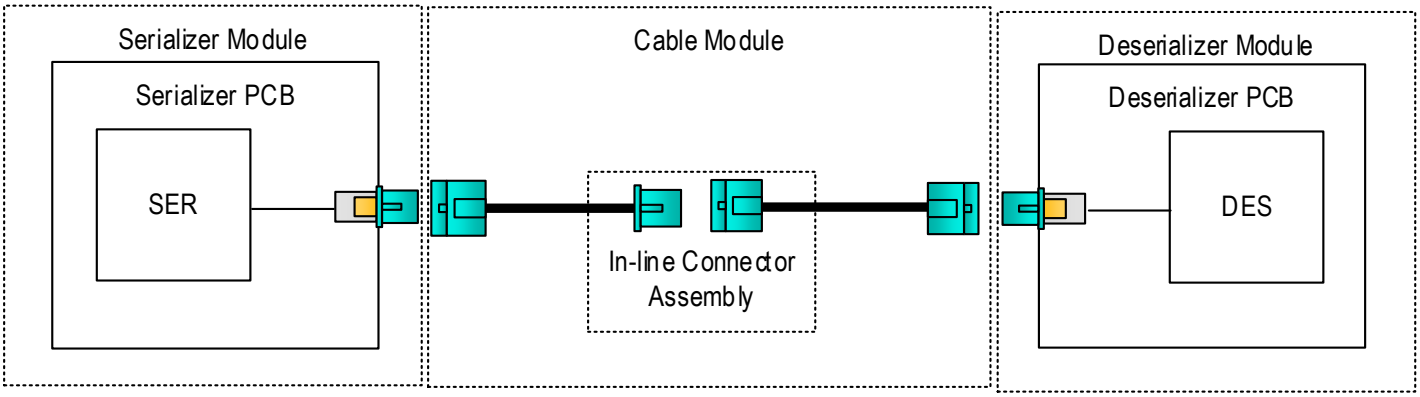


Figure 2.D. GMSL Module Channels

2.2.1 Measurements for Insertion and Return Loss (PCB Channel)

Using a replica/coupon board, connect the VNA to the SMA connector, and the GMSL2 Module connector through an adapter (contact the connector manufacturer regarding adapters). Ensure to calibrate out losses of the SMA cables and adapters.

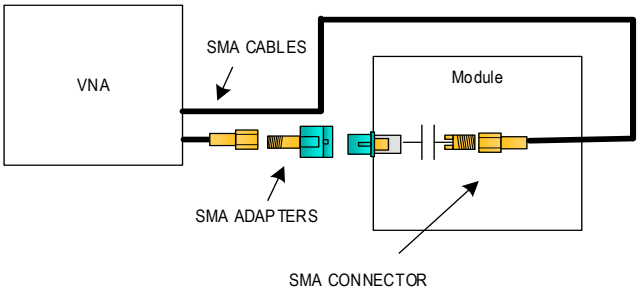


Figure 2.E. Coax VNA Connection

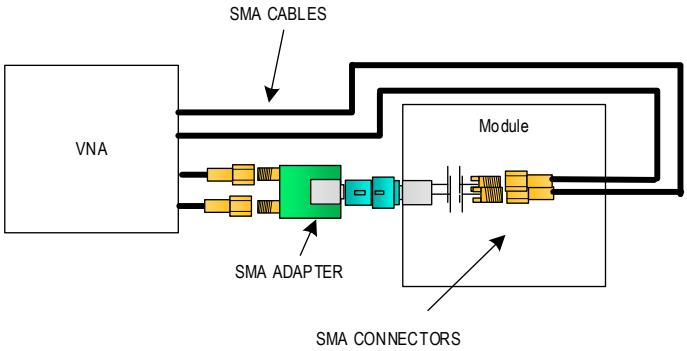


Figure 2.F. STP VNA Connection

Set up the VNA with the following parameters:

- Start Frequency: Minimum of 2MHz or lower
- Stop Frequency: 10GHz
- Step size: 1MHz
- Sweep: Linear sweep
- Power Level: 0dBm

2.2.2 Measurements for Insertion and Return Loss (Cable Channel)

Connect the Network Analyzer to both ends of the cable with adapters (if necessary).

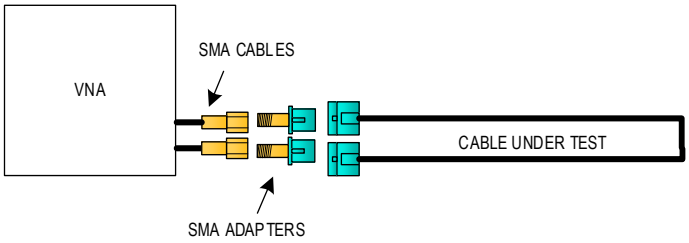


Figure 2.G. Coax VNA Connection

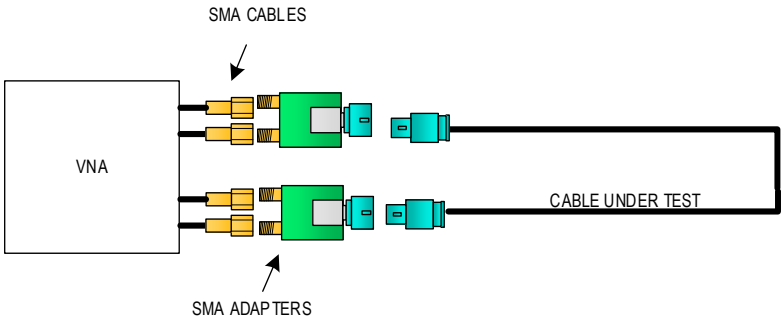


Figure 2.H. STP VNA Connection

Set up the VNA with the following parameters:

- Start Frequency: 100kHz or lower
- Stop Frequency: 10GHz
- Step size: 1MHz
- Sweep: Linear sweep
- Power Level: 0dBm

2.2.3 Measurements for Crosstalk (PCB Channel)

2.2.3.1 Crosstalk from GMSL2 or Other Broadband Signals

The setup shown in Figure 2.I and Figure *2.J* is used to measure crosstalk between the different ports (connectors) on a PCB. The data traffic causing interference is running on Ports 1..N, and crosstalk is measured on Port M of the PCB.

The worst-case crosstalk condition occurs with channels (Ports 1..N) with minimum insertion loss, this maximizes the received signal power on Port M. Crosstalk is measured as peak amplitude on Port M using an oscilloscope. The GMSL2 device on Port M should be configured in squelch mode (contact factory for instructions on how to enter squelch mode). Scopes with enough bandwidth (4Ghz min) generally have a low enough noise floor to not require additional gain stages. If a gain stage is needed, use a broadband, AC coupled, gain block to increase the noise signal to a measurable level. Gain should be high enough that the noise level falls within an acceptable input level for the scope.

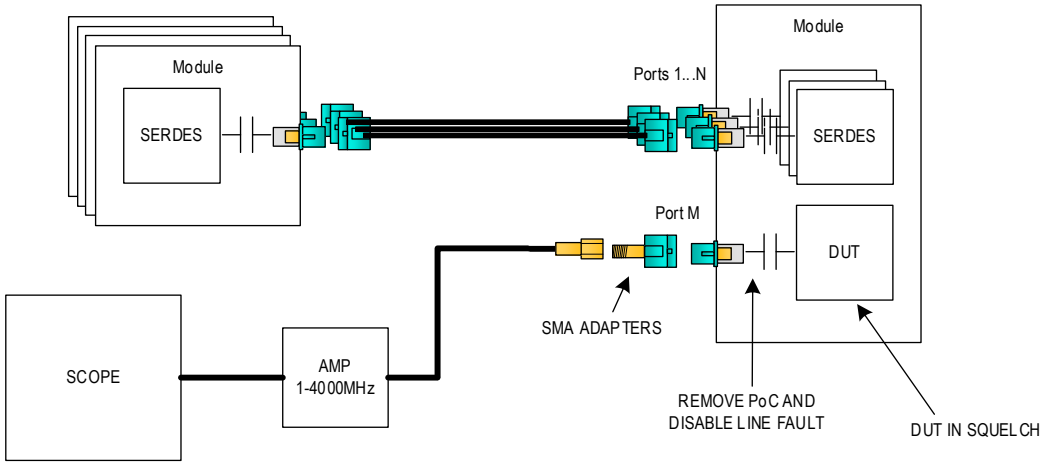


Figure 2.I. Broadband Crosstalk Characterization Method (Coax)

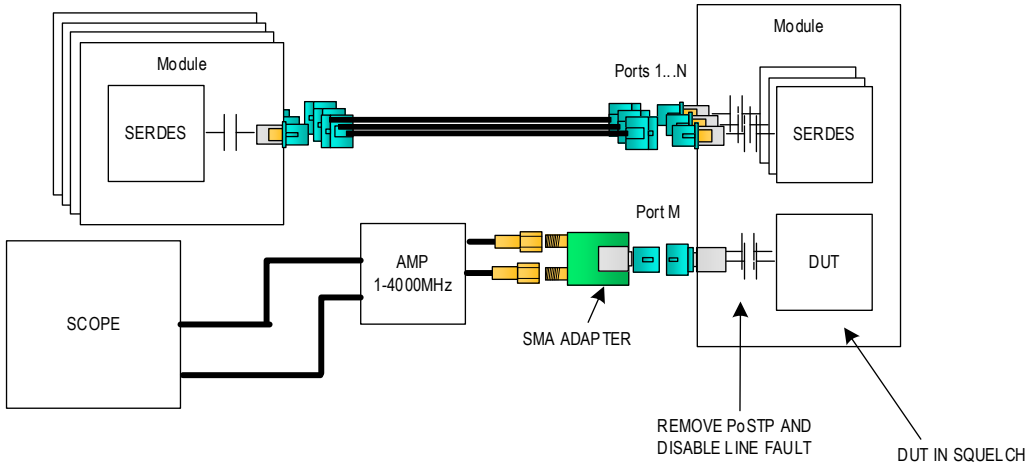


Figure 2.J. Broadband Crosstalk Characterization Method (STP)

*Note: Removal of PoC, PoSTP, and Line Fault may be required if equipment requires 0V DC inputs.

2.2.3.2 Crosstalk from Narrowband Signals

Connect the system as shown in Figure 2.K or Figure 2.L. The device under test is in squelch mode. All other links 1..N are operating normally. A spectrum analyzer separates out noise sources so you can measure the narrowband power of a single noise source. Measure the total power of the noise source (not just dBm level of the peak). Use a balun if measuring a twisted pair system to match the DUT with the analyzer input. Make sure to account for the balun's insertion loss. Alternatively, the noise level can be measured with an oscilloscope. In contrast to the broadband crosstalk measurement, a band-pass filter and a low noise amplifier is used to measure narrowband signals individually. The gain needs to be large enough that the noise can be measured by the scope. The filters need to be selective enough to isolate frequencies. These vary depending on the system, but in general, lab grade devices should suffice.

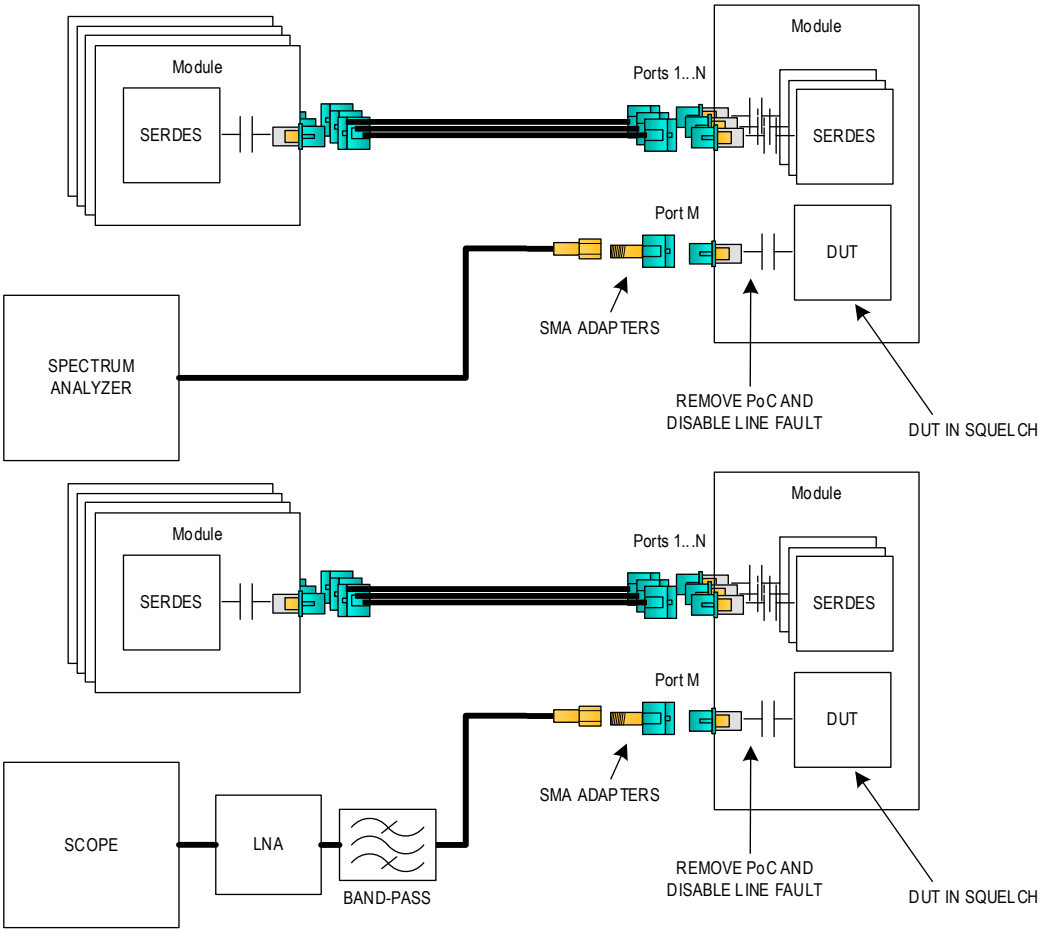


Figure 2.K. Measurement Setup for Narrowband Crosstalk (Coax)

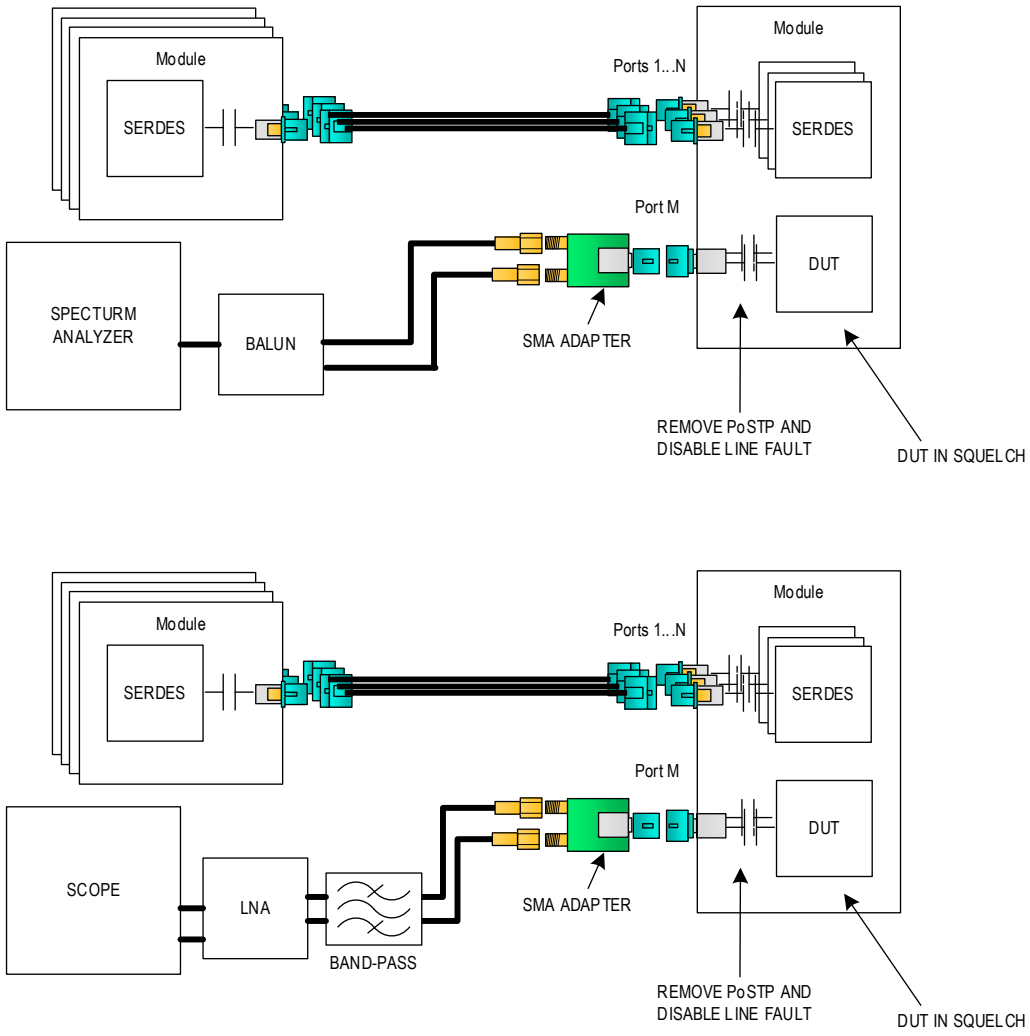


Figure 2.L. Measurement Setup for Narrowband Crosstalk (STP)

*Note: Removal of PoC, PoSTP, and Line Fault may be required if equipment requires 0V DC inputs.

2.2.4 Measurements for Crosstalk (Cable Bundles)

2.2.4.1 Near-End Cable Bundle Crosstalk

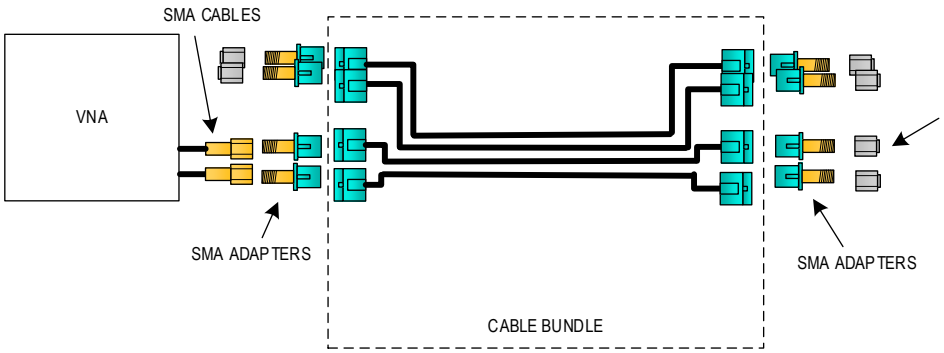


Figure 2.M. Near-End Crosstalk (NEXT) Coax

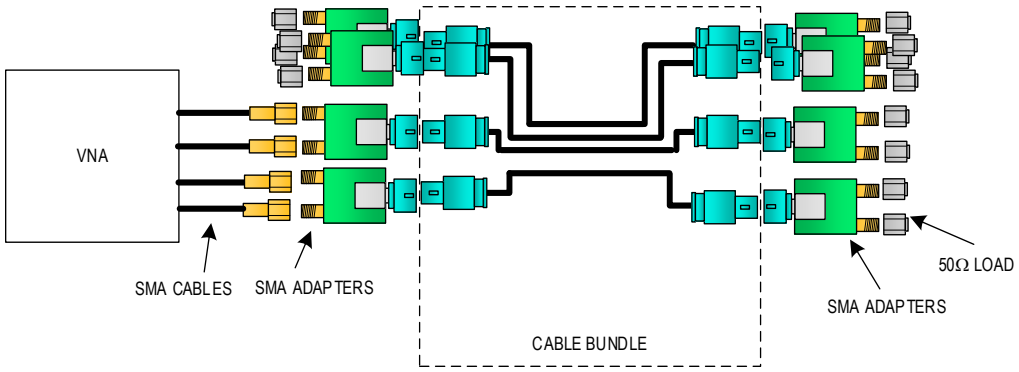


Figure 2.N. Near-End Crosstalk (NEXT) STP

The near-end crosstalk is usually dominant. NEXT is based on the injection and measurement ports shown in Figure 2.M and Figure 2.N.

The NEXT measurement is performed as a sequence of multiport S-parameter measurements using a VNA. The transfer functions from injection port to measurement port are added in the power domain.

*Note: During measurement, all unused ports must be terminated in 50Ω for Coax or 100Ω for STP.

2.2.4.2 Far-End Cable Bundle Crosstalk

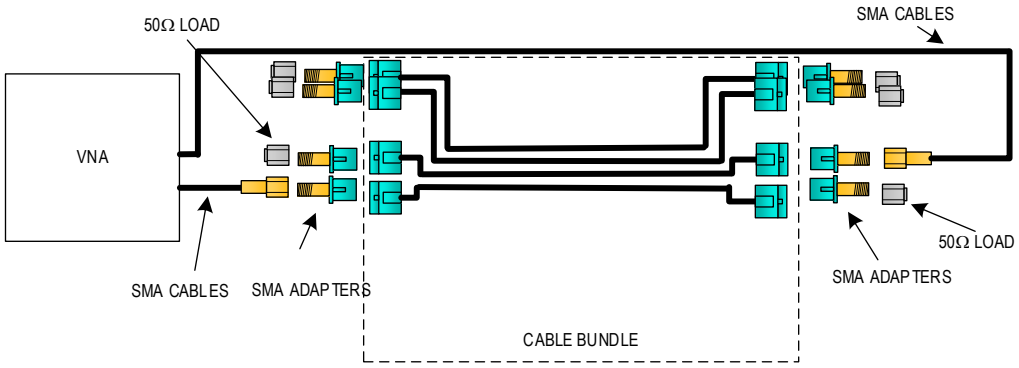


Figure 2.O. Far-End Crosstalk (FEXT) Coax

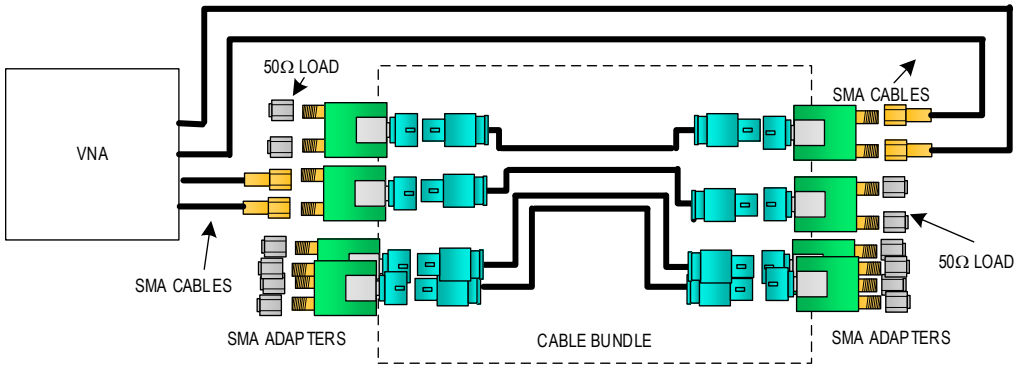


Figure 2.P. Far-End Crosstalk (FEXT) STP

Far-end crosstalk (FEXT) is a measure of the crosstalk received at the far-end of the cable with the disturbance applied at the near-end of the cable (Figure 2.O).

*Note: During measurement, all unused ports must be terminated in 50Ω for Coax or 100Ω for STP.

3. Measurement Boards

There are two preferred methods to model the channel specification. The first method copies the application PCB and replaces all GMSL2 ICs with high-quality SMA connectors. This ensures that any losses or discontinuities due to layout or components are preserved.

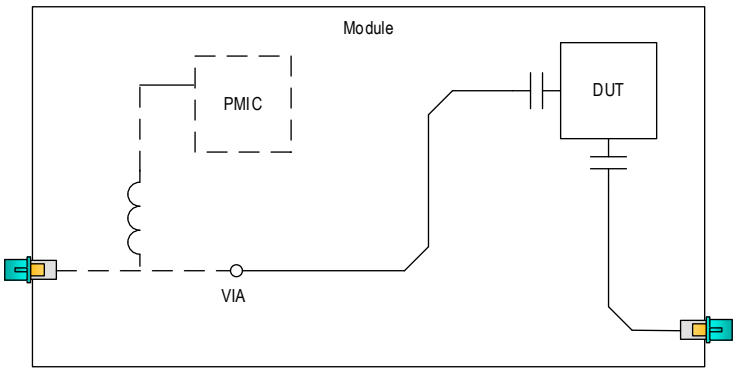


Figure 3.Q. Original PCB

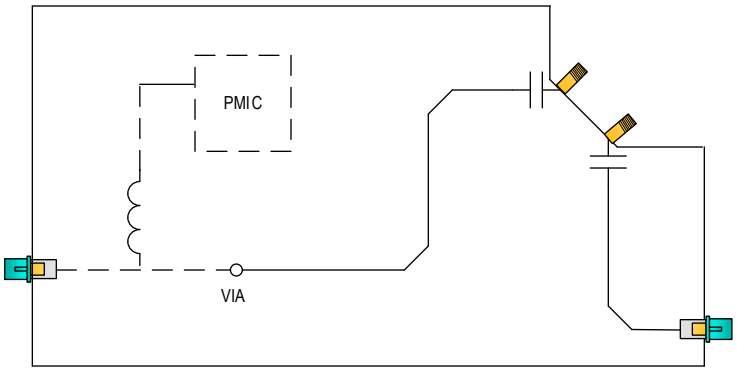


Figure 3.R. S-Parameter Measurement PCB

Alternatively, use a coupon board to model the channel. Keep the following parameters the same as the original PCB:

- Passive components (including connectors, filters, capacitors)
- Electrical length between components (including vias)
- Board Stack up

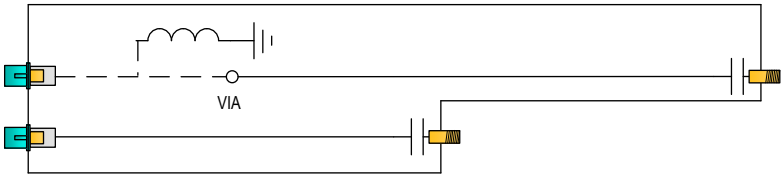


Figure 3.S. Coupon Board

4. Squelch Mode

Many measurements taken on PCB modules (TDR, S-parameters, Noise measurements) are with the GMSL2 device in place. To ensure proper termination, without turning on the transmitters, set the following parameters before making measurements. Note if both ends of the link are connected (e.g., serializer module connected to deserializer module), then both ends need to be put into squelch mode by their respective local uCs.

Command	Register/Setting	Notes
(Optional) Set the GMSL2 Bitrate and mode	GMSL2 = X TX_RATE = X RX_RATE = X	Set the modes if not already set by default configuration pin settings.
Turn on the correct link (Quad Deserializers)	Register 0x06 LINK_EN_A/B/C/D = X	Manually turn on the desired link.
Turn on the correct link (All others)	Register 0x0010 AUTOLINK = 0 LINK_CFG = XX	Turns off auto linking. Manually turn on the desired link.
Set the transmitters to squelch mode	RLMSA8 = 0xE0 RLMSA9 = 0xA8	Registers 0xXXA8 and 0xXXA9 in the relevant RLMS block

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION
0	6/23	Initial release