Evaluation Board User Guide

LT3046 Evaluation Kits

Evaluate: LT3046

General Description

The LT3046 evaluation kits (EV kits) feature the LT3046, a 20V, 200mA ultra-low noise and ultra-high power-supply rejection ratio (PSRR) low-dropout (LDO) linear regulator.

See the *Ordering Information* section for the two types of EV kits available to evaluate the LT3046. There is an EV kit that features a 12-lead, 3mm x 3mm, plastic dual-flat no-leads (DFN) package with an exposed pad on the bottom side of the IC, and there is also an EV kit that features an 11-ball, 1.621mm x 1.680mm, WLCSP Package. Proper board layout is essential for maximum thermal performance.

The LT3046 EV boards operate over an input voltage range of 3.8V to 20V. The LT3046 delivers a maximum output current of 200mA. In addition to featuring ultra-low noise and ultra-high PSRR, the regulator offers programmable power-good functionality and a programmable current limit. Current monitoring is also achieved by sensing the ILIM pin voltage.

Built-in protection includes reverse-battery protection, reverse-current protection, internal current limit with foldback and thermal limit with hysteresis.

For full details on the LT3046, refer to the *LT3046* data sheet, which must be consulted with this user guide when using the LT3046 EV kits.

Design files are available on the *LT3046 EV kit page*.

Features and Benefits

- Input Voltage Range: 3.8V to 20V
- Resistor-Programmed 3.32V Output Voltage
- Maximum Output Current: 200mA
- BNC Connectors for Noise and PSRR Measurement
- Resistor Programmed Power-Good
- Resistor-Programmable Current Limit, Current Monitoring, and UVLO
- Thermally Enhanced, 12-Lead, 3mm x 3mm, DFN Package or an 11-ball, 1.621mm × 1.680mm, WLCSP Package

Quick Start

Required Equipment

- A DC power supply
- Multimeters for voltage and current measurements
- Electronic or resistive loads

***Ordering Information* appears at end of data sheet.**

Procedure

The LT3046 EV kits are simple to set up to evaluate the performance of the LT3046. See *Figure 1* or *Figure 2* for the proper measurement equipment setup, and take the following steps:

1. Connect the load between the VOUT and GND terminals.
2. With power off, connect the input power supply to the VIN and GND terminals. Ensure that the shunt of JP1 is in the ON position.
3. With the load turned down, turn the input power supply on, and ensure that the voltage is between 3.8V and 20V.
4. Vary VIN from 3.8V to 20V and vary the load current from 0A to 200mA. Note the following when setting VIN and the load current:
   - An input voltage that is too close to the programmed output voltage (too low) can cause dropout operation and a loss of output-voltage regulation.
   - The amount of output current combined with an input voltage that is too high above the output can increase power dissipation to an unacceptable level.
   - The LT3046 limits output current at higher input-to-output voltage differentials (refer to the *LT3046* data sheet for more information).
5. Refer to *Application Note 83* and *Application Note 159* for measuring the output noise and PSRR. Note that J1 and J2 are Bayonet Neill-Concelman (BNC) connectors that are used for noise and PSRR measurements.
6. With JP1 in the ON position, R5 and R6 can be used to set an accurate undervoltage lockout (UVLO) threshold.
7. Change to a suitable ILIM resistor (R4) to program a current limit and provide output current monitoring at the resistor or pin.
8. In addition, change the PGFB divider resistors (R2 and R3) if the SET resistor (R1) is changed. Monitor power good at the PG terminal.
9. The position of JP2 selects either VEXT, VIN, or VOUT as the voltage for PG pull-up. Apply an external voltage to the VEXT terminal when JP2 is in the VEXT position.

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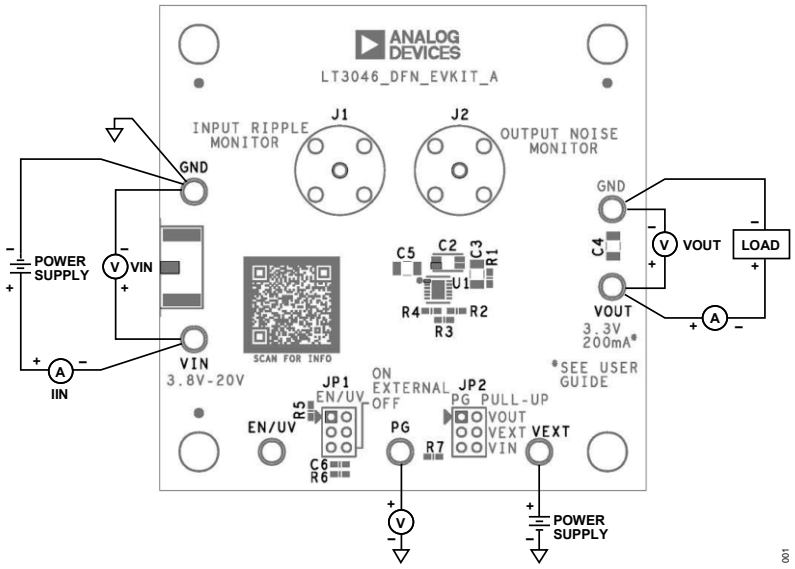

Figure 1. Proper Measurement Equipment Setup for the LT3046 DFN Package Evaluation Board

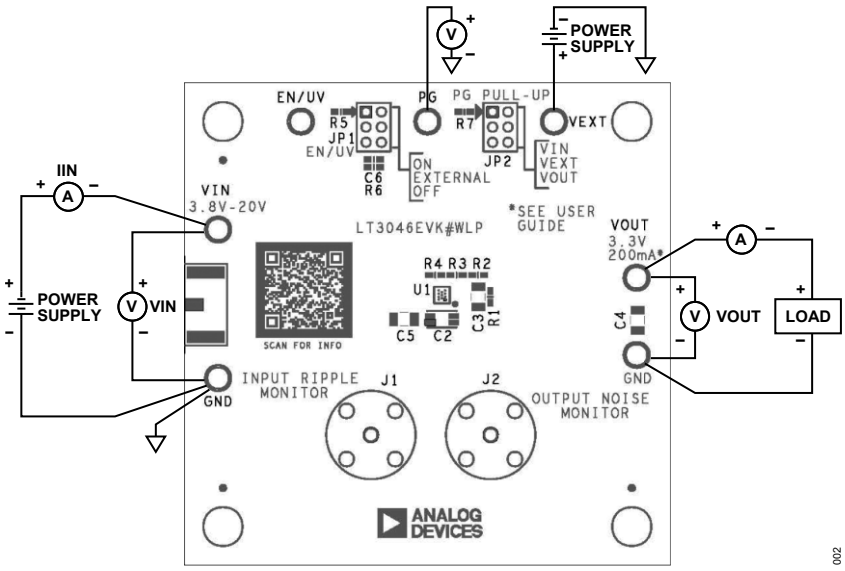

Figure 2. Proper Measurement Equipment Setup for the LT3046 WLCSP Package Evaluation Board

Revision History

REVISION NUMBER	REVISION DATE	NATURE OF CHANGE	PAGE NUMBER
0	10/23	Initial Release	—
A	04/24	Added EV kit for WLCSP Package	1–10

Performance Summary

Specifications are at T_A = +25°C, unless otherwise noted.

Table 1. Performance Summary for the LT3046 DFN Package Evaluation Board

PARAMETER	SYMBOL	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{IN}	I_{OUT} = 150mA, V_{OUT} = 3.3V	3.8		20	V
		I_{OUT} = 200mA, V_{OUT} = 3.3V	3.8		14.3[1]	V
Output Voltage	V_{OUT}	V_{IN} = 5V, I_{OUT} = 200mA, R1 = 33.2kΩ	3.25	3.32	3.39	V
Shutdown Input Current	I_{IN}	JP1 = off, R7 = open, V_{IN} = 6V		26		µA

[1] *The LT3046 limits output current at higher input-to-output voltage differentials. Refer to the LT3046 data sheet for more information.*

Table 2. Performance Summary for the LT3046 WLCSP Package Evaluation Board

PARAMETER	SYMBOL	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{IN}	I_{OUT} = 60mA, V_{OUT} = 3.3V	3.8		20	V
		I_{OUT} = 200mA, V_{OUT} = 3.3V	3.8		8.6[1]	V
Output Voltage	V_{OUT}	V_{IN} = 5V, I_{OUT} = 200mA, R1 = 33.2kΩ	3.25	3.32	3.39	V
Shutdown Input Current	I_{IN}	JP1 = off, R7 = open, V_{IN} = 6V		26		µA

[1] *The maximum power dissipation and, consequently, the maximum input voltage for an output that is programmed to 3.3V with a 200mA load is set by the 60°C temperature rise of the LT3046 on the evaluation board. In addition, consider the effect of ambient temperature and the maximum junction temperature that may occur. Refer to the LT3046 data sheet for more information.*

Printed Circuit Board (PCB) Layout

Best PSRR Performance: PCB Layout for Input Traces

For applications using the LT3046 for post-regulating switching converters, placing a capacitor directly at the LT3046 input results in AC current (at the switching frequency) flowing near the LT3046. Without careful attention to PCB layout, this relatively high frequency switching current generates an electromagnetic field (EMF) that couples to the LT3046 output, degrading its effective PSRR. The PSRR degradation can be 30dB at 1MHz but is also highly dependent on the PCB, the switching regulator, the input capacitor size, and other factors. This degradation is present even if the LT3046 is desoldered from the board because it effectively degrades the PSRR of the PCB itself. While negligible for conventional low PSRR LDO regulators, the ultra-high PSRR of the LT3046 requires careful attention to higher-order parasitics to realize the full performance offered by the regulator.

The LT3046 evaluation board alleviates this degradation in PSRR by using a specialized layout technique. The V_{IN} input trace and its corresponding return path (GND) are highlighted in red for just the DFN package evaluation board in *Figure 3* and *Figure 4*, but the traces are similar for the WLCSP package evaluation board. *Figure 4* also shows the location of the C1 input capacitor and the connection between the GND return path for the VIN input trace and GND for the rest of the PCB. Normally, when AC voltages are applied to the inputs of the board, AC current flows on the input and return paths, thus generating an electromagnetic field (EMF). This EMF couples to the C2 output capacitor and the related traces, making the PSRR appear worse than it actually is. With the input trace directly above the return path, the EMFs are in opposite directions, and consequently, cancel each other out. Making sure that these traces exactly overlap each other maximizes the cancellation effect and thus provides the maximum PSRR offered by the regulator.

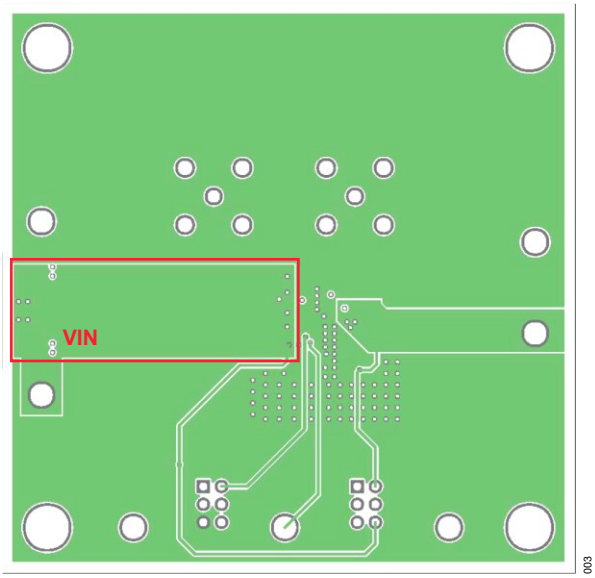

Figure 3. Layer 3 of the LT3046 DFN Package Evaluation Board

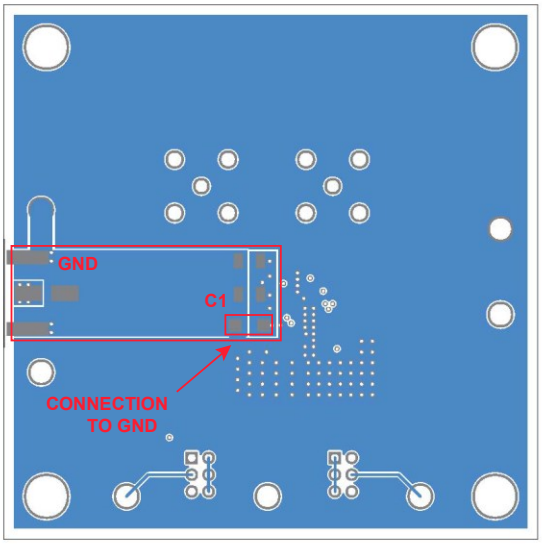

Figure 4. Layer 4 of the LT3046 DFN Package Evaluation Board

Best AC Performance: PCB Layout for Output Capacitor C2

For ultra-high PSRR performance, the LT3046 bandwidth is quite high (~750kHz), making it close to the self-resonance frequency (~1.6MHz) of the output capacitor. Therefore, it is important to avoid adding extra impedance (effective-series inductance (ESL) and effective-series resistance (ESR)) outside the feedback loop. To achieve this avoidance, minimize the effects of the PCB trace and solder inductance by Kelvin connecting the output sense pin (OUTS) and the SET pin capacitor (C_{SET}) GND directly to the terminals of the output capacitor (C2) using a split capacitor technique, as shown in *Figure 5*, *Figure 6*, and *Figure 7*. With only small AC current flowing through these connections, the impact of solder joint and/or PCB trace inductance on stability is eliminated. While the LT3046 is robust enough not to oscillate if the recommended layout is not followed, phase and gain margin and stability degrade.

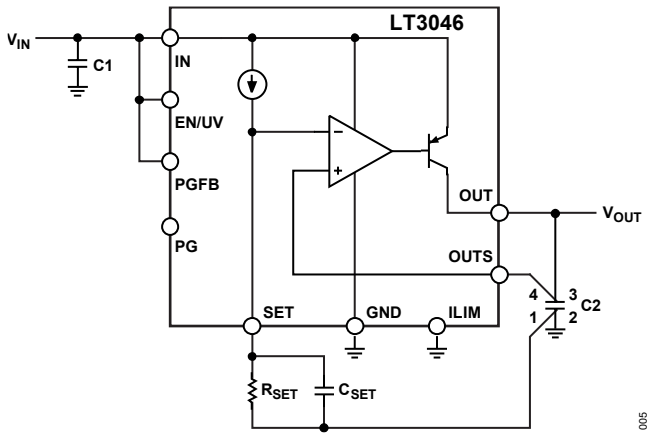

Figure 5. C2 and CSET Connections for Best Performance

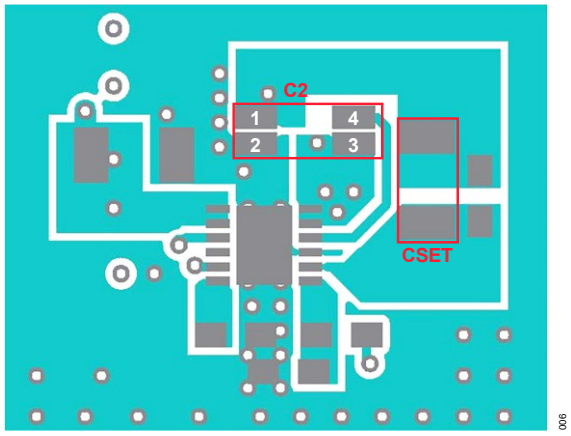

Figure 6. Split Pads for C2 in the Top Layer of the LT3046 DFN Package Evaluation Board

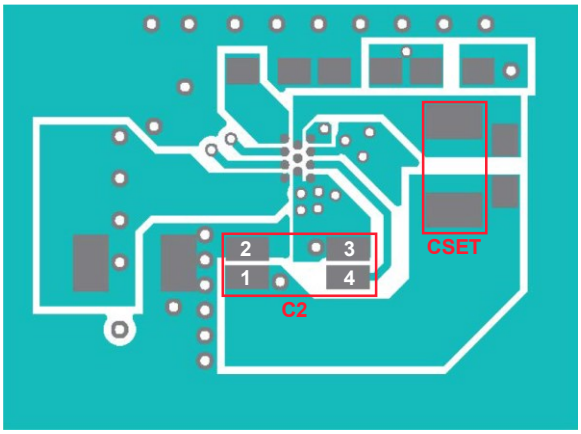

Figure 7. Split Pads for C2 in the Top Layer of the LT3046 WLCSP Package Evaluation Board

Default Jumper Settings

JUMPER	SHUNT POSITION	FUNCTION
JP1	Pin 1-2	Part enable
JP2	Pin 3-4	Power good pull-up to an external voltage

Ordering Information

PART	TYPE
LT3046EVK#DFN	LT3046 DFN Package EV Kit
LT3046EVK#WLP	LT3046 WLCSP Package EV Kit

#Denotes RoHS-compliant.

LT3046 EV Kit Bill of Materials for the LT3046 DFN Package

ITEM	QUANTITY	REFERENCE DESIGNATOR	PART DESCRIPTION	MANUFACTURER, PART NUMBER
REQUIRED CIRCUIT COMPONENTS				
1	1	C1	4.7µF capacitor, X7R, 25V, 10%, 1206	KEMET, C1206C475K3RAC
2	1	C2	4.7µF capacitor, X7R, 25V, 10%, 1206	Murata, GCM31CR71E475KA55L
3	1	C3	4.7µF capacitor, X7R, 25V, 10%, 1206	Murata, GCJ31CR71E475KA12L
4	1	R1	33.2kΩ resistor, 1%, 1/10W, 0603	Vishay, CRCW060333K2FKEA
5	1	U1	20V, 200mA, ultra-low noise, ultra-high PSRR, linear regulator	Analog Devices, Inc., LT3046ATC+ for LT3046EVK#DFN
OPTIONAL EVALUATION BOARD COMPONENTS				
1	1	CIN	22µF capacitor, 35V, 20%, 5mm x 5.4mm	KEMET, EDK226M035A9D
2	0	C4, C5	Capacitors, 1206, optional	
3	0	C6	Capacitor, 0603, optional	
4	1	R4	0Ω, 1/10W, 0603, AEC-Q200	Vishay, CRCW06030000Z0EA
5	1	R2	453kΩ resistor, 1%, 1/10W, 0603	Vishay, CRCW0603453KFKEA
6	1	R3	49.9kΩ resistor, 1%, 1/10W, 0603	Vishay, CRCW060349K9FKEA
7	1	R5	100kΩ resistor, 1%, 1/10W, 0603	Vishay, CRCW0603100KFKEA
8	1	R7	200kΩ resistor, 5%, 1/10W, 0603	Vishay, CRCW0603200KJNEA
9	0	R6	Resistor, 0603, optional	

HARDWARE				
1	7	EN/UV, GND, GND1, PG, VEXT, VIN, VOUT	Test points, turret, 0.094” PBF	Mill-Max, 2501-2-00-80-00-00-07-0
2	2	J1, J2	Connector, RF, BNC, receptacle, jack, 5-pin, straight, through-hole, 50 Ω	Amphenol RF, 112404
3	2	JP1, JP2	Connector, header, male, 2x3, 2mm, vertical, straight, through hole	Wurth Elektronik, 62000621121
4	2	XJP1, XJP2	Connector, shunt, female, 2 position, 2mm	Wurth Elektronik, 60800213421
5	4	MP1 to MP4	Standoff, nylon, snap-on, 6.4mm	Wurth Elektronik, 702931000

LT3046 EV Kit Bill of Materials for the LT3046 WLCSP Package

ITEM	QUANTITY	REFERENCE DESIGNATOR	PART DESCRIPTION	MANUFACTURER, PART NUMBER
REQUIRED CIRCUIT COMPONENTS				
1	1	C1	4.7µF capacitor, X7R, 25V, 10%, 1206	KEMET, C1206C475K3RAC
2	1	C2	4.7µF capacitor, X7R, 25V, 10%, 1206	Murata, GCM31CR71E475KA55L
3	1	C3	4.7µF capacitor, X7R, 25V, 10%, 1206	Murata, GCJ31CR71E475KA12L
4	1	R1	33.2kΩ resistor, 1%, 1/10W, 0603	Vishay, CRCW060333K2FKEA
5	1	U1	20V, 200mA, ultra-low noise, ultra-high PSRR, linear regulator	Analog Devices, Inc., LT3046ANQ+ for LT3046EVK#WLP
OPTIONAL EVALUATION BOARD COMPONENTS				
1	1	CIN	22µF capacitor, 35V, 20%, 5mm x 5.4mm	KEMET, EDK226M035A9D
2	0	C4, C5	Capacitors, 1206, optional	
3	0	C6	Capacitor, 0603, optional	
4	1	R4	0Ω, 1/10W, 0603, AEC-Q200	Vishay, CRCW06030000Z0EA
5	1	R2	453kΩ resistor, 1%, 1/10W, 0603	Vishay, CRCW0603453KFKEA
6	1	R3	49.9kΩ resistor, 1%, 1/10W, 0603	Vishay, CRCW060349K9FKEA
7	1	R5	100kΩ resistor, 1%, 1/10W, 0603	Vishay, CRCW0603100KFKEA
8	1	R7	200kΩ resistor, 5%, 1/10W, 0603	Vishay, CRCW0603200KJNEA
9	0	R6	Resistor, 0603, optional	
HARDWARE				
1	7	EN/UV, GND, GND1, PG, VEXT, VIN, VOUT	Test points, turret, 0.094” PBF	Mill-Max, 2501-2-00-80-00-00-07-0
2	2	J1, J2	Connector, RF, BNC, receptacle, jack, 5-pin, straight, through-hole, 50 Ω	Amphenol RF, 112404
3	2	JP1, JP2	Connector, header, male, 2x3, 2mm, vertical, straight, through hole	Wurth Elektronik, 62000621121
4	2	XJP1, XJP2	Connector, shunt, female, 2 position, 2mm	Wurth Elektronik, 60800213421
5	4	MP1 to MP4	Standoff, nylon, snap-on, 6.4mm	Wurth Elektronik, 702931000

LT3046 EV Kit Schematic for the LT3046 DFN Package

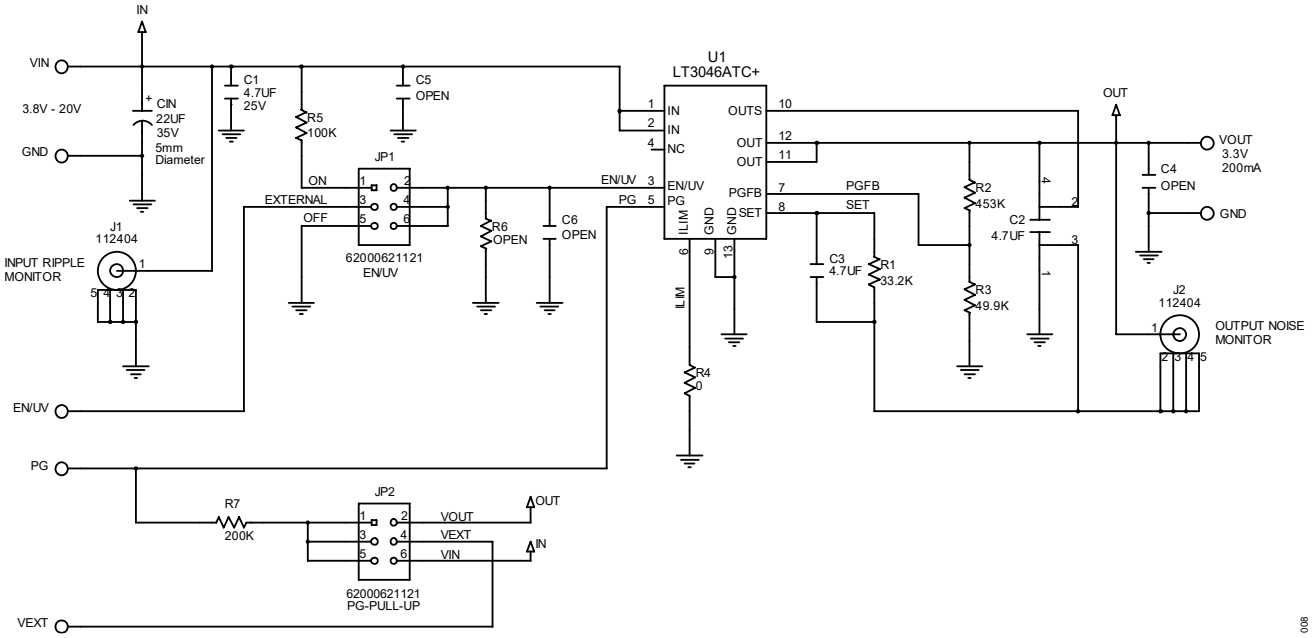

Figure 8. Schematic Diagram for the LT3046 DFN Package Evaluation Board

LT3046 EV Kit Schematic for the LT3046 WLCSP Package

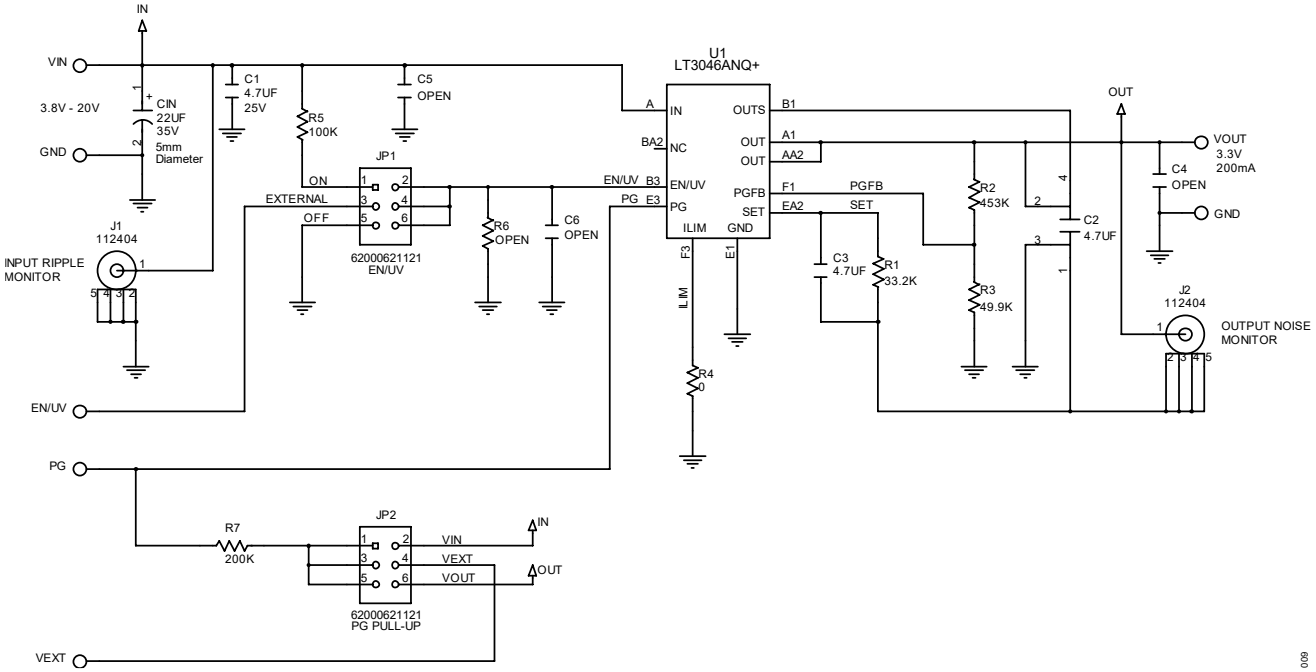

Figure 9. Schematic Diagram for the LT3046 WLCSP Package Evaluation Board

Notes