MAX1730x/MAX1731x Battery Pack Implementation Guide

UG6945; Rev 0; 4/19

Abstract

This application note describes the various steps for implementing the MAX17301–MAX17303/MAX17311–MAX17313 1-cell ModelGauge m5 EZ fuel gauge with protector and SHA-256 authentication in a battery pack. The memory programming instructions describe how to load the fuel gauge and authentication information and lock it to prevent tampering with the authentication or fuel-gauge mechanisms.

Table of Contents

List of Figures

List of Tables

Description

This guide provides the instructions for designing the PCB and programming the MAX17301/MAX17311/MAX17302/MAX17312/MAX17303/MAX17313 for use in battery packs. Proper circuit board layout is critical for measurement accuracy and ESD ruggedness. This application note is a guide for achieving the highest performance possible given limited board size and component position flexibility. **Figure 1** shows the typical schematic for battery pack-side application. This IC requires very short production test time.

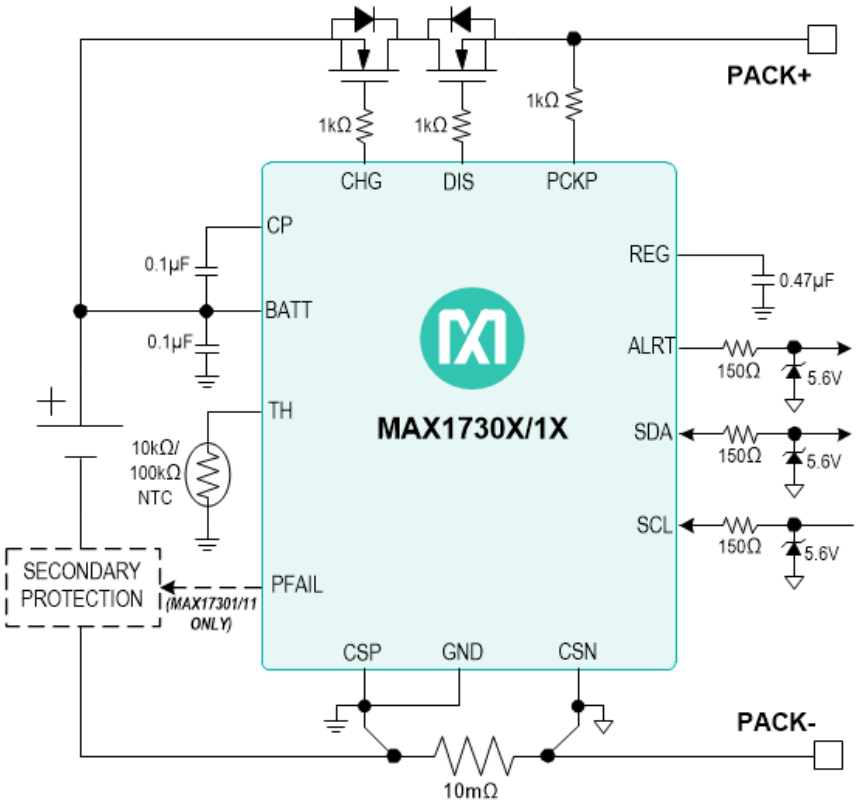

Figure 1. Typical application circuit.

Typical handheld applications limit board space to the dimensions of the accompanying cell. Components are normally limited to just one side of a 4-layer board with the external contacts located on the opposite side. The battery connection pads are normally on the ends, while the external contact pads are normally grouped in the middle. **Figure 2** shows the physical board requirements for this example.

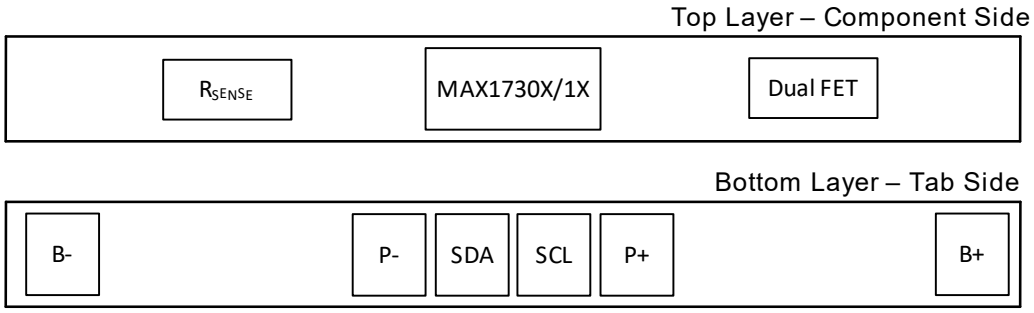

Figure 2. General board requirements.

Layout Considerations for Current Measurement Accuracy

To determine current flow through the pack, the MAX1730x/1x performs a differential voltage measurement across the external sense resistor through the CSP and CSN pins. The CSN pin is a high-impedance ADC input, but the CSP pin shares the ADC input with the power supply ground of the IC. Because there is current flow through the CSP pin, external resistance must be kept to a minimum. Any external resistance on CSP directly translates into a negative offset error of the current measurement result.

1. **Minimize CSP Trace Resistance**

   The CSP trace should travel directly from the CSP pin to the battery side of the sense resistor. The trace length should be minimized and should not travel through vias. Whenever possible, maximize the trace width.

2. **Minimize Regulator and Charge Pump Bypass Capacitor Loop Areas**

   The REG pin bypass capacitors should be mounted as close as possible to the IC with connections running directly to the CSP and REG pins. Similarly, the CP pin bypass capacitor should be put as close to the IC as possible with direct connection to the CP and BATT pins. Minimize any loop area between the capacitor and the IC.

3. **Kelvin Connection to Sense Resistor**

   The CSN and CSP traces from the IC should run directly to the inner side of the sense resistor pads. There should be no shared trace area with the high-current path of battery negative (B-) and pack negative (P-). For a WLP package, connect the GND pin to the high current path of the B- side trace and DO NOT directly connect the GND and CSP pins.

4. **Minimize CSN/CSP Loop Area**

   The CSP input is high impedance; therefore, the trace can have series resistance without affecting accuracy. Ideally, the CSP trace should run parallel to the CSN trace to minimize inductive loop area between the two.

5. **Exposed Pad Connection (TDFN)**

   Connect the exposed pad directly to the CSP pin.

Figure 3 shows the recommended board layout to achieve maximum current measurement accuracy. The circuit connections related to current measurement are shaded dark blue in the example.

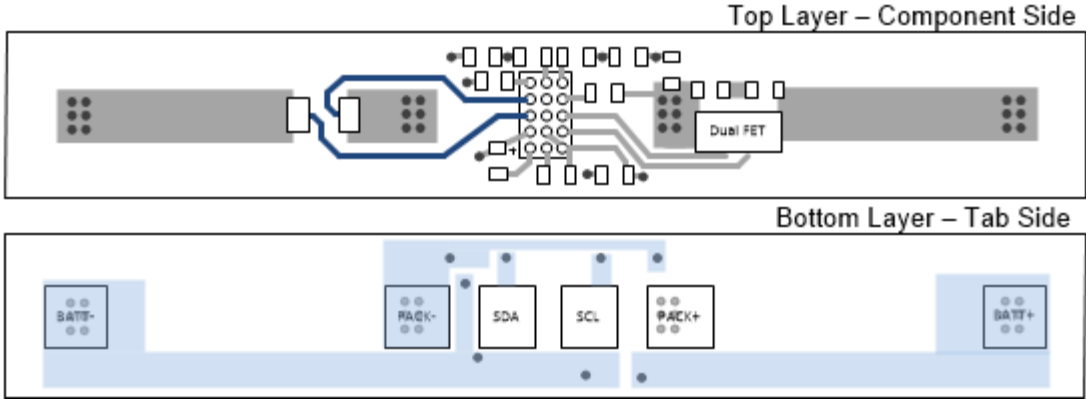

Figure 3. Recommended layout for current measurement accuracy.

Layout Considerations for ESD Immunity

ESD energy can enter the cell pack through the exposed output pads. The energy follows the most direct path to the cell and leaves the cell pack through capacitive coupling to the environment. The goal of adding ESD protection to the MAX1730x/1x circuit board is to provide a channel for the ESD energy to leave the board safely and provide a buffer area around the MAX1730x/1x to isolate it.

External capacitors are added in series to provide a high energy path around the protection FETs and between the pack outputs. The zener diodes on the communication lines allow ESD energy to move to the negative pack terminal. The communication line resistors limit current through these diodes during an ESD event. **Figure 4** shows the desired high energy paths during ESD events.

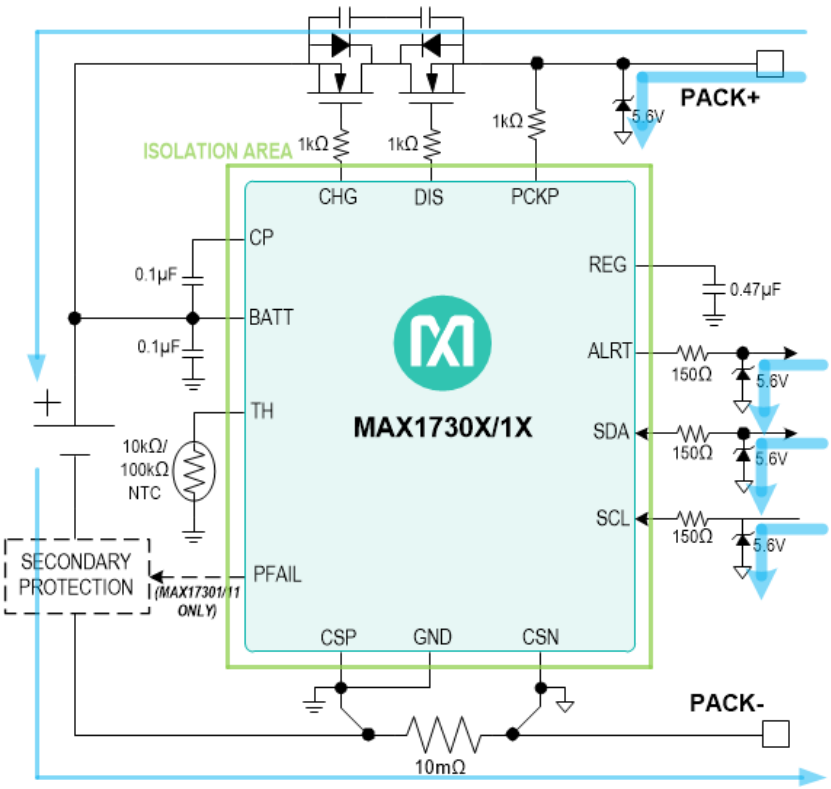

Figure 4. Circuit schematic showing ESD channeling paths.

For circuit layout, traces expected to carry ESD energy should have minimum inductance. They should be wide and short, and travel in the most direct manner possible from the input pads to the cell tabs. Ideally, the MAX1730x/1x should be completely removed from any area carrying high current; however, cell pack board limitations make this nearly impossible in most applications. At a minimum, the MAX1730x/1x should be isolated from these paths as much as possible by physical placement of the IC and by surrounding the IC with a ground plane.

1. **Passive Component Placement**

   Depending on ESD strike location and polarity, ESD energy travels through the communication line series resistors and zener diodes to PACK-. The ideal placement location for these components is directly behind the input pads using wide circuit traces. This helps direct the ESD energy through these components and away from the IC.

2. **FET Bypass Capacitors**

   FET bypass capacitors help provide an alternate path to channel ESD energy away from the protection FETs. As with the other passive components, trace widths should be kept short and wide.

3. **Ground Plane**

   Any unused board area on the component layer and middle layers should be connected to a ground plane that isolates the IC as much as possible from the ESD channeling traces. This ground plane should be connected to the negative battery terminal as close as possible to the B- tab.

Nonvolatile Memory Operations

Table 1 shows the nonvolatile memory of the MAX1730x/1x. The highlighting described in **Figure 5** separates the sections into what is provided by the battery characterization table, what is programmed by the factory, and the registers that are free or configurable to be free memory.

Table 1. MAX1730x/1x Nonvolatile Memory

Page	18xh	19xh	1Axh	1Bxh	1Cxh	1Dxh	1Exh
0h	nXTable0	nOCVTable0	nQRTable00	nConfig	nPermVal0	nVPrtTh1	nDPLimit
1h	nXTable1	nOCVTable1	nQRTable10	nTaskPeriod	nPermVal1	nTPrtTh1	nScOcvLim
2h	nXTable2	nOCVTable2	nQRTable20	nMiscCfg	nPermVal2	nTPrtTh3	nAgeFcCfg
3h	nXTable3	nOCVTable3	nQRTable30	nDesignCap	nPermVal3	nIPrtTh1	nDesignVoltage
4h	nXTable4	nOCVTable4	nCycles	nSBSCfg	nRGain	nVPrtTh2	nVGain
5h	nXTable5	nOCVTable5	nFullCapNom	nPackCfg	nPackResistance	nTPrtTh2	nRFastVShdn
6h	nXTable6	nOCVTable6	nRComp0	nRelaxCfg	nFullSOCThr	nProtMiscTh	nManfctrDate
7h	nXTable7	nOCVTable7	nTempCo	nConvgCfg	nTTFCfg	nProtCfg	nFirstUsed
8h	nXTable8	nOCVTable8	nBattStatus	nNVCfg0	nCGain	nJEITAC	nSerialNumber0
9h	nXTable9	nOCVTable9	nFullCapRep	nNVCfg1	nTCurve	nJEITAV	nSerialNumber1
Ah	nXTable10	nOCVTable10	ndQTot	nNVCfg2	nTGain	nJEITACfg	nSerialNumber2
Bh	nXTable11	nOCVTable11	nMaxMinCurr	nHibCfg	nTOff	nStepChg	nDeviceName0
Ch	nVAlrtTh	nIChgTerm	nMaxMinVolt	nROMID0	nManfctrName0	nDelayCfg	nDeviceName1
Dh	nTAlrtTh	nFilterCfg	nMaxMinTemp	nROMID1	nManfctrName1	nODSCTh	nDeviceName2
Eh	nIAlrtTh	nVEmpty	nSOC	nROMID2	nManfctrName2	nODSCCfg	nDeviceName3
Fh	nSAlrtTh	nLearnCfg	nTimerH	nROMID3	nRSense	nCheckSum	nDeviceName4

Required for Custom Model	If a custom battery model is being used, these registers will need to be programmed.
Reserved for 1-Wire ID	These registers are used for the 1-Wire® ROM ID and device serial number. They are not writable. Do not configure these registers.
Free Memory	These registers don't have fuel-gauge functions. The customer can use these registers for operations suggested by the names (such as SerialNumber, ManfctName), or use them as free memory.
Freeable Memory	These registers contain general algorithm/IC operation configurations, but the default configuration values can be loaded from ROM. If unused, these registers are free for customer data storage.
Required for Protector Configuration	Configuration of these registers is mandatory if protector functionality is enabled.
Mandatory Configuration Registers	These registers must be configured for the IC to work correctly.

Figure 5. Nonvolatile memory operation descriptions.

1-Wire is a registered trademark of Maxim Integrated Products, Inc.

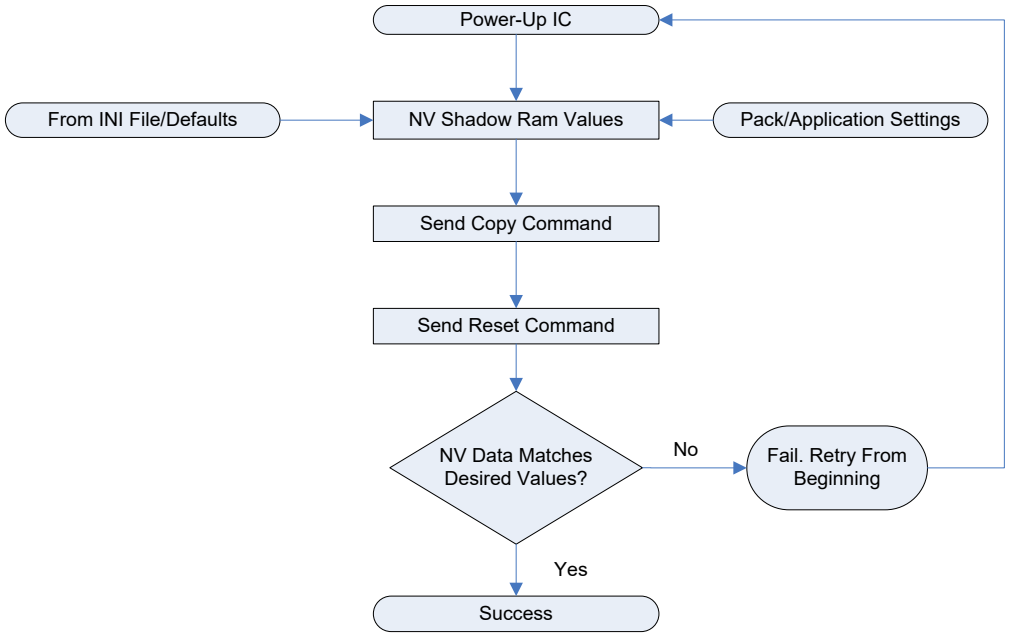

Figure 6. Nonvolatile memory loading process.

The starting values for the memory table should be obtained from the INI file (or default values if no custom model is available). The evaluation kit (EV kit) GUI configuration wizard can be used to configure the nonvolatile memory, or the values can be constructed by exploring each register in the data sheet. Use the “export INI” functionality in the GUI to export the full INI. In the full INI, all the register values starting from 0x180 are listed. The free memory can be written to any values desired by the pack maker or end customer. Modify the free memory region as desired in the INI file and save the file.

Once the values are known, they should be written to the Shadow memory at the addresses listed in **Table 1**. To copy the contents of Shadow Ram to nonvolatile memory, send command 0xE904 to register 0x060 to initiate a burn. Wait until CommStat.NVBusy is cleared to indicate the copy command is complete. This takes approximately 368ms (t_{BLOCK}). Register 0x061 (CommStat) contains the NVBusy and NVError bits. NVError is set if an error occurred during the burn. NVBusy is clear when the burn operation is complete.

The IC should be reset to force the RAM to update to the desired configuration. To issue a full IC reset, the ESD detection mechanism must be bypassed. This is accomplished by modifying the model table. The following sequence forces a complete IC reset. If the fuel-gauge performance is evaluated shortly after the reset, the battery must be relaxed (no charge or load for 1 hour) before the reset command is sent.

1. Write register 0x080 = 0x0000.
2. Write register 0x060 = 0x000F.
3. Wait 150ms (NV memory recall and RAM initialization).
4. Write register 0x0BA to clear bit 0x8000. (Disable hibernate mode. It should be re-enabled at the end of factory production.)

After the reset is complete, the contents of the nonvolatile memory should be verified against the desired write values. If everything matches, the process is complete. If there is any discrepancy,

the number of write cycles should be examined to check if there is nonvolatile memory remaining. See the *Determining the Number of Remaining Updates* section of the data sheet for details.

Setting the SHA Secret for Authentication

The SHA secret in the IC cannot be directly read out or written. To initialize the SHA secret, the following sequence is needed:

1. Clear the NVError bit (write register 0x060 = 0).
2. Validate that the secret is all zeros by computing a response with all zeros.
3. If the secret is not all zeros, clear the SHA secret to all zeros (write register 0x060 = 0x5A00).
4. The secret clears to all zeros after the NVBusy flag clears (t_{UPDATE} = 64ms typical).
5. Write a challenge to addresses 0x0C0 to 0x0C9.
6. Send either the next secret with ROM ID (write 0x060 = 0x3300) or without ROM ID (write 0x060 = 0x3000).
7. The new secret is the last 160 bits of the response.
8. Validate that the internal secret is what is expected by writing a new challenge and validating the response.
9. Send the Lock Secret command (write 0x060 = 0x6000). **This lock is irreversible**. It permanently locks the SHA secret, and it is not changeable. If a multistep secret generation process is used, the lock should only be set at the final step.

Production Test

Hibernate mode should already be disabled in the nonvolatile memory initialization section. If it is not disabled, clear HibCfg.EnHib. Ensure that Status2.HibStat is clear before proceeding.

1. Check Communication
   - Validate that the IC is powered on by reading the DevName register (0x021). If the IC responds with the correct version number, the communication test is successful.
2. Check Voltage Measurement
   - Read the VCell register and compare the measured voltage against the IC readings. If the error is less than 10mV, the voltage measurement check is successful.
3. Check No Load Current Measurement
   - Check the Current and AvgCurrent registers. The current should read in the range of +1mA to -1mA.
4. Set the load to the lesser of half the full-scale measurement range (25mV/R_{SENSE}), or half of the cell C-Rate (C/2).
   - Apply the selected load current.
   - Read the Current register.
   - Wait until the Timer register changes (up to 702ms).

- The test is successful if the current reading is in an acceptable range of the set load current.

Calibration

This fuel gauge does not require any calibration for accurate fuel-gauging. The voltage, current, and temperature accuracy are trimmed during the Maxim factory test program. The algorithm does not require any cycling for accurate state-of-charge (SOC) reporting.

For a special pack-side application with a sense resistor that is lower than 2mΩ, or if there is requirement for absolute current measurement accuracy or absolute capacity accuracy in additional to fuel-gauge SOC accuracy, an additional calibration procedure can be performed.

Preparation for Current Offset Calibration

The current offset calibration requires a long period during which the battery pack is unloaded. It is suggested that, in production phase, there is a long delay between battery assembly and test/calibration.

From Battery Assembly to Test and Calibration

At the start of battery assembly, the internal timer on the IC starts operation. At the same time, the raw coulomb counter starts to accumulate unloaded offset current. When calibrating, the accumulated result of the coulomb counter will be divided by the time elapsed from the start of the battery assembly to get the long-time-average offset current value.

Current Calibration Process

With a carefully designed sense resistor layout and sensing trace, there is typically no need to calibrate current offset for a sense resistance higher than 3mΩ. Usually, good sense resistor layout is more important than calibration. Contact Maxim Technical Support to have the PCB layout checked before calibrating.

For complete calibration, you will need:

- Calibrated power supply with 6V/5A range channel (alternatively, a battery soldered on PCB design already)
- Calibrated ammeter with more than 5A range
- Calibrated load box with more than 5A range
- MAX173xxxEVKIT with USB Micro-B cable
- Official EV kit GUI with newest version number and a PC with Windows 7 or above

Make sure that the connections are the same as shown in **Figure 7**.

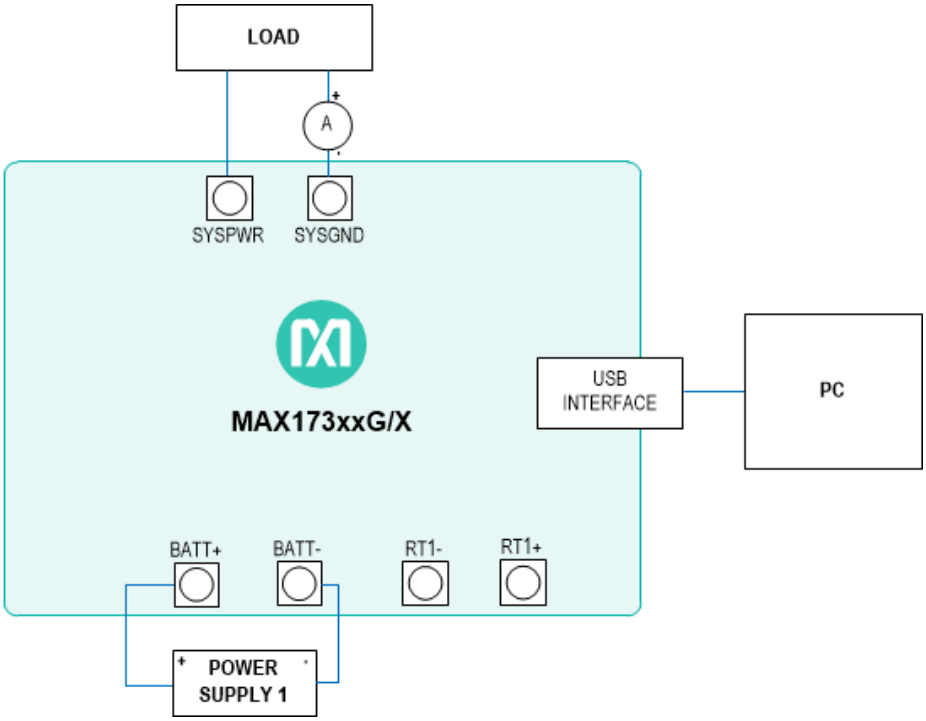

Figure 7. Calibration connections.

Calibration Steps

1. Keep the load off and disconnected. Set Power Supply 1 to 4V, output on (or use a battery as Power Supply 1). Apply a charger, short the PACK+ to BATT+, or on the EV kit, push button S1 to wake up the chip.
2. Read the following four registers together:
   - Timer register (0x6C:0x3E), Timerh register (0x6C:0xBE)
   - QH register (0x6C:0x4D), QL register (0x6C:0x4E)
3. Calculate 32-bit Q = (QH << 16) | QL (signed two's complement value)
   a. Calculate 32-bit T = (Timerh << 16) | Timer
   b. Calculate Offset = Round (-Q/T)
4. Set the COFF register (0x6C:0x2F) to Offset.

   This completes Current Offset Calibration.
5. Set the FilterCfg register (0x6C:0x29) to 0x0EA3. This sets the filtering time constant at 2.8125s.
6. Set the load box to sink at Curr_Test less than the source limit of Power Supply 1 and turn on the load.

7. Read the ammeter reading, and denote it as CURRENT_REF. (e.g., CURRENT_REF = 4.985A)
8. Wait 0.5s for the MAX17303 to read the current.
9. Read the current register (0x6C:0x1C) and denote it as CURRENT_INST. Write the CURRENT_INST value to the AvgCurrent register (0x6C:0x1D). This accelerates the averaging filter.
10. Wait 5s. Read the AvgCurrent register. Denote this value as CURRENT_MEAS (e.g., CURRENT_MEAS = -5.001A).

nCGAIN Register format:

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Definition	GAIN										OFF					
POR (Binary)	0b0100000000										0b000000					
POR (Hex)	0x4000															

For gain, 0b0100000000 is 100%. Scale this value to the desired gain.

11. Calculate the value of CGAIN:

$$raw\_gain = Round\left(\frac{abs(CURRENT\_MEAS)}{abs(CURRENT\_REF)} \times 0b010000000000\right)$$

nCAIN.GAIN = last 10 bits of (raw_gain >> 2) + [(raw_gain and 2) >> 1]

nCAIN.OFF = last 6 bits of COFF

(The above measurements give raw_gain = 0x03FD.)

This completes Current Gain Calibration.

NVMemory Burn: nCGAIN. This sets both CGAIN and COFF permanently.

Conclusion

This application note describes the various steps for implementing the MAX1730x/MAX1731x in a battery pack. Follow this guide closely during design, evaluation, and production phases. System circuit design and layout that does not follow guidance may affect measurement accuracy. The memory programming instructions describe how to load the fuel-gauge and authentication information and lock it to prevent tampering with the authentication or fuel-gauge mechanisms. See the **MAX1730x/MAX1731x Host Software Implementation Guide** for details on software implementation.