MAX17320 Battery Pack Implementation Guide

UG7177; Rev 0; 3/20

Abstract

This guide aims at helping the battery pack maker to design the battery pack with the MAX17320 battery fuel-gauge + protector. It introduces the necessary processes for design, layout, factory programming, and testing for the fuel gauge.

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Description

The MAX17320 battery fuel-gauge + protector is the most integrated solution for multiple series cell battery pack applications. This guide provides the instructions for designing the PCB and programming the MAX17320 for use in battery packs. Proper circuit board layout is critical for measurement accuracy and ESD ruggedness. This application note is a guide for achieving the highest performance possible given limited board size and component position flexibility. Figure 1 shows the typical schematic for battery pack side application. This IC requires less than 3s of production test time.

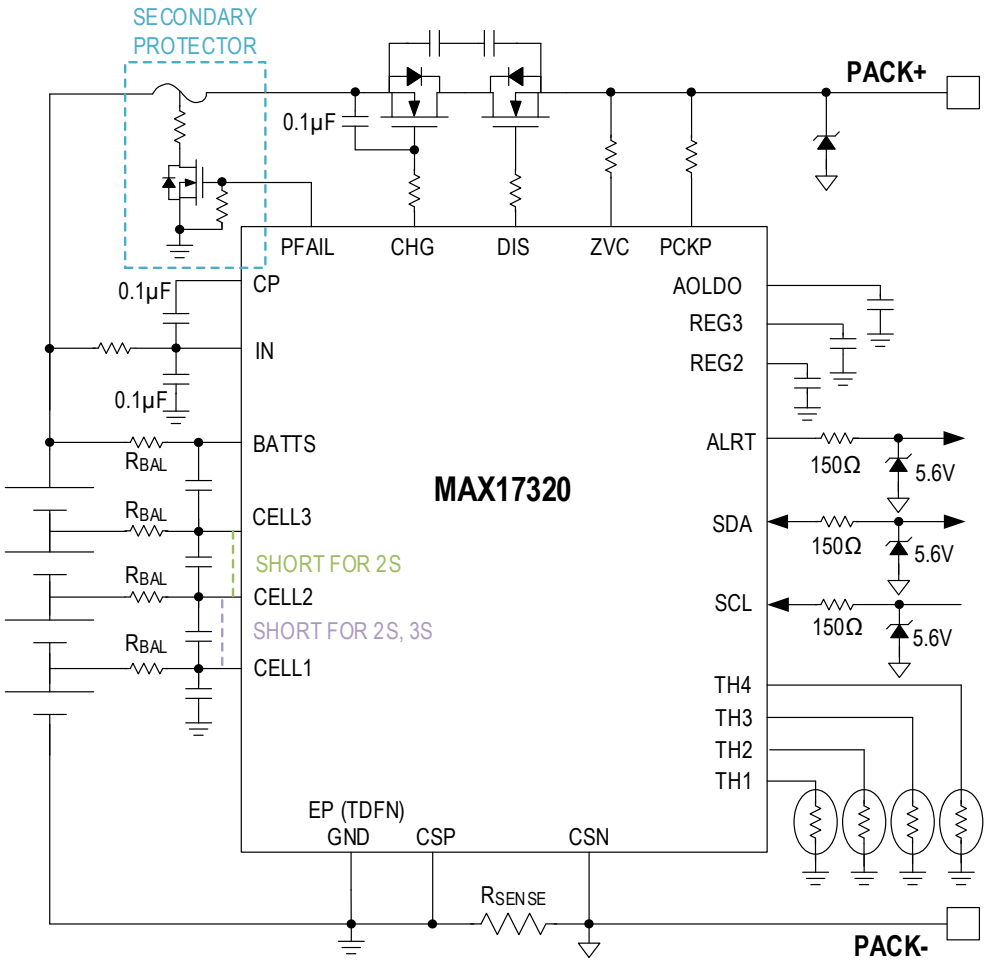

Figure 1. Example circuit schematic.

The typical board requirements for a handheld application limit the board space to the dimensions of the accompanying cell. Components are typically limited to just one side of a 4-layer board with the external contacts located on the opposite side. The battery connection pads are normally on the ends, while the external contact pads are generally grouped in the middle. Figure 2 shows the physical board layout example.

Layout Considerations for Current Measurement Accuracy

Figure 2 shows a typical example layout for pack-side applications.

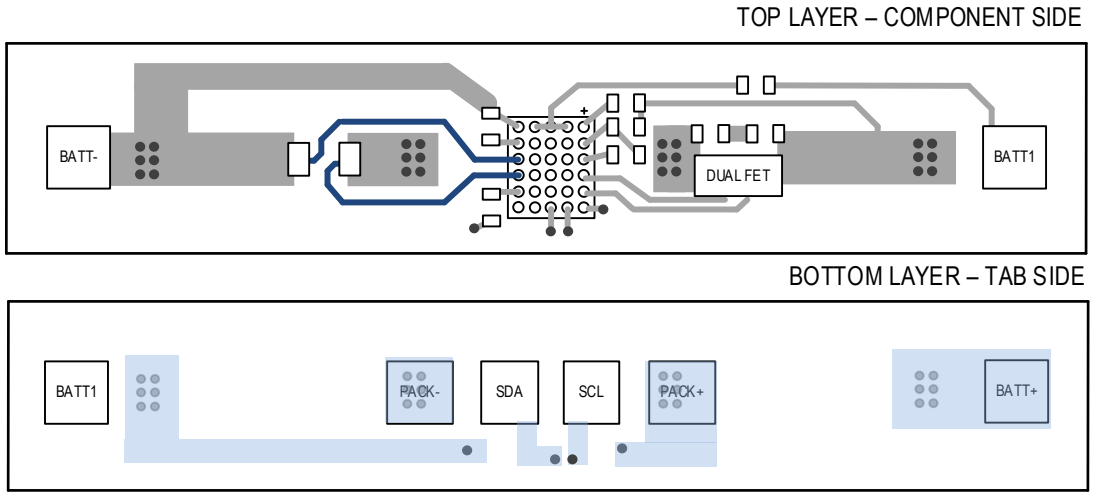

Figure 2. MAX17320 layout example (only top and bottom layer shown).

Use the following five recommendations for layout design:

1. Minimize the regulator and charge pump bypass capacitor loop areas.

   The REG2 and REG3 pin bypass capacitor should be mounted as close as possible to the IC with connections running directly to the GND and REG pins. Similarly, the CP pin bypass capacitor should be put as close to IC as possible with direct connection to the CP and the IN pins. Minimize any loop area between the capacitor and the IC.

2. Kelvin connection to the sense resistor.

   The CSN and CSP traces from the IC should run directly to the inner side of the sense resistor pads. There should be no shared trace area with the high-current path of battery negative (B-) and pack negative (P-) traces. Connect the GND pin to the high-current path of the B- side trace and DO NOT directly connect the GND and CSP pin. Do not branch the CSN/CSP lines in any way.

3. Minimize the CSN/CSP loop area.

   The CSP input is high impedance and therefore the trace can have series resistance without affecting accuracy. However, ideally the CSP trace should run parallel the CSN trace to minimize inductive loop area between the two.

4. Make the trace for CELL1, CELL2, CELL3, and BATTS thicker.

   Make the trace thick enough according to the balancing current setting.

5. Exposed pad connection (TDFN).

   Connect the exposed pad directly to the GND pin.

Layout Considerations for ESD Immunity

ESD energy can enter the cell pack through the exposed output pads. The energy will follow the most direct path to the cell and leave the cell pack through capacitive coupling to the environment. The goal of adding ESD protection to the MAX17320 circuit board is to provide a channel for the ESD energy to leave the board safely and provide a buffer area around the MAX17320 to isolate it.

External capacitors are added in parallel to provide a high energy path around the protection FETs and between the pack outputs. The zener diodes on the communication lines allow ESD energy to move to the negative pack terminal. The communication line resistors limit current through these diodes during an ESD event. See Figure 3 as a 4S example.

For circuit layout, traces expected to carry ESD energy should have minimum inductance. They should be wide and short, and travel in the most direct manner as possible from the input pads to the cell tabs. Ideally, the MAX17320 should be completely removed from any area carrying high current. However, cell pack board limitations make this nearly impossible in most applications. At a minimum, the MAX17320 should be isolated from these paths as much as possible by physical placement of the IC and by surrounding the IC with a ground plane.

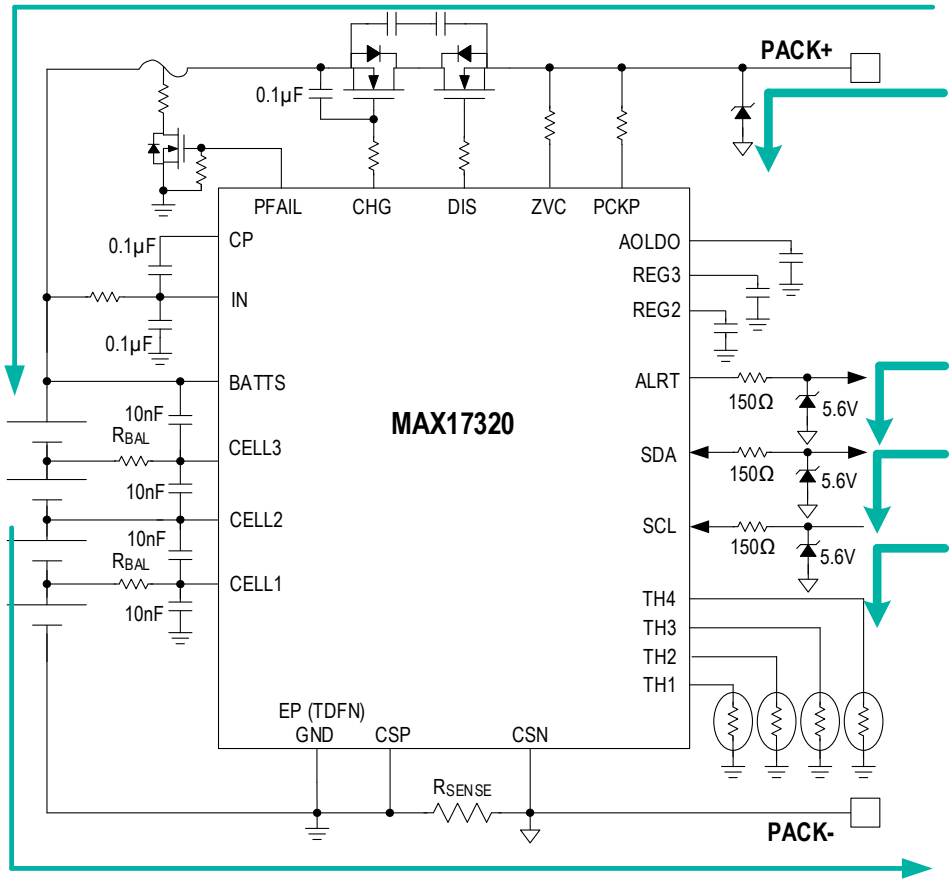

Figure 3. MAX17320 ESD energy flow.

Follow these three points for proper pack-side ESD design:

1. Passive component placement.

Depending on ESD strike location and polarity, ESD energy travels through the communication line series resistors and zener diodes to PACK-. The ideal placement location for these components is directly behind the input pads using wide circuit traces. This helps direct the ESD energy through these components and away from the IC.

2. FET bypass capacitors.

   FET bypass capacitors help provide an alternate path to channel ESD energy away from the protection FETs. As with the other passive components, trace widths should be kept short and wide.

3. Ground plane.

   Any unused board area on the component layer and middle layers should be connected to a ground plane that isolates the IC as much as possible from the ESD channeling traces. This ground plane should be connected to the battery negative as close as possible to the B- tab.

Nonvolatile Memory Operations

Table 1 shows the nonvolatile memory of the MAX17320. The different highlighting separates the sections into what will be provided by the battery characterization table, what will be programmed by the factory, and the registers that are free or configurable to be free memory.

Table 1. Nonvolatile Memory Registers of the MAX17320

Page	18xh	19xh	1Axh	1Bxh	1Cxh	1Dxh	1Exh
0h	nXTable0	nOCVTable0	nQRTable00	nConfig	nPReserved0	nUVPrtTh1	nDPLimit
1h	nXTable1	nOCVTable1	nQRTable10	nTaskPeriod	nPReserved1	nTPrtTh1	nScOcvLim
2h	nXTable2	nOCVTable2	nQRTable20	nMiscCfg	nChgCfg	nTPrtTh3	nAgeFcCfg
3h	nXTable3	nOCVTable3	nQRTable30	nDesignCap	nChgCtrl	nIPrtTh1	nDesignVoltage
4h	nXTable4	nOCVTable4	nCycles	nSBSCfg	nRGain	nBalTh	RSVD
5h	nXTable5	nOCVTable5	nFullCapNom	nPackCfg	nPackResistance	nTPrtTh2	RSVD
6h	nXTable6	nOCVTable6	nRComp0	nRelaxCfg	nFullSOCThr	nProtMiscTh	nManfctrDate
7h	nXTable7	nOCVTable7	nTempCo	nConvgCfg	nTTFCfg	nProtCfg	nFirstUsed
8h	nXTable8	nOCVTable8	nBattStatus	nNVCfg0	nCGain	nJEITAC	nSerialNumber0
9h	nXTable9	nOCVTable9	nFullCapRep	nNVCfg1	nTCurve	nJEITAV	nSerialNumber1
Ah	nXTable10	nOCVTable10	nVoltTemp	nNVCfg2	nThermCfg	nOVPrtTh	nSerialNumber2
Bh	nXTable11	nOCVTable11	nMaxMinCurr	nHibCfg	RSVD	nStepChg	nDeviceName0
Ch	nVAlrtTh	nIChgTerm	nMaxMinVolt	nROMID0	nManfctrName0	nDelayCfg	nDeviceName1
Dh	nTAlrtTh	nFilterCfg	nMaxMinTemp	nROMID1	nManfctrName1	nODSCTh	nDeviceName2
Eh	nIAlrtTh	nVEmpty	nFullCapFlt	nROMID2	nManfctrName2	nODSCCfg	nDeviceName3
Fh	nSAlrtTh	nLearnCfg	nTimerH	nROMID3	nRSense	nCheckSum	nDeviceName4

Legend:

Required for Custom Model	If a custom battery model is being used, these registers will need to be programmed.
Reserved for 1-Wire ID	These registers are used for the 1-Wire ROM ID and device serial number. They are not writable. Do not configure these registers.
Free Memory	These registers do not have fuel-gauge functions. The customer can use these registers for operations suggested by the names (Such as SerialNumber, ManfctName), or use them as free memory.
Free-able Memory	These registers contain general algorithm/IC operation configurations, but the default configuration values can be loaded from ROM. If unused, these registers are free for customer data storage.
Required for Protector Configuration	Configuration of these registers is mandatory if protector functionality is enabled.
Mandatory Configuration registers	These registers must be configured for the IC to work correctly.

Steps to Develop and Finalize Manufacturing Configuration INI File

1. Contact local Maxim support to characterize your battery fuel-gauging model. (This is not required if using the EZ model.) If the battery is characterized by Maxim, you will obtain an initial INI file.
2. Download the MAX17320 GUI and request a MAX17320 evaluation kit (EV kit) to evaluate the performance with the MAX17320 GUI.
3. In the **Configuration** tab, click the **Launch** button to launch the configuration wizard.
4. In the configuration wizard, follow the steps to configure the nonvolatile memory. You will be asked to include the characterization INI file if you have characterized the battery.
5. In the last step, click **Save new configuration settings to .INI file**, and click the **Update IC** button. As a result, a full configuration INI is generated. The full configuration INI will include all the required setting values for the nonvolatile memory.
6. Perform testing on the EV kit with the full INI parameters and see if any adjustment is needed. Finalize the configuration INI setting after this step.

Nonvolatile Memory Loading During Production

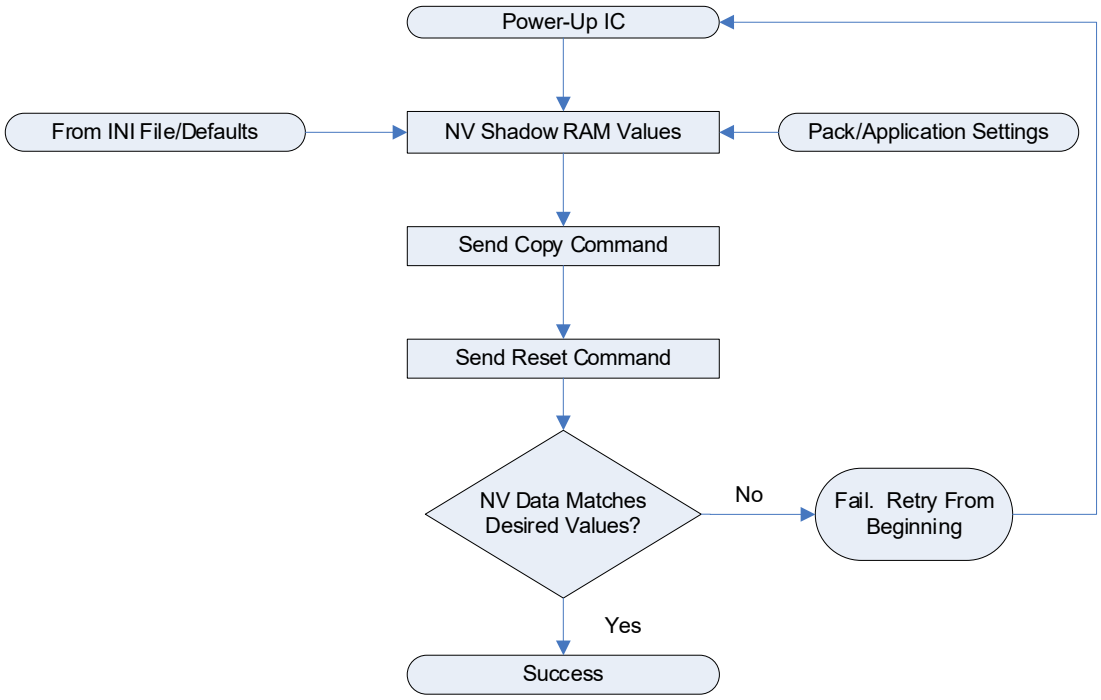

Figure 4. Nonvolatile memory loading process.

The process of nonvolatile memory loading is shown in Figure 4. Once you decide the nonvolatile values, write the values into the shadow RAM memory at the addresses listed in Table 1. To copy the contents from the shadow RAM to nonvolatile memory, unlock write protection and send command 0xE904 to register 0x60 to initiate a burn. Wait until CommStat.NVBusy is cleared to indicate the copy command is complete. This will take approximately 368ms (t_{BLOCK}). Register 0x61 (CommStat) contains the NVBusy and NVError bits. NVError is set if an error occurred during the burn. NVBusy will be clear when the burn operation is complete. The following is a step-by-step guide to program the nonvolatile memory:

1. Write 0x0000 to the CommStat register (0x61) twice in a row to unlock write protection.
2. Write all nonvolatile memory locations, excluding nROMID0/1/2/3, to full configuration INI values. Then, check if all nonvolatile memory has written correctly. If not, write again.
3. Write 0x0000 to the CommStat register (0x61) one more time to clear the CommStat.NVError bit.
4. Write 0xE904 to the Command register 0x060 to initiate a block copy.
5. Wait t_{BLOCK} for the copy to complete.
6. Check the CommStat.NVError bit. If set, repeat the process. If clear, continue.
7. Write 0x000F to the Command register 0x060 to send the full reset command to the IC.

8. Wait 10ms for the IC to reset. Write protection resets after the full reset command. At this step, verify that there is no NVError and check whether all nonvolatile memory is correct. If there is an NVError or the register value is wrong, then nonvolatile programming has failed. Restart the whole process.
9. Write 0x0000 to the CommStat register (0x61) twice in a row to unlock write protection.
10. Write 0x8000 to the Config2 register (0x0AB) to reset firmware.
11. Wait for the POR_CMD bit (bit 15) of the Config2 register to be cleared to indicate that the POR sequence is complete.
12. Write 0x00F9 to the CommStat register (0x61) twice in a row to lock write protection.

The IC has a total of seven configuration spaces. If there has been total of seven nonvolatile copy commands sent to the IC, then the nonvolatile configuration memory will be used up. Refer to the Determining the Number of Remaining Updates section in the MAX17320 data sheet for details on how to check the number of remaining configuration spaces.

Setting the SHA Secret for Authentication (MAX17320X12/X22/G12/G22 only)

The SHA secret in the IC cannot be directly read out or written. To initialize the SHA secret, the following sequence is needed:

1. Write 0x0000 to the CommStat register (0x61) twice in a row to unlock write protection.
2. Clear the NVError bit. (Write register 0x61 = 0.)
3. Validate that the secret is all zeros by computing a response with all zeros.
4. If the secret is not all zeros, clear the SHA secret to all zeros. (Write register 0x60 = 0x5A00.)
5. The secret will clear to all zeros after the NVBusy flag clears (t_{UPDATE} = 64ms, typ).
6. Write a challenge to addresses 0xC0 to 0xC9.
7. Send the next secret either with ROM ID (write 0x60 = 0x3300) or without ROM ID (write 0x60 = 0x3000).
8. The new secret will be the last 160 bits of the response.
9. Validate that the internal secret is what is expected by writing a new challenge and validating the response.
10. Send the Lock Secret command (write 0x60 = 0x6000). This lock is irreversible. It will permanently lock the SHA secret, and it will not be changeable. If a multistep secret generation process is used, the lock should only be set at the final step.

Production Test

Hibernate mode should already be disabled in the nonvolatile memory initialization section. If it is not disabled, unlock write protection, then clear HibCfg.EnHib. Ensure that Status2.HibStat is clear and write protection is unlocked before proceeding.

1. Check communication.

   Validate that the IC is powered on by reading the DevName register (0x21). If the IC responds with the correct version number, the communication test is successful.

2. Check voltage measurement.

   Read the Batt register (or the Cell1, Cell2, Cell3, and Cell4 registers for individual cell voltages based on the pack configuration) and compare the measured voltage of the battery pack against the IC readings. If the error is less than 10mV, the voltage measurement check is successful.

3. Check the no load current measurement.

   Check the Current and AvgCurrent registers. The average current should read within 10 LSb.

4. Set the load to 50% of the lesser of the full-scale value of the sense resistor or C/2.

   a. Apply the selected load current.

   b. Read the Current register.

   c. Wait until the Timer register changes (up to 702ms).

   d. The test is successful if the current reading is in an acceptable range of the set load current.

5. Check ODCP protection.

   Apply a current load higher than the overcurrent threshold setting at the pack side. Verify whether the pack-side voltage dropped to 0 within the specified protection time.

6. Check OCCP protection.

   Apply a current-limited supply at the pack side with the current limit set to be over the protection threshold. Make sure the battery simulator or battery can sink the current. Verify whether the charging current stops within the specified protection time.

7. Check OVP protection.

   At the battery side, apply a per-cell voltage greater than the OVP threshold and check whether the external supply at the pack side could charge the battery.

8. Check UVP protection.

   At the battery side, apply a per-cell voltage less than the UVP threshold and verify whether external load at the pack side could load the battery.

9. Check any other optional protections that have been programmed, including imbalance protection.

Calibration

This fuel gauge does not require any calibration for accurate fuel gauging. The voltage, current, and temperature accuracy are trimmed in the Maxim Integrated factory. The algorithm does not require any cycling for accurate state-of-charge reporting.

For special pack-side application with lower than a 2mΩ sense resistor, or if there is requirement for absolute current measurement accuracy or absolute capacity accuracy in additional to fuel-gauge SOC accuracy, you can perform additional calibration procedure as follows.

Preparation for Current Offset Calibration

The current offset calibration requires a long unloaded condition time period. In the production phase, it is best to have a long delay between battery assembly and test and calibration. At the start of battery assembly, the IC's internal timer starts operation. At the same time, the raw coulomb counter starts to accumulate unloaded offset current. When calibrating, the accumulated result of the coulomb counter will be divided by the time elapsed from battery assembly to get the long-time-average offset current value.

Current Calibration Process

There is usually no need to calibrate current offset for sense resistance higher than 3mΩ with a carefully designed sense resistor layout and sensing trace. A good sense resistor layout is typically more important than calibration. Have Maxim review your PCB layout before calibrating for best results.

For complete calibration, you will need:

- Battery pack or supply
- Calibrated ammeter with a 5A range
- Calibrated load box with a 5A range
- MAX17320x EV kit with a USB Micro-B cable
- Most recent official EV kit GUI and a PC with Windows 7 or above

Use the following steps for current offset and current gain calibration:

1. Keep the load off and disconnected. Connect the battery-side supply. Push button S1 to wake up the chip.
2. Read the following four registers together:
   - Timer register (0x6C:0x3E),
   - TimerH register (0x6C:0xBE)
   - QH register (0x6C:0x4D)
   - QL register (0x6C:0x4E)
3. Calculate 32-bit Q = (QH << 16) | QL (Note: Signed two's complement value)
   Calculate 32-bit T = (TimerH << 16) | Timer

   Calculate Offset = Round (- Q/T)

4. Set the COFF register (0x6C:0x2F) to the value of the offset.

   This completes current offset calibration.

5. Set the FilterCfg register (0x6C:0x29) to 0x0EA3. This sets the filtering time constant to 2.8125s.
6. Set the load box to sink at Curr_Test less than the source limit of supply 1 and turn on the load.
7. Read the ammeter reading and denote it as CURRENT_REF (e.g., CURRENT_REF = 4.985A).
8. Wait 0.5s for the MAX17320 to read the current.
9. Read the Current register (0x6C:0x1C) and denote it as CURRENT_INST. Write the CURRENT_INST value to the AvgCurrent register (0x6C:0x1D). This accelerates the averaging filter.
10. Wait 5s, then read the AvgCurrent register. Denote this value as CURRENT_MEAS (e.g., CURRENT_MEAS = -5.001A).

Table 2. nCGAIN Register Format

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Definition	GAIN										OFF					
POR	0b0100000000										0b000000					
POR	0x4000															

For gain, 0b0100000000 is 100%. Scale this value to the desired gain.

11. Calculate the value of CGAIN:

$$raw\_gain = Round\left(\frac{abs(CURRENT\_MEAS)}{abs(CURRENT\_REF)} \times 0b010000000000\right)$$

$$nCGAIN.GAIN = last\ 10\ bit\ of\ (raw\_gain >> 2) + ((raw\_gain\ \&\ 2) >> 1)$$

$$nCGAIN.OFF = last\ 6\ bit\ of\ COFF$$

(The above measurements give raw_gain = 0x03FD.)

This completes current gain calibration.

NVMemory Burn Register: nCGAIN. This sets both CGAIN and COFF permanently.

Conclusion

This application note describes the various steps for implementing the MAX17320X/G in a battery pack. Follow the guide closely during design, evaluation, and production phases, as system circuit design and layout that follows guidance may provide higher measurement accuracy. The memory programming instructions describe how to load the fuel gauge and authentication information and lock it to prevent tampering with the authentication or fuel-gauge mechanisms. For details on software implementation, refer to the **MAX17320 Software Implementation Guide**.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	03/20	Initial release	—