ANALOG-DIGITAL CONVERSION

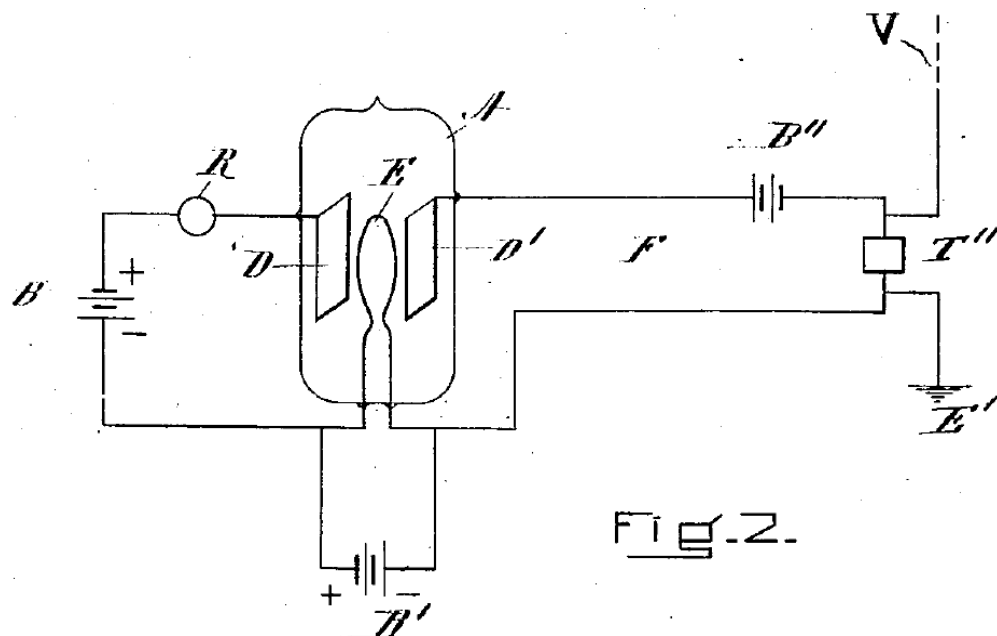# ◪ ANALOG-DIGITAL CONVERSION

CHAPTER 4
DATA CONVERTER PROCESS TECHNOLOGY

SECTION 4.1: EARLY PROCESSES
Walt Kester

Vacuum Tube Data Converters

The vacuum tube was the first enabling technology in the development of data converters—starting in the 1920s and continuing well into the late 1950s. As discussed in Chapter 1 of this book, the vacuum tube was invented by Lee De Forest in 1906 (Reference 1). A figure from the patent is shown in Figure 4.1. Vacuum tubes quickly found their way into a variety of electronic equipment, and the Bell Telephone system began using vacuum tube amplifiers in their telephone plants as early as 1914.

Extracted from: Lee De Forest, "Device for Amplifying Feeble Electrical Currents," *U.S. Patent 841,387*, **Filed October 25, 1906, Issued January 15, 1907**

Figure 4.1: *The Invention of the Vacuum Tube: 1906*

Amplifier development has always been critical to data converter development, starting with these early vacuum tube circuits. A significant contribution was the invention of the feedback amplifier (op amp) by Harold S. Black in 1927 (References 2, 3, 4). Vacuum tube circuit development continued throughout World War II, and many significant

contributions came from Bell Labs. For a detailed discussion of the history of op amps, please refer to Walt Jung's book, *Op Amp Applications* (Reference 5).

In the 1920s, 1930s, 1940s, and 1950s, vacuum tubes were the driving force behind practically all electronic circuits. In 1953, George A. Philbrick Researches, Inc., introduced the world's first commercially available op amp, known as the K2-W (Reference 6). A photo and schematic are shown in Figure 4.2.
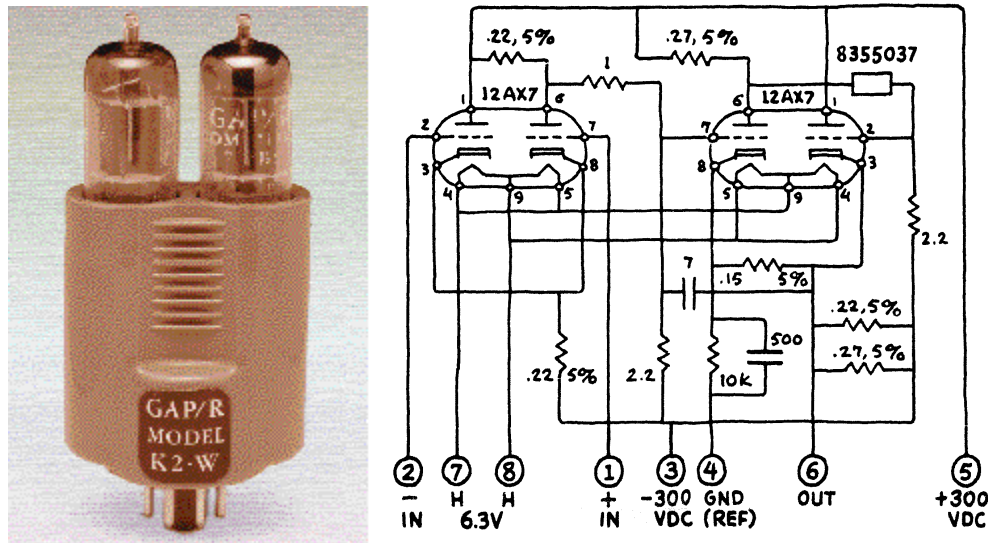

Figure 4.2: *The K2-W Op Amp Introduced in 1953 (Courtesy of Dan Sheingold)*

Pulse code modulation (PCM) was the first major driving force in the development of early data converters, and Alec Hartley Reeves is generally credited for the invention of PCM in 1937. (Reference 7). In his patent, he describes a vacuum tube "counting" ADC and DAC (see Chapter 3 of this book). Data converter development continued at Bell Labs during the 1940s, not only for use in PCM system development, but also in wartime encryption systems.

The development of the digital computer in the late 1940s and early 1950s spurred interest in data analysis, digital process control, etc., and generated more commercial interest in data converters. In 1953 Bernard M. Gordon, a pioneer in the field of data conversion, founded a company called Epsco Engineering (now Analogic, Inc.) in his basement in Concord, MA. Gordon had previously worked on the UNIVAC computer, and saw the need for commercial data converters. In 1954 Epsco introduced an 11-bit, 50-kSPS vacuum-tube based SAR ADC called the DATRAC. This converter, shown in Figure 4.3, is generally credited as being the first commercial offering of such a device. The DATRAC was offered in a 19" × 26" × 15" housing, dissipated several hundred watts, and sold for approximately $8000.00.

While the vacuum tube DATRAC was certainly impressive for its time, solid-state devices began to emerge during the 1950s which would eventually revolutionize the entire field of data conversion and electronics in general.

- 19" × 15" × 26"
- 150 lbs
- 500W
- $8,500.00

Figure 4.3: *1954 "DATRAC" 11-bit, 50-kSPS SAR ADC
Designed by Bernard M. Gordon at EPSCO*

Solid State, Modular, and Hybrid Data Converters

Although the transistor was invented in 1947 by John Bardeen, Walter Brattain, and William Shockley of Bell Labs (References 8, 9, 10, 11), it took nearly a decade for the technology to find its way into commercial applications. The overall reliability of the devices was partly responsible for this, as the first transistors were germanium, and were limited in terms of leakage currents, general stability, maximum junction temperature, and frequency response.

In May of 1954, Gordon Teal of Texas Instruments developed a grown-junction silicon transistor. These transistors could operate up to 150°C, far higher than germanium. Additional processing refinements were to improve upon the early silicon transistors, and eventually lead a path to the invention of the first integrated circuit in 1958 by Jack Kilby of Texas Instruments (Reference 12).

Kilby's work was paralleled by Robert Noyce at Fairchild, who also developed an IC concept in 1959 (Reference 13). Noyce used inter-connecting metal trace layers between transistors and resistors, while Kilby used bond wires. As might be expected from such differences between two key inventions, so closely timed in their origination, there was no instant concensus on the true "IC inventor." Subsequent patent fights between the two inventor's companies persisted into the 1960s. Today, both men are recognized as IC inventors.

In parallel with Noyce's early IC developments, Jean Hoerni (also of Fairchild Semiconductor) had been working on means to protect and stabilize silicon diode and

transistor characteristics. Until that time, the junctions of all mesa process devices were essentially left exposed. This was a serious limitation of the mesa process. The mesa process is so-named because the areas surrounding the central base-emitter regions are etched away, thus leaving this area exposed on a plateau, or mesa. In practice, this factor makes a semiconductor so constructed susceptible to contaminants, and as a result, inherently less stable. This was the fatal flaw that Hoerni's invention addressed. Hoerni's solution to the problem was to re-arrange the transistor geometry into a flat, or planar surface, thus giving the new process its name (see References 14 and 15). However, the important distinction in terms of device protection is that within the planar process the otherwise exposed regions are left covered with silicon dioxide. This feature reduced the device sensitivity to contaminants; making a much better, more stable transistor or IC. With the arrangement of the device terminals on a planar surface, Hoerni's invention was also directly amenable to the flat metal conducting traces that were intrinsic to Noyce's IC invention. Furthermore, the planar process required no additional process steps in its implementation, so it made the higher performance economical as well. As time has now shown, the development of the planar process was another key semiconductor invention. It is now widely used in production of transistors and ICs.

At a time in the early 1960s shortly after the invention of the planar process, the three key developments had been made as summarized in Figure 4.4. They were the *(silicon) transistor* itself, the *IC*, and the *planar process*. The stage was now set for important solid-state developments in data converters. This was to take place in three stages. First, there would be discrete transistor and modular data converters, second there would be hybrid data converters, and thirdly, the data converter finally became a complete, integral, dedicated IC. Of course, within these developmental stages there were considerable improvements made to device performance. And, as with the vacuum tube/solid-state periods, each stage overlapped the previous and/or the next one to a great extent.

◆ **Invention of the (Germanium) transistor at Bell Labs: John Bardeen, Walter Brattain, and William Shockley in 1947.**

◆ **Silicon Transistor: Gordon Teal, Texas Instruments, 1954.**

◆ **Birth of the Integrated Circuit:**
- **Jack Kilby, Texas Instruments, 1958 (used bond wires for interconnections).**
- **Robert Noyce, Fairchild Semiconductor, 1959 (used metallization for interconnections).**

◆ **The Planar Process: Jean Hoerni, Fairchild Semiconductor, 1959.**

Figure 4.4: Key Solid-State Developments: 1947-1959

The first solid-state data converters utilized discrete transistors, few if any ICs, and required multiple PC boards to implement the analog and digital parts of the conversion process. A typical example was the HS-810, 8-bit, 10-MSPS ADC introduced in 1966 by Computer Labs, Inc. and shown in Figure 4.5. One of the PC boards from the HS-810 is

shown in Figure 4.6. (Computer Labs was later acquired by Analog Devices in 1978). The entire converter was built from discrete transistors, resistors, and capacitors, with practically no integrated circuits. The unit was designed to fit in a 19" rack, contained all required power supplies, dissipated over 100 W, and cost over $10,000 at the time of introduction. Data converters such as the HS-810 were primarily used in research applications and in early digital radar receivers.

Figure 4.5: *HS-810, 8-bit, 10MSPS ADC Released by Computer Labs, Inc. in 1966*
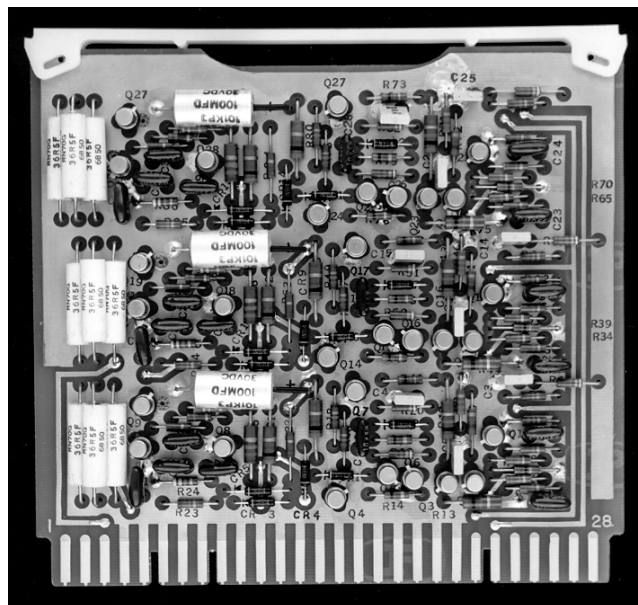

Figure 4.6: *Double-Sided PC Board from HS-810 ADC*

By the late 1960s and early 1970s, various IC building blocks such as op amps, comparators, and digital logic became available which allowed a considerable reduction in parts count in ADCs and DACs. This led to the *modular* data converter—basically various combinations of ICs, transistors, resistors, capacitors, etc., mounted on a small PC board with pins, and encapsulated in a potted plastic case. The potting compound helped to distribute the heat throughout the module, provided some degree of thermal tracking between critical components, and made it a little more difficult for a competitor to reverse engineer the circuit design.

A good example of an early converter module was the Analog Devices' industry-standard ADC12QZ, 12-bit, 40-µs SAR ADC introduced in 1972 and shown in Figure 4.7. The ADC12QZ was the first low-cost commercial general-purpose 12-bit ADC on the market. The converter used the *quad-switch* ICs in conjunction with precision thin film resistor networks for the internal DAC (the quad switch AD550 *µDAC* circuits are discussed in more detail in Chapter 3 of this book).

Figure 4.7: *ADC-12QZ General Purpose 12-Bit, 40-µs SAR ADC Introduced in 1972*

Another popular process for data converters that had its origins in the 1970s is the *hybrid*. Hybrid circuits are typically constructed using un-encapsulated die, or "chips," such as ICs, resistors, capacitors, etc., which are bonded to a ceramic substrate with epoxy—in some cases, eutetically bonded. The bond pads on the various chips are connected to pads on the substrate with wire bonds, and interconnections between devices are made with metal paths on the substrate, similar in concept to a PC board. The metal conductor paths are either thick film or thin film, depending upon the process and the manufacturer. For obvious reasons, hybrid technology is often referred to as "chip-and-wire." After assembly, the package is sealed in an inert atmosphere to prevent contamination.

Various technologies are used to construct hybrids, including thick and thin film conductors and resistors, and the devices tend to be rather expensive compared to ICs. The AD572 12-bit, 25-µs ADC released by Analog Devices in 1977 is an excellent example of a hybrid and is shown in Figure 4.8. It is significant that the AD572 was the first 12-bit hybrid ADC circuit to obtain MIL-883B approval.
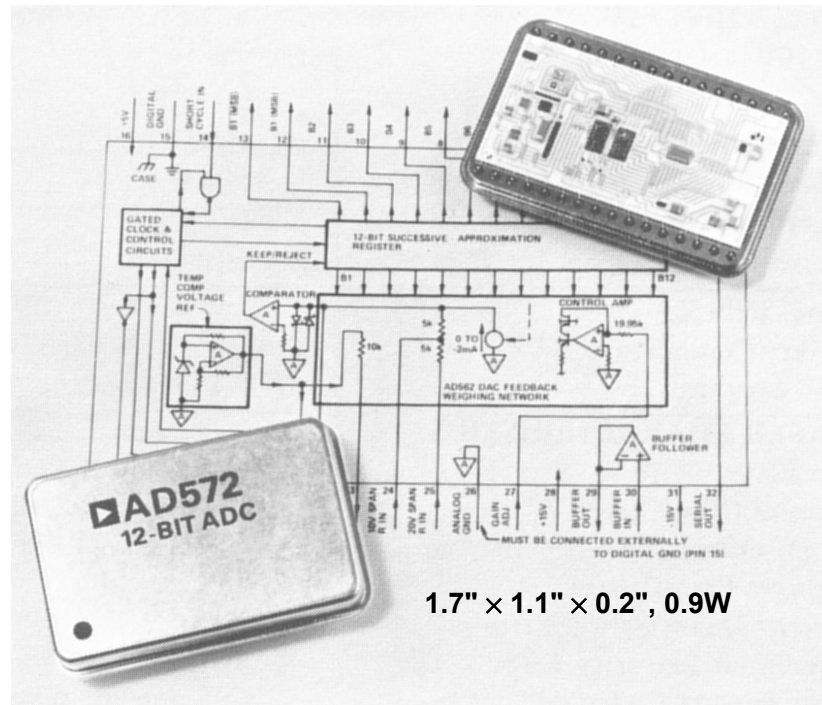
1.7" × 1.1" × 0.2", 0.9W

Figure 4.8: *AD572 12-Bit, 25-µs ADC, 1977*

The chief motivation behind modules and hybrids was to produce data converters with speed and resolution not achievable with the early IC processes. Hybrid circuit designers could choose from a variety of discrete PNP, NPN, and FET transistors, IC op amps, IC comparators, IC references, IC DACs, IC logic, etc. Coupled with the ability to perform active in-circuit laser trimming of resistors, the hybrid circuits could achieve relatively high levels of performance compared to what was possible in ICs alone. Customers were willing to pay premium prices for the hybrids, because that was the only way to achieve the desired performance. Also, there was usually a period of at least several years before the equivalent function was achievable in completely monolithic form, thereby giving a hybrid a reasonable product life cycle.

Today, however, the situation is reversed—the speed and resolution of modern IC data converters is generally limited by internal process-related parasitics, and these parasitics are much smaller than could ever be achieved in an equivalent hybrid circuit. In other words, it would be impossible to duplicate the performance of most modern IC data converters using conventional hybrid technology. For these reasons, hybrids today serve relatively small niche markets today, such as dc-to-dc and synchro-to-digital converters.

Note the distinction between chip-and-wire hybrids and modern *multichip modules* (MCMs) which basically use surface-mount ICs and other components on small multilayer PC boards to achieve higher levels of functionality than possible in a single IC.

It is also important to distinguish chip-and-wire hybrids and multichip modules from another IC packaging technology—usually referred to as *compound monolithic*—where

two die (usually an analog IC and a digital IC) are mounted on a single lead frame, electrically connected with wirebonds, and encapsulated in a plastic IC package.

Calibration Processes

Nearly all data converters require some calibration to ensure overall INL, DNL, gain, and offset errors are within specified limits. For low resolution converters, the accuracy and matching of the various circuit components may be sufficient to ensure this. For high resolution converters (greater than 10-bits or so), methods must generally be provided to accomplish various types of trims. The early rack-mounted and PC board data converters generally used potentiometers and/or selected precision resistors to accomplish the required calibration. In many cases, a precision resistor in the circuit was "padded" with a larger parallel resistor to achieve the desired value.

Modular data converters achieved their accuracy either by using pre-trimmed ICs and precision resistor networks as building blocks, or by manually selecting resistors prior to potting. An interesting trim method was used in the popular DAC-12QZ—the first modular 12-bit DAC which was introduced in 1970. It utilized thick film resistors that were trimmed to the appropriate values by sandblasting.

Because modular data converters had to be calibrated before potting, the effects of the thermal shifts due to potting had to be factored into the actual trim process.

Hybrid circuits generally utilized a variety of types of trimming processes, depending upon the process and the manufacturer. Again, the use of pre-trimmed IC building blocks, such as the AD562 or AD565 IC DAC, minimized substrate-level trimming requirements in such products as the AD572 mentioned previously. Other popular methods included functional laser trimming of thick or thin film resistors on the substrate. These trimmed resistors could be in the form of deposited substrate resistors or resistor networks bonded to the substrate. Both thick and thin film resistor technology was utilized, although thin film resistors generally had better stability.

REFERENCES:
4.1 EARLY PROCESSES

1. Lee De Forest, "Device for Amplifying Feeble Electrical Currents," **U.S. Patent 841,387**, filed October 25, 1906, issued January 15, 1907 *(The triode vacuum tube, or 'Audion', the first amplifying device)*.

2. H. S. Black, "Wave Translation System," **U.S. Patent 2,102,671**, filed August 8, 1928, issued December 21, 1937 *(The basis of feedback amplifier systems)*.

3. H. S. Black, "Stabilized Feedback Amplifiers," **Bell System Technical Journal**, Vol. 13, No. 1, January 1934, pp. 1-18 *(A practical summary of feedback amplifier systems)*.

4. Harold S. Black, "Inventing the Negative Feedback Amplifier," **IEEE Spectrum**, December, 1977 *(Inventor's 50th anniversary story on the invention of the feedback amplifier)*.

5. Walter G. Jung, **Op Amp Applications**, Analog Devices, 2002, ISBN 0-916550-26-5.

6. Data Sheet For Model K2-W Operational Amplifier, George A. Philbrick Researches, Inc., Boston, MA, January 1953. See also "40 Years Ago," **Electronic Design**, December 16, 1995, pp. 8. *(The George A. Philbrick Research dual triode K2-W, the first commercial vacuum tube op amp)*.

7. Alec Harley Reeves, "Electric Signaling System," **U.S. Patent 2,272,070**, filed November 22, 1939, issued February 3, 1942. Also **French Patent 852,183** issued 1938, and **British Patent 538,860** issued 1939. *(the ground-breaking patent on PCM. Interestingly enough, the ADC and DAC proposed by Reeves are counting types, and not successive approximation)*.

8. Ian M. Ross, "The Foundation of the Silicon Age," **Bell Labs Technical Journal**, Vol. 2, No. 4, Autumn 1997.

9. C. Mark Melliar-Smith et al, "Key Steps to the Integrated Circuit," **Bell Labs Technical Journal**, Vol. 2, No. 4, Autumn 1997.

10. J. Bardeen, W. H. Brattain, "The Transistor, a Semi-Conductor Triode," **Physical Review**, Vol. 74, No. 2, July 15, 1947 pp. 230-231 *(the invention of the germanium transistor)*.

11. W. Shockley, "The Theory of p-n Junctions in Semiconductors and p-n Junction Transistors," **Bell System Technical Journal**, Vol. 28, No. 4, July 1949, pp. 435-489 *(theory behind the germanium transistor)*.

12. J. S. Kilby, "Invention of the Integrated Circuit," **IRE Transactions on Electron Devices**, Vol. ED-23, No. 7, July 1976, pp. 648-654 *(Kilby's IC invention at TI)*.

13. Robert N. Noyce, "Semiconductor Device-and-Lead Structure," **U.S. Patent 2,981,877**, filed July 30, 1959, issued April 25, 1961 *(Noyce's IC invention at Fairchild)*.

14. Jean A. Hoerni, "Method of Manufacturing Semiconductor Devices," **U.S. Patent 3,025,589**, filed May 1, 1959, issued March 20, *1962 (the planar process—a manufacturing means of protecting and stabilizing semiconductors)*.

15. Jean Hoerni, "Planar Silicon Diodes and Transistors," **IRE Transactions on Electron Devices**, Vol. 8, March 1961, p. 168 *(technical discussion of planar processed devices)*.

NOTES:

SECTION 4.2: MODERN PROCESSES
Walt Kester, James Bryant

Bipolar Processes

The basic bipolar IC process of the 1960s was primarily optimized to yield good NPN transistors. However, low beta, low bandwidth PNP transistors were available on the process—the *lateral* PNP and the *substrate* PNP. Clever circuit designers were able to use the PNPs for certain functions such as level shifting and biasing. Bob Widlar of Fairchild Semiconductor Corporation was one of these early pioneers, and designed the first monolithic op amp, the µA702, in 1963. Other op amps followed rapidly, including the µA709 and the industry-standard µA741. Another Widlar design, the µA710/µA711 comparator, was introduced in 1965. These types of linear devices, coupled with the introduction of the 7400-series TTL logic, provided some of the key building blocks for the modular and hybrid data converters of the 1970s. For more details of the history of op amps, please refer to Walt Jung's excellent book, *Op Amp Applications* (Reference 1).

Analog Devices was founded in 1965 by Ray Stata and Matt Lorber, and focused its early efforts on precision modular amplifiers. In 1969, Analog Devices acquired Pastoriza Electronics, then a leader in data conversion products—thereby making a solid commitment to both data acquisition and linear technology. In 1971, Analog Devices acquired a small IC company, Nova Devices of Wilmington, MA, and this later led to many monolithic linear and data converter products.

Thin Film Resistor Processes

There is another process technology which does deserve special mention, since it is crucial to the manufacture of many linear circuits and data converters requiring stable precision resistors and the ability to perform calibrations. This is thin film resistor technology.

Analog Devices began its efforts to develop thin film resistor technology in the early 1970s. Much effort has been spent to develop the ability to deposit these stable thin film resistors on integrated circuit chips, and even more effort to laser trim them at the wafer level. They have temperature coefficients of <20 ppm/°C and matching to within 0.005%. The resistors can be made to match to within 0.01% or better without laser trimming, but to achieve this they must be relatively large—in practice if resistors must match to better than 0.1% or 0.05%, it is more economical to laser trim them than to design them to meet the specification without trimming.

It is interesting to note that although it is possible to make these resistors very precise (ratiometrically), they usually have quite wide tolerances. The reason is economic—most applications require precision matching and low temperature coefficient but do not actually need very high absolute precision. It is possible to optimize all three, but much less expensive to optimize two out of three—so this is what is usually done.

Many of the precision resistors used in the various data converters are laser trimmed SiCr thin film resistors, although the new submicron and non-volatile memory processes make laser trimming unnecessary in many new data converters, where it would have been unavoidable in earlier generations.

In summary, the bipolar process, coupled with thin film resistors and laser wafer trim technology, led to the proliferation of IC data converters during the 1970s, 1980s, and 1990s. For example, the AD571 was the first complete monolithic 10-bit SAR ADC designed by Paul Brokaw and was introduced in 1978. The AD571 used a bipolar process with integrated-injection-logic (I^2L) as well as thin film laser wafer trimmed resistors. I^2L geometries were made to use a set of diffusions compatible with high performance linear transistors (Reference 2). The AD571 was soon followed by other converters, such as the industry-standard AD574 12-bit ADC in 1980. In addition, the IC converters provided building blocks for high performance modular and hybrid converters during the same period.

Complementary Bipolar (CB) Processes

Although clever IC circuit designers made the best use possible of the poor quality substrate and lateral PNP transistors available on the NPN-based bipolar processes of the 1970s and 1980s, the lack of matching high bandwidth PNP transistors definitely limited circuit design options in linear ICs, especially high speed op amps.

In the mid 1980s, Analog Devices developed the world's first p-epi complementary bipolar (CB) process, and the AD840-series of op amps was introduced starting in 1988. The f_ts of the PNP and NPN transistors in this first-generation 36-V CB process were approximately 700 MHz and 900 MHz, respectively. Since the introduction of the original CB process, several generations of faster CB processes have been developed at Analog Devices designed for even higher speeds with lower breakdowns. Descriptions of the ground-breaking first-generation CB process can be found in References 3 and 4.

Analog Devices' CB processes all have JFETs, allowing high input impedance op amps as well as sample-and-hold amplifiers for data converters. The dielectrically isolated "XFCB" process provided real breakthroughs in speed and distortion performance. Introduced in 1992, this process yields 3-GHz PNPs and 5-GHz matching NPNs. The "XFCB 1.5" process has 5-GHz PNPs and 9-GHz NPNs. A 5-V "XFCB 2" process has 9-GHz PNPs and 16-GHz NPNs.

The XFCB process (and later generations) has been used to produce several notable high-end data converters. For example, the AD9042, designed by Roy Gosser and Frank Murden and introduced in 1995, was the first low distortion 12-bit, 41-MSPS ADC on the market, with greater than 80-dBc SFDR over the Nyquist bandwidth. The AD9042 was followed by several additional XFCB converters, including the AD6645 14-bit, 80-/105-MSPS ADC which was introduced in 2001, with 90-dBc SFDR and 75-dB SNR. Both the AD9042 and the AD6645 use laser wafer trimming to achieve their high level of performance.

CMOS Processes

Metal-on-silicon (MOS) devices had their origins in late 1950s and early 1960s in the pursuit of a process tailored for digital devices. The first complementary-metal-oxide-semiconductor (CMOS) devices began to appear in the mid-1960s, and provided both P-channel and N-channel MOS devices on the same process. CMOS offered the potential of much higher packing density and lower power than TTL (bipolar-based) devices, and soon became the IC process of choice for complex VLSI digital devices. The same advances in technology that have enabled cheap, powerful, low-power consumption processors with large memory to revolutionize mobile telephony, portable computing and many other fields have also revolutionized data converters.

Data converter designers soon realized the advantages of using CMOS for ADCs and DACs. As discussed in Chapter 7 of this book, CMOS switches make ideal building blocks for data acquisition systems. In addition, CMOS offers the ability to add digital functionality to data converters without incurring significant cost, power, and size penalties.

In 1974, Analog Devices combined its thin film technology with CMOS to produce the first 10-bit multiplying CMOS DAC, the AD7520, designed by Jim Cecil and Hank Krabbe. In 1976, Analog Devices established a CMOS IC design and manufacturing operation in Limerick, Ireland, and rapidly introduced many more general purpose CMOS DACs and ADCs starting in the 1970s and continuing to this day.

Although CMOS is capable of making high density low power logic very efficiently and can make excellent analog switches, it is not quite as suitable for amplifiers and voltage references as bipolar processes. These considerations caused process technologists to combine bipolar and CMOS processes to achieve both low power high density logic and high accuracy low noise analog circuitry on a single chip. The resulting processes are more complex, and therefore more expensive, than simple bipolar and CMOS processes, but do have better mixed-signal performance. They include BiMOS processes, which are basically bipolar processes to which CMOS structures have been added, and linear compatible CMOS (LC²MOS or LCCMOS), which is basically CMOS with added bipolar capability. Analog Devices' Limerick facility in Ireland began introducing data converters, switches, and multiplexers using its own proprietary LC^2MOS process in the mid-1980s.

However, the compromises necessary to combine features mean that neither BiMOS nor LC^2MOS offers quite as good performance as its senior parent process does in its own speciality. Thus BiMOS and LC^2MOS have not replaced bipolar, complementary bipolar, or CMOS technology, but designers now have four processes to choose from when designing a data converter.

Modern submicron CMOS technology is cheap, fast and low powered. It is also precise—the same techniques that enable submicron features in logic and memory ICs allow us to manufacture matched resistors and capacitors which are smaller, cheaper and more accurately matched without subsequent trimming than has hitherto been possible, and to make switches with lower leakage, lower on-resistance and less stray capacitance. These advances on their own enable the manufacture of smaller, faster, cheaper and lower powered DACs and ADCs and the integration of complex devices which would have been too big to put on a chip a few years ago. The technology brings an additional bonus—logic made with these processes is so small, cheap and low powered that incorporating auto-calibration and other computational features to improve data converter performance and accuracy is virtually free.

Cheap, reliable, non-volatile memory is another recent process innovation which improves the performance of new generation data converters. Gain, offset and even linearity can be adjusted after the chip has been packaged (so packaging stresses will not affect accuracy), at a cost far lower than that of laser trimming. Many data converters trimmed in this way are "locked" before leaving the factory so that the calibration cannot be damaged accidentally—and so the user cannot trim them to his system's requirements. However, the same technology does allow users to store calibration coefficients and similar data. Other converters allow for periodic self-calibrations for gain, offset, and even linearity errors. Various types of "fuse blowing" or "link trimming" techniques are quite often used in the calibration process rather than more expensive thin film laser wafer trimming.

One feature of these new submicron CMOS processes which is both a benefit and a problem is that they have low breakdown voltage and must operate on low voltage supplies: 0.6-μm CMOS uses 5 V, and less for the smaller geometry processes (0.35 μm ~ 3.3 V, 0.25 μm ~ 2.5 V, 0.18 μm ~ 2 V, 0.15 μm ~ 1.5 V, and 0.13 μm ~ 1 V). This makes them virtually useless with the traditional precision analog supplies of ±15 V. They will, however, operate accurately and at high speed on the lower supply voltages, making them convenient for low power circuitry. However, this reduces their dynamic range, as their fullscale output is closer (in the case of 3-V single supply circuitry 20-dB closer) to the noise floor.

For high speed data converters, however, the reduced signal amplitude can be an advantage, because it is generally much easier to drive low amplitude signals with low distortion into 50-Ω or 75-Ω loads than larger amplitude signals. The optimum amplitude for the best compromise between noise and distortion generally ranges between 1-V and 2-V peak-to-peak in communications-oriented data converters, although there are some exceptions to this.

A brief summary of data converter processes is given in Figure 4.9.

◆ **NPN-Based bipolar**

◆ **NPN-Based bipolar with JFETs and LWT thin film resistors**

◆ **NPN-Based Bipolar with Integrated Injection Logic (I^{2}L) and LWT thin film resistors**

◆ **Complementary Bipolar (CB) with JFETs and LWT thin film resistors**

◆ **Dielectrically Isolated Complementary Bipolar with JFETS and LWT thin film resistors**

◆ **CMOS**

◆ **CMOS and LWT thin film resistors**

◆ **LC^{2}MOS and BiCMOS with LWT thin film resistors**

◆ **Hybrid (chip-and-wire)**

◆ **Multichip Module (MCM)**

◆ **GaAs, SiGe**

Figure 4.9: Data Converter Processes

Data Converter Processes and Architectures

In the last decade, CMOS has become a dominant process for data converters—replacing more expensive bipolar laser wafer trimmed devices. Submicron CMOS has extremely low parasitic resistance, capacitance, and inductance, and is ideal for a number of data converter architectures, including successive approximation, Σ-Δ, and pipeline. The fine-line lithography techniques associated with submicron processes allow excellent matching between capacitors in a capacitor DAC (a fundamental building block for SAR ADCs). The internal capacitor DACs are then trimmed by adding or subtracting small parallel capacitors using either some form of fuse blowing, link trimming, or autocalibration routine utilizing volatile memory. The addition of analog input multiplexers to form a complete data acquisition system is also relatively easy due to the high quality switches and multiplexers available in CMOS.

CMOS is also the process of choice for all types of Σ-Δ ADCs and DACs, which are also based on switched capacitor circuits. In addition, the Σ-Δ architecture is highly digitally intensive—another reason for utilizing the packing density and low power of CMOS. Statistical matching techniques are popular in the multibit Σ-Δ data converters as a means for higher resolution and dynamic range without the need for trimming.

For high speed pipelined ADCs, the digital capability of CMOS is ideal to perform the required error correction. Fully differential circuit design techniques, coupled with the high speed switched capacitor capabilities of CMOS, produce excellent performance.

CMOS is also excellent for high speed communications DACs, as exhibited in the Analog Devices' TxDAC family with resolutions up to 16 bits and speeds of several hundred MHz. To illustrate the progression of DAC performance over the last decade,

Figure 4.10 shows update rate moving from less than 30 MSPS in 1994 to nearly 1 GSPS in 2004. This is primarily due to the reduction in parasitic capacitance, inductance, and resistance associated with the smaller and smaller submicron processes. Figure 4.11 shows a similar plot for SFDR (10-MHz output signal), which has increased from 50 dBc in 1994 to nearly 90 dBc in 2004.
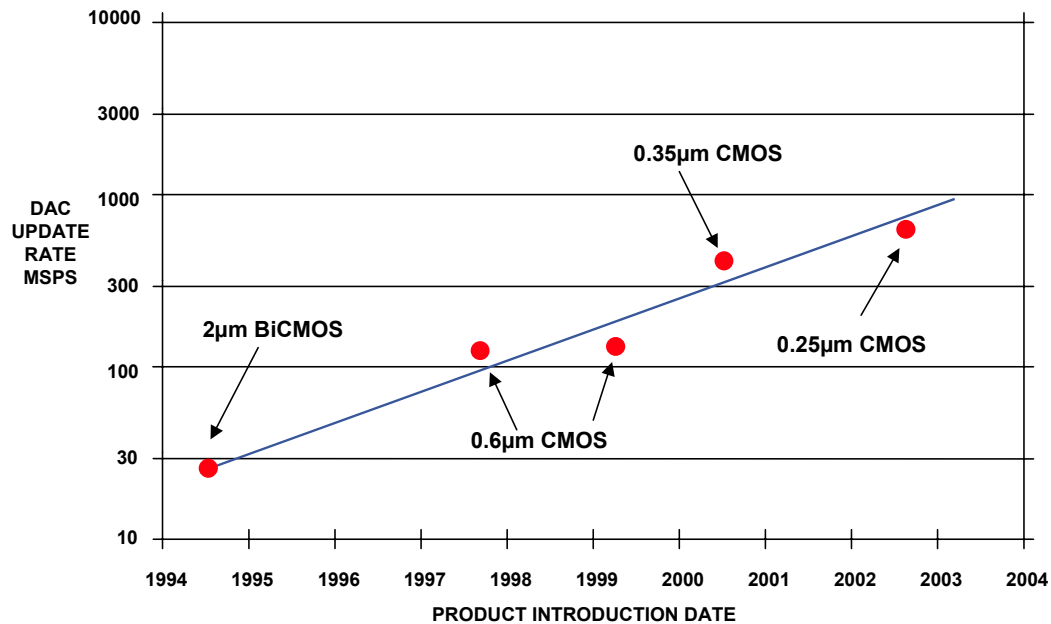

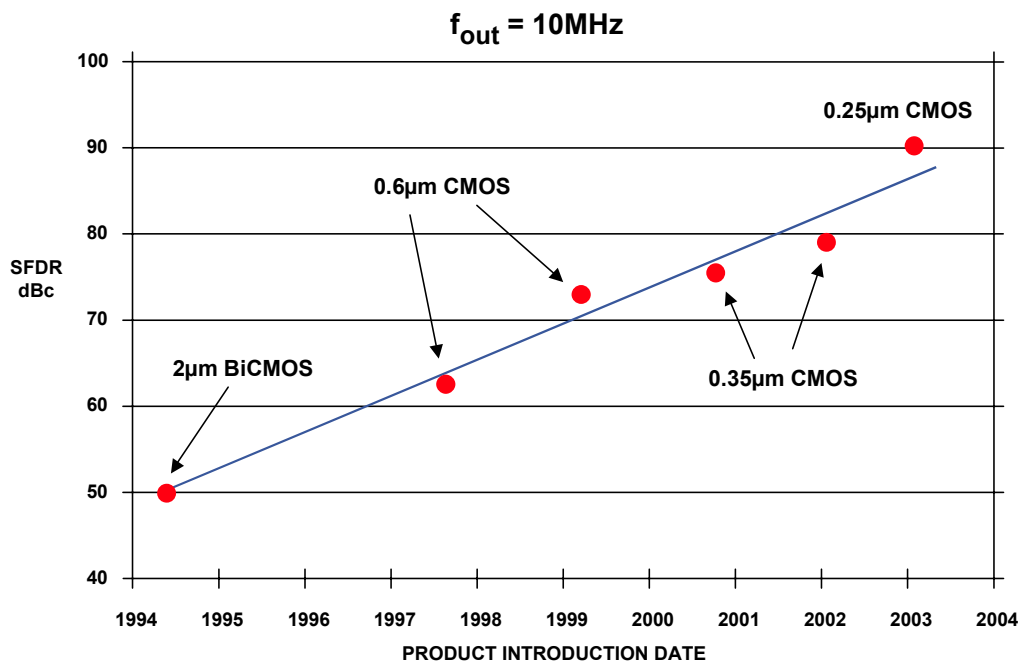**Figure 4.10:** *High-Speed DAC Update Rate Trend*

Figure 4.11: *High-Speed DAC SFDR Performance Trend*

The trend in modern data converters is to add much more digital functionality, such as digital filtering, multiplexing, decoding, modulation, etc., and CMOS is the ideal process for this.

As mentioned earlier, analog building blocks such as amplifiers, mixers, and voltage references designed in CMOS cannot achieve the levels of performance attainable in bipolar, hence the need for a process that combines bipolar with CMOS, or BiCMOS. BiCMOS processes are more expensive, but are useful where an ADC with an extremely high performance analog front end is required. Functions such as mixers, sample-and-holds, input buffer amplifiers, and accurate voltage references can be implemented in bipolar, while the digital portion of the data converter is CMOS.

Multichip modules offer the flexibility of combining various IC technologies to perform functions otherwise not possible in all-monolithic parts. For instance, high performance RF analog front ends can be tuned to match the input impedance of IC ADCs, and thereby increase overall bandwidth. Another example is the use of digital post processing using FPGAs to effectively increase the sampling frequency by time interleaving several ADCs (see Chapter 8 of this book for further discussions on this topic). Modern multichip modules are typically constructed on small low-cost PC boards using surface mount components and offer enhanced performance in less real estate than would be required by discrete components.

The role of *Gallium Arsenide* (GaAs) in modern data converters is limited to 6-bit to 8-bit >1-GSPS flash converters and 6-bit to 10-bit DACs. These devices are high in both cost and power and serve small niche markets.

Silicon Germanium (SiGe) offers little as a stand-alone data converter process, but combined with CMOS, could allow the integration of RF front ends along with the data converter function. However, these products would probably be very application specific, as greater flexibility can probably be achieved with the devices in separate packages. (Refer to the next section for a general discussion of the related issue of "smart partitioning").

A brief summary of data converter processes and how they relate to various architectures is given in Figure 4.12.

Finally, no discussion on data converter processes would be complete without touching upon the issue of packaging. In the last decade, there has been an increase in the demand for small, low cost, high performance, surface mount packages suitable for mass production using automated assembly techniques. Today this is possible, primarily because of the lower power and small die size associated with modern submicron processes. Many devices are suitable for packages such as those shown in Figure 4.13, which are representative of today's trends. Smaller chip-scale-packaged (CSP) devices are available when required, and ball-grid-array (BGA) packages are useful for high pin-count, high-speed devices.

◆ **CMOS:**
- ● **Ideal for switched capacitor SAR, Σ-Δ, Pipelined**
- ● **Additional digital functionality**
- ● **Volatile and non-volatile trimming at package level**

◆ **BiCMOS**
- ● **Useful if analog front-end requires extremely high performance**
- ● **Amplifiers, mixers, SHAs, highly accurate voltage references**

◆ **Calibration processes**
- ● **LWT, fuse blowing, link trimming, volatile and non-volatile memory, autocalibration**

◆ **Multichip Module**
- ● **Multiple ADCs and DACs, analog front ends, digital post processing**

◆ **GaAs**
- ● **6, 8-bit GHz flash ADCs, high power and cost**

◆ **SiGe**
- ● **Could be useful combined with CMOS**

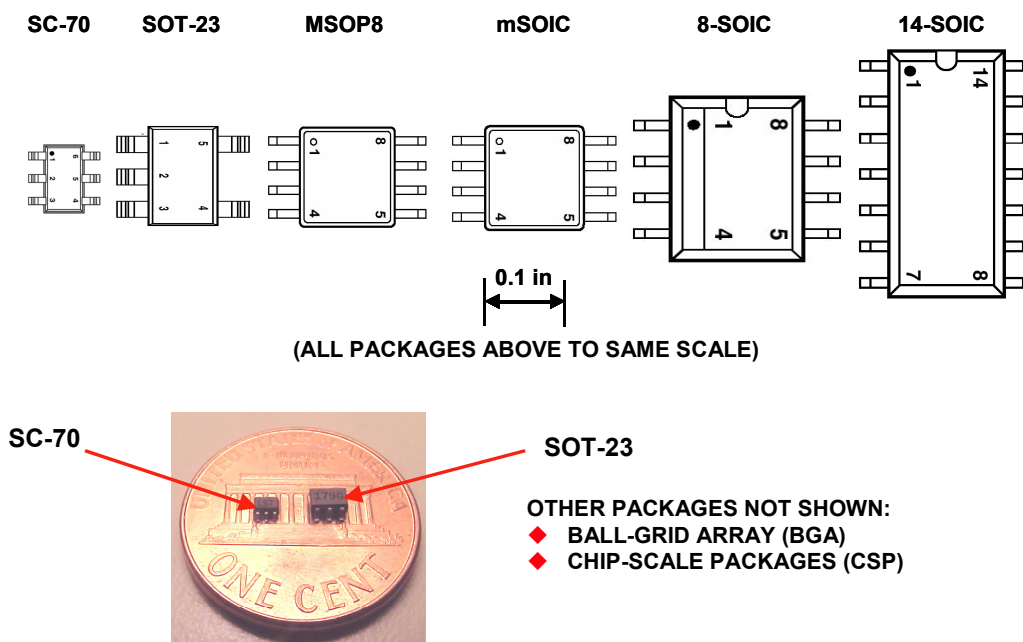*Figure 4.12: Data Converter Processes and Architectures*

Figure 4.13: Examples of Modern Data Converter Packages

When power dissipation becomes significant, larger packages come equipped with built-in heatsinking "slugs" or "epads," which can be soldered directly to the PC board ground plane to effectively dissipate the heat. The use of high speed serial interfaces is also an important trend in reducing the total package pin count to maintain small package profiles.

REFERENCES:
4.2 MODERN PROCESSES

1.   Walter G. Jung, **Op Amp Applications**, Analog Devices, 2003, ISBN 0-916550-26-5. *(The first chapter on op amp history is complete with numerous references to patents, articles, etc.)*.

2.   A. Paul Brokaw, "A Monolithic 10-Bit A/D Using I^{2}L and LWT Thin-Film Resistors," **IEEE Journal of Solid State Circuits**, Vol. SC-13, December 1978, pp. 736-745.

3.   "Op Amps Combine Superb DC Precision and Fast Settling," **Analog Dialogue**, Vol. 22, No. 2, 1988 *(The AD846 IC op amp, the AD840 series, and the high speed CB process used)*.

4.   Jerome F. Lapham, Brad W. Scharf, "Integrated Circuit with Complementary Junction-Isolated Transistors and Method of Making Same," **U.S. Patent 4,969,823**, filed May 5, 1988, issued Nov. 13, 1990. *(Design of the ADI CB IC process)*.

ACKNOWLEDGEMENTS

NOTES:

SECTION 4.3
SMART PARTITIONING
Dave Robertson, Martin Kessler

When Complete Integration Isn't the Optimal Solution

For 30 years, the main path to "smaller, faster, better, cheaper" electronic devices has been through putting more and more of a given system onto a single chip. Large rewards were reaped by those companies that could overcome the various technologic barriers to integration, providing more functionality on a single chip. But as we enter the very deep submicron age, we are approaching some important physical limitations that will change the cost and performance tradeoffs that designers have traditionally made.

As we approach the limits of practical reduction in feature size, it will increasingly turn out that a two-chip design will be smaller, faster, better, cheaper than a single, integrated solution. The key in these cases will be selecting the boundary between these chips. Although high levels of integration will continue to be a feature of the most advanced systems, reaching the optimum in cost and performance will no longer be a simple case of steadily increasing integration. Rather, progress will be measured by changes in circuit partitioning that enable system improvements.

There are several examples of this partitioning already evident today. For instance, large amounts of memory are generally cheaper to implement as a separate DRAM chip than to embed into a microprocessor. It is important to note that as integration barriers emerge, we will not step back to the days where the design model was "analog on one chip, digital on another, memory on a third." Chip partitioning will be done along boundaries that optimize the flow of signal information, as well as augment the intellectual property strengths of the chip providers. It will not be a simple case of "dis-integration." Instead, the best systems will reflect carefully considered integration, facilitating a "smart partitioning."

What makes one partitioning "smarter" than another? There are several important factors to consider:

- *Supply Voltage*—Each advance in lithography brings with it a reduced supply voltage. While this generally helps to lower the power in digital circuits, a lower supply voltage can actually cause power dissipation to increase for high-performance analog circuits. Lower supply voltages also force the use of smaller signal swings, making it difficult to maintain good signal-to-noise ratios. Many systems will look to implement critical analog functions on technologies that support a higher supply voltage as is being done today in cable modem line drivers.

- *Pin Count*—This still drives package/assembly cost as well as board area, so it is desirable to partition systems in a way that minimizes the number of chip-to-chip interconnections. For example, simple digital-to-analog converter (DAC) functions can still be best integrated onto the digital chip if it allows a single analog output pin rather than a full 12-line digital bus.

- *Interface Bandwidth*—A digital bus running at 500 MHz dissipates more power and generates more EMI than a digital bus running at 5 MHz. Wherever possible, the system should be partitioned across buses running at modest rates; in some cases, the data flow can even be carried as a serial bus, thereby also saving pins. Often, this means putting a large amount of digital processing on an otherwise "analog" chip. Examples of this include decimation filters on analog-to-digital-converters (ADCs), interpolation filters on DACs, and Direct Digital Synthesis with integrated DACs. Low voltage differential signaling (LVDS) can be used for high-speed interfaces (>200 MHz). LVDS provides better signal integrity and lower power dissipation at higher frequencies than a standard CMOS interface but doubles the pin count due to its differential nature.

- *Testability and Yield*—Some levels of integration are technically possible, but a poor choice from a manufacturability perspective. Integrating a finicky function with yield issues onto a very large chip means one is forced to throw the entire large chip away each time the function fails a test-which can be very expensive. It is far more cost effective to segregate the function that is subject to yield fallout.

- *External Components*—When considering integration, it is important to factor in not only the ICs, but also the external passive components (capacitors, inductors, SAW filters, etc.). In many cases, an innovative architecture coupled with smart partitioning can provide significant savings in external components, leading to much smaller form-factor and manufacturing costs. One example is illustrated in Figure 4.14 with ADI's OTHELLO® direct-conversion chipset. The multimode cellular handset chipset combines circuit innovation with system understanding and smart partitioning to create a breakthrough in form factor, performance and power saving.
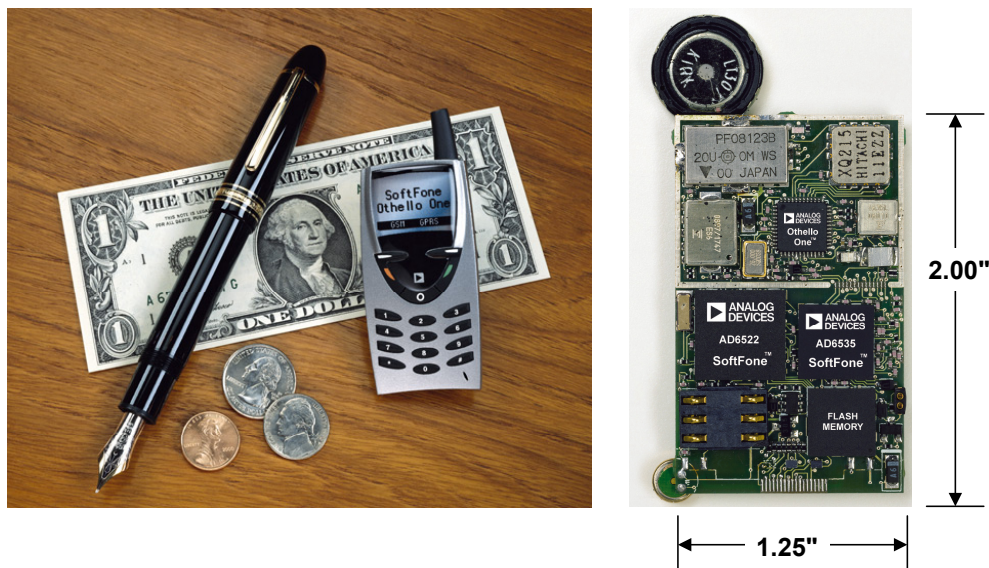

Figure 4.14: *Othello Direct Conversion Radio*

- *Flexibility*—For the highest volume applications, a completely optimized solution is generally provided in the form of full-custom ASICs. However, the vast majority of applications never reach the run rate that justifies a fully committed integrated circuit solution. In this case, the designer will look for the highest levels of integration and performance available-often leveraging neighboring high-volume applications—and will fill in around these with FPGA or other programmable solutions to customize to the application. Examples include the use of TV tuners in cable modem boxes and the use of cell phone handset chipsets in some low-end base stations.

- *Cost*—As CMOS fabrication processes move to finer geometries, digital circuits shrink dramatically and become more cost efficient despite higher silicon wafer costs (see Figure 4.15). Analog circuitry however, as illustrated in Figure 4.16, does not shrink as significantly when migrating to finer process geometries. It may in fact even grow in size to maintain performance. At finer process geometries, the overall digital per-function cost decreases while the overall analog per-function cost increases. Moreover, chips that integrate digital with analog functions may experience significantly higher yield losses than pure digital chips.
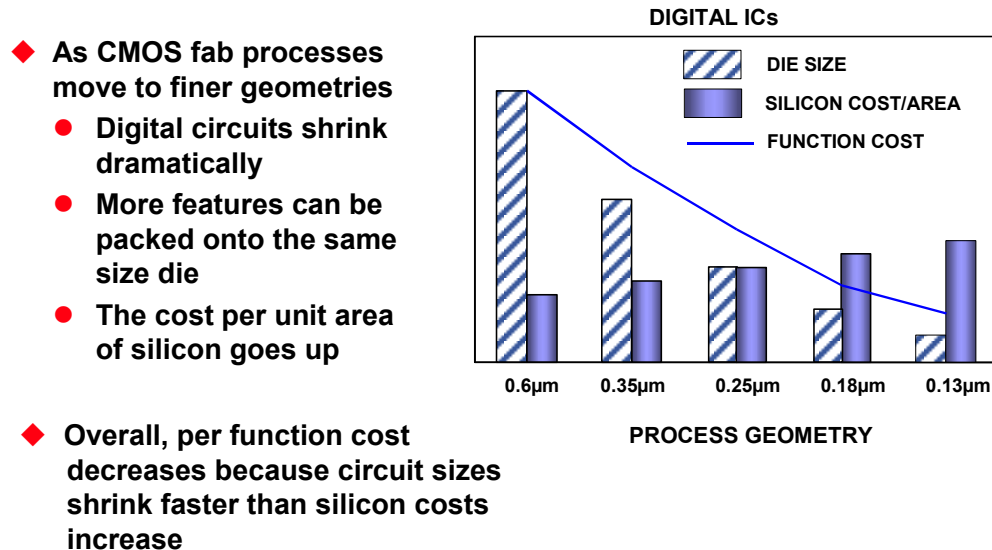
DIGITAL ICs

- ◆ **As CMOS fab processes move to finer geometries**
  - ● **Digital circuits shrink dramatically**
  - ● **More features can be packed onto the same size die**
  - ● **The cost per unit area of silicon goes up**

  DIE SIZE
  SILICON COST/AREA
  FUNCTION COST

- ◆ **Overall, per function cost decreases because circuit sizes shrink faster than silicon costs increase**

0.6µm   0.35µm   0.25µm   0.18µm   0.13µm

PROCESS GEOMETRY

Figure 4.15: *Fab Process Geometry Effects on Cost of Digital ICs*

Smart partitioning separates analog and mixed-signal circuits from pure digital circuitry for cost optimization (see Figure 4.17). An example of such a partitioning is demonstrated in Figure 4.18 with a set-top-box chip-set that can also provide cable-modem functionality. The high-density digital ASIC is separated from the analog or mixed-signal components. All ADCs and DACs are integrated with front-end digital functions like interpolator, DDS and modulator into a single, mixed-signal front-end, the AD9877/AD9879 from Analog Devices.

4.23

◆ **As CMOS processes shrink below 0.25μm**
  - **Analog circuitry does not shrink significantly**
  - **It may in fact grow to maintain performance**
  - **Issues of supporting signal dynamic range arise with decreasing supply voltages**

◆ **Designing high performance analog circuits gets harder and takes longer**

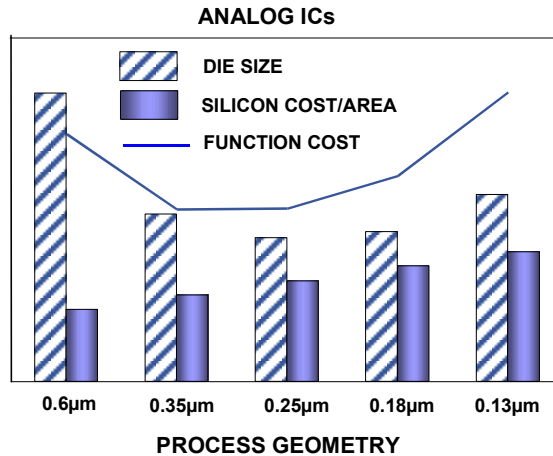◆ **Overall, per function cost increases!!**

ANALOG ICs

DIE SIZE

SILICON COST/AREA

FUNCTION COST

| 0.6μm | 0.35μm | 0.25μm | 0.18μm | 0.13μm |

PROCESS GEOMETRY

Figure 4.16: *Fab Process Geometry Has a Different Effect on Analog Cost*

Traditional Partitioning—
Digital Chip, **Integrated**
Mixed Signal Front End (MxFE):

New Partitioning Trend—
Digital Customer ASIC, **Separate**
Mixed Signal Front End (MxFE):

0.35μm

Digital — Analog MxFE

NOW

0.18μm !

Digital — Analog MxFE — 0.35μm

NOW

$$$

$$

0.18μm

Digital — Analog MxFE

SOON

0.13μm !

Digital — Analog MxFE — 0.18μm

SOON

◆ **Better Overall Yield**
◆ **More Cost Effective**
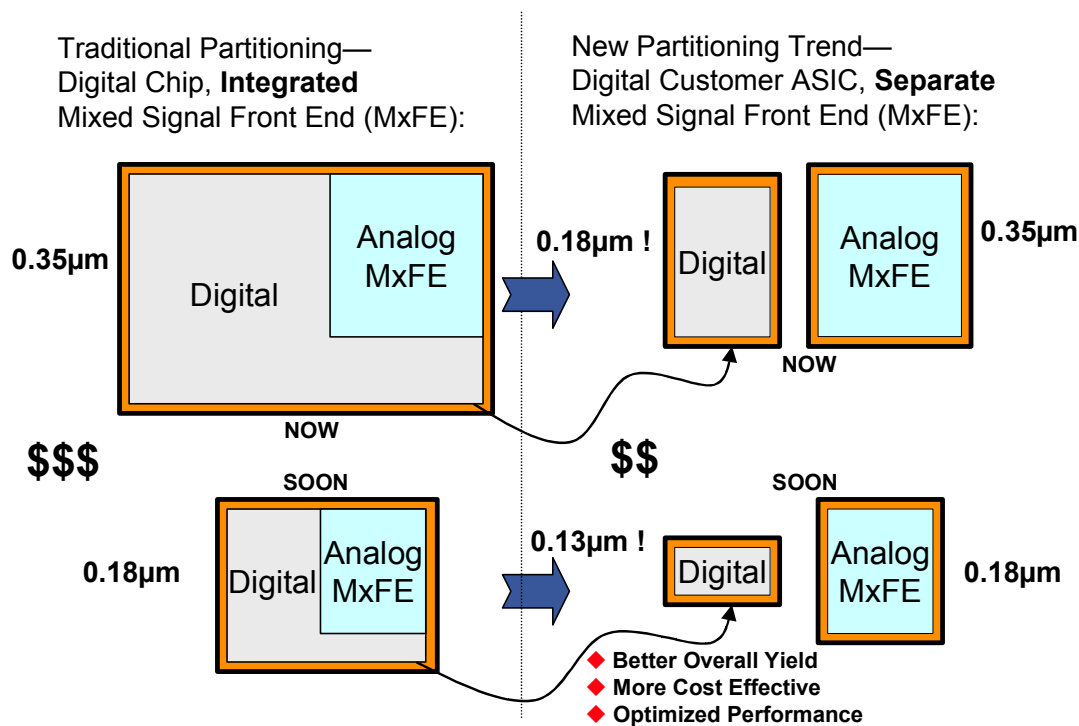◆ **Optimized Performance**

Figure 4.17: *Smart Analog/Digital Partitioning*
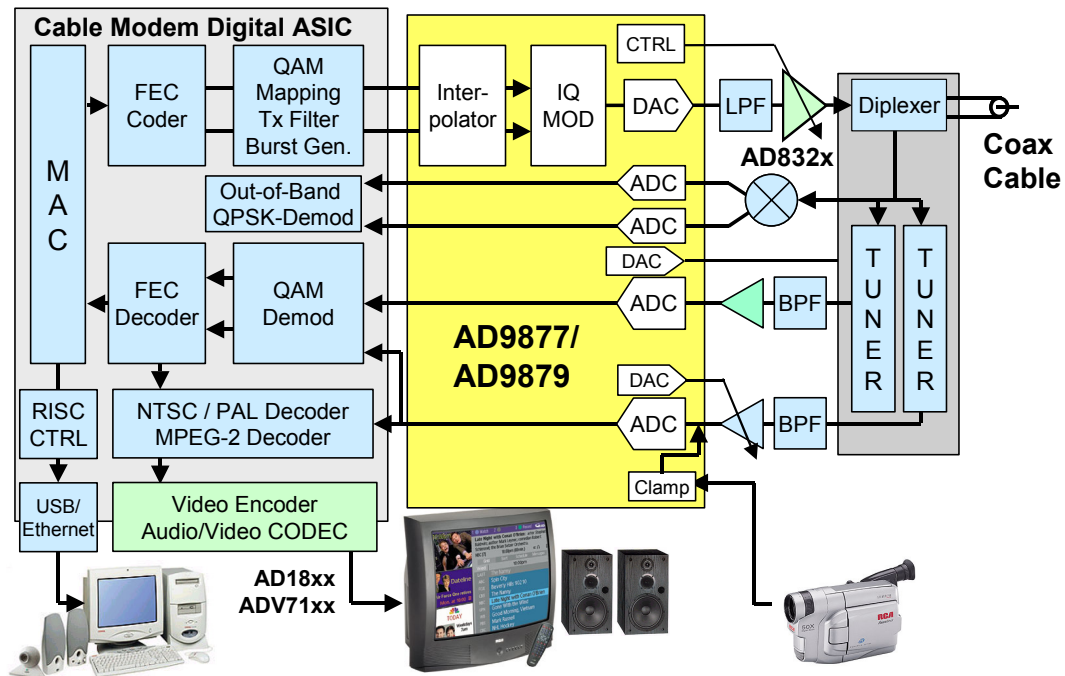
4.24

Figure 4.18: *AD9877 / AD9879 Set-Top Box Mixed Signal Front End (MxFE™)*

- *Performance*—ADI's TxDAC® family was launched several years ago, ushering in a new generation of CMOS digital-to-analog converters with exceptional dynamic performance suitable for communications applications. While the product family has three generations of stand-alone converters, it also includes several converters that take advantage of the fine-line CMOS process by integrating digital interpolation filters. These filters take the input data word stream and insert additional sample words that are created by on-chip digital FIR filters. The AD9777 (Figure 4.19) features a few interesting dimensions of smart partitioning.
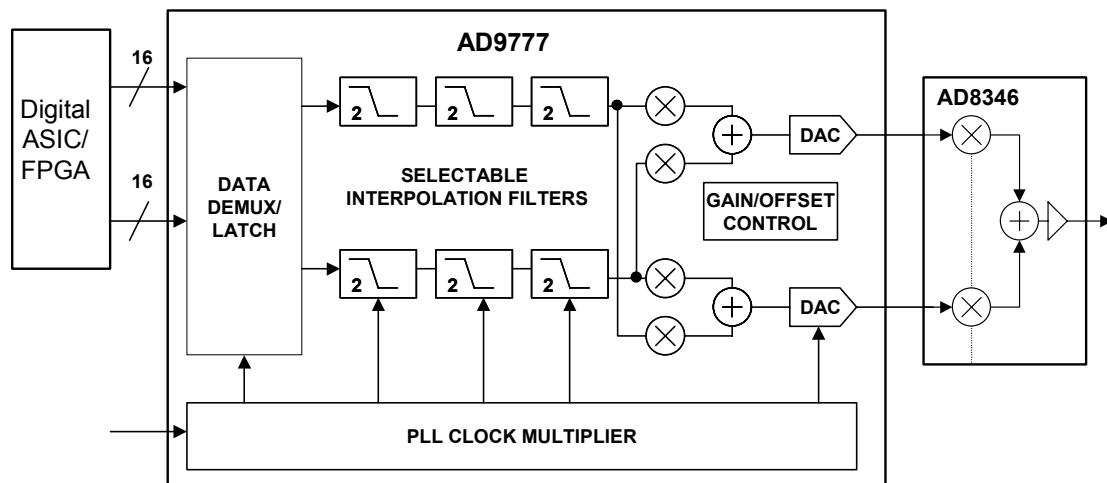

Figure 4.19: *AD9777 TxDAC and AD8346 Quadrature Modulator*

For example, putting both DACs on the same piece of silicon significantly improves the matching performance, which is critical for quadrature balance in many communications applications. Furthermore, it allows a complex digital upconversion to be performed. Integrating the interpolation filter means that the very high-speed data bus to the DAC (which may run at 400 MHz or more) need never come off chip, providing significant improvements in power dissipation and EMI. The AD9777 is designed to mate with ADI's quadtrature modulator chip AD8346 as a two-chip set, significantly reducing the number of external components required. Why not integrate the analog mixer? For performance and testability reasons, it is implemented on a bipolar process. Its specifications far exceed what is possible in CMOS.

The primary benefit of smart partitioning is the ability to integrate digital functionality onto high-performance analog circuits and vice-versa. This frees designers to partition rather than forcing them into a certain arrangement based on the inherent limitations of their chip's functionality.

Combining functionality in high-performance analog circuitry and high-performance DSP provides great latitude in partitioning options. This must be combined with a strong system understanding in order to make the wisest choices.

Why Smart Partitioning is Necessary

A single, dominant force has governed the semiconductor universe over the past 25 years: the trend toward ever-higher levels of integration. Gordon Moore of Intel even effectively quantified the slope of this trend, claiming that the level of integration on ICs would double every 18 months. This has become known as Moore's Law, and has been a remarkably accurate predictor of the integration trend for semiconductor circuits.

There have been many critical technology advances that have enabled the industry to keep pace with Moore's prediction. These have included advances to finer and finer lithography, the ability to handle larger and larger wafers, improvements in chemical purity, and reductions in defect density. The benefits of marching down this integration curve have been astounding: exponentially improved processing capability, faster processing speeds, decreasing costs, and reduced size and power consumption.

While the most notable examples of the integration trend have been seen in memory circuits (like DRAM) or in microprocessors, the theme of ever-higher levels of integration pervades virtually every corner of the semiconductor world. The analog world has been no exception. Over the last 30 years, the state of the art in analog has moved from operational amplifiers (op-amps) on a single chip, to whole converters, to entire mixed-signal systems that replace 30 to 50 discrete chips.

Originally, analog integrated circuits were implemented on process technologies that differed significantly from those used for digital circuits. During the 1980s and 90s, there was increasing emphasis placed on building analog functions on digital processes, allowing the analog and digital circuitry to be integrated onto a signal IC—a "mixed-signal" integrated circuit. This has been highly effective, and mixed signal ICs are pervasive in today's products, from cell phones to digital still cameras. However, the complexities involved with implementing the analog functions have meant that mixed-

signal ICs tend to lag their entirely digital counterparts by at least one lithography generation. While today's state-of-the art digital circuits are being designed on 0.13-µm processes, the most advanced mixed-signal circuits are being done on 0.18-µm or 0.25-µm processes.

What's Changing?

As we enter the new millennium, we are starting to see some changes that could have a significant impact on the seemingly inevitable trend to higher integration. Fundamental laws of physics may ultimately limit the ability to keep shrinking the lithography. We are already seeing some significant increases in costs (refer back to Figure 4.15 and Figure 4.16), and in a few generations, we may reach a point where further feature-size reductions aren't economically practical.

Through most of the 1990s, the analog designers rode the lithography curve that the digital circuits were pushing. However, late in the decade, there was a significant catch: with each lithography shrink below 0.5 µm, the maximum allowable supply voltage also falls. While this was of little consequence to the digital designer (it actually helps to lower power dissipation), it has enormous significance to the analog designer. Shrinking supply voltages force the use of smaller signal voltages, making it even more difficult to preserve the analog signal in the presence of inevitable noise.

Instead of being able to transfer circuit blocks from one lithography generation to the next, each new lithography sends the analog designer back to the drawing board. The consequences can be significant. Instead of mixed signal lagging digital by one lithography generation, this lag is starting to stretch to two to three generations. Some very high-performance circuits may eventually be impractical (though probably not impossible) on extremely fine line geometries.

As supply voltages on state-of-the-art digital processes continue to drop, specialized processes may become more popular for high-performance mixed-signal circuits. Figure 4.20 illustrates that there are other process technology curves that parallel the digital CMOS curve. These are processes that have been optimized for analog circuits, making different trade-offs more appropriate to the needs of the analog circuit designers.

In addition to the difficulties of designing analog circuits in smaller geometries, there is another problem facing "further integration" as the model for future electronic design: process technology has, in many cases, outpaced design and simulation capability. We are now able to integrate larger systems than we are able to effectively simulate, analyze or test.

In the face of these problems, some pundits have predicted that things will go back to the way they were in the mid-to-late 1980s: digital circuits on one chip, analog circuits on another, with different process technologies, simulation tools, and designers used for each. This would essentially constitute a "dis-integration" of the analog from the digital. While some systems may break down this way, in many cases, the real answer will be more subtle (and more interesting).
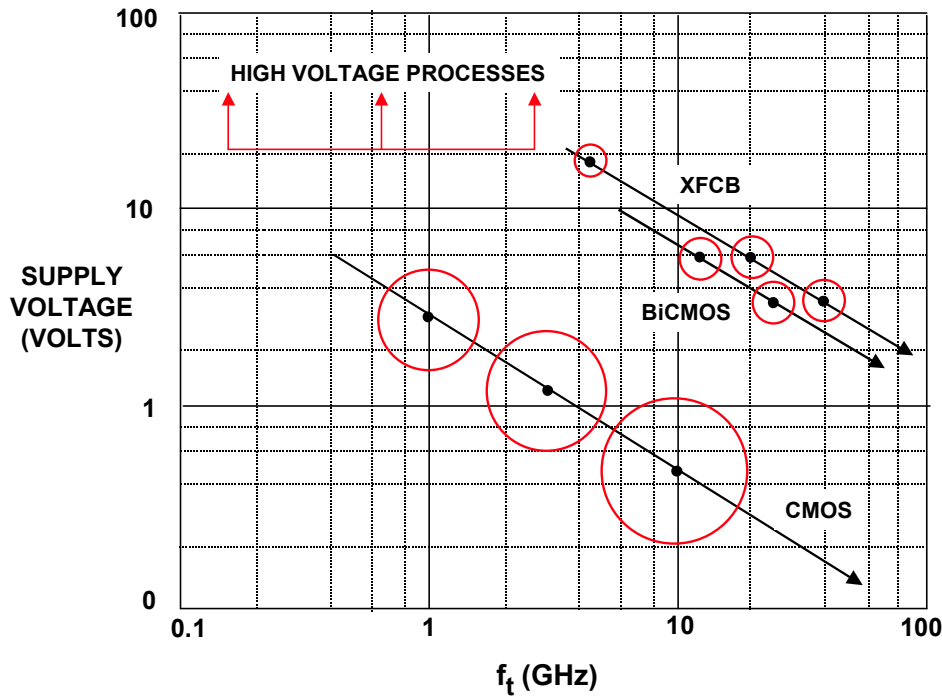
Figure 4.20: *Range of Semiconductor Processes*

There was an evening panel discussion several years ago at one of the major integrated circuits conferences-the topic was "The Single-chip Cell Phone." The discussion pushed back and forth about the technical challenges associated with combining the different chips in a cellular telephone. At one point, a panelist put a picture of a cell phone circuit board up on the screen. He noted 6 integrated circuits and 300 passive components. "Stop trying to combine these 6 ICs into one," he said, "and let's do something about all the passive components!" The lesson from this story is that integration needs to be used in an intelligent way to reduce the cost, size, and power demands of the overall system, not simply as an exercise in blindly reducing the IC count.

As we approach the practical limits of integration and lithography, intelligence will need to be applied as to where and how to integrate. The key is to find optimal points to break the system into functional blocks. Typically, these will be places that require a minimum information flow across the boundaries between them, allowing the pin counts (and therefore cost and size) of the ICs to be kept low. Consideration should also be given to how the system and ICs will be simulated and analyzed. The partitioning dictated by these factors may or may not correspond to the boundary between analog and digital.

Analog Devices has been working on chip set partitioning for a number of years, and the theme of "smart partitioning" has emerged as one of the most significant factors in optimizing the cost, size, power, and performance for systems that feature both analog and digital circuits.

Figure 4.21 illustrates an example, taken from a real case, where three chips are cheaper than one or two. One of the keys is allowing the majority of the digital functionality to be implemented in the most effective process possible, avoiding the one-to-three generation

lag normally associated with attempting to integrate everything. Using higher-performance optimized processes for the mixed-signal and analog functions eliminates a large number of external passive/discrete components, thereby significantly reducing system size and cost. The mixed-signal front end AD9860/AD9862 as shown in this application is actually an excellent example for integration of several high-speed converters onto a single CMOS chip (see also Figure 4.22).
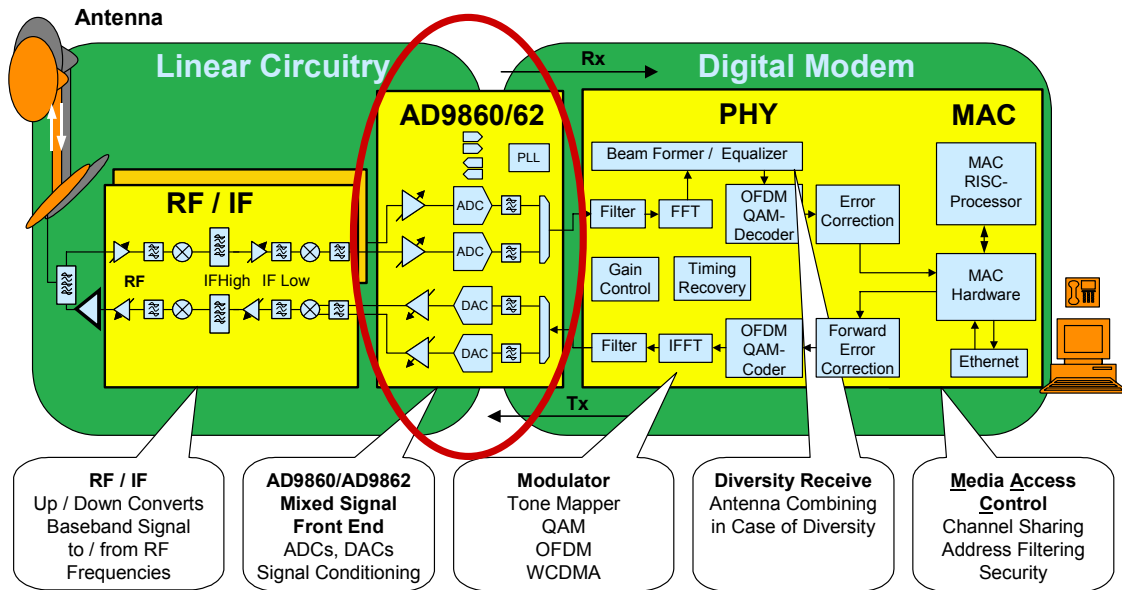

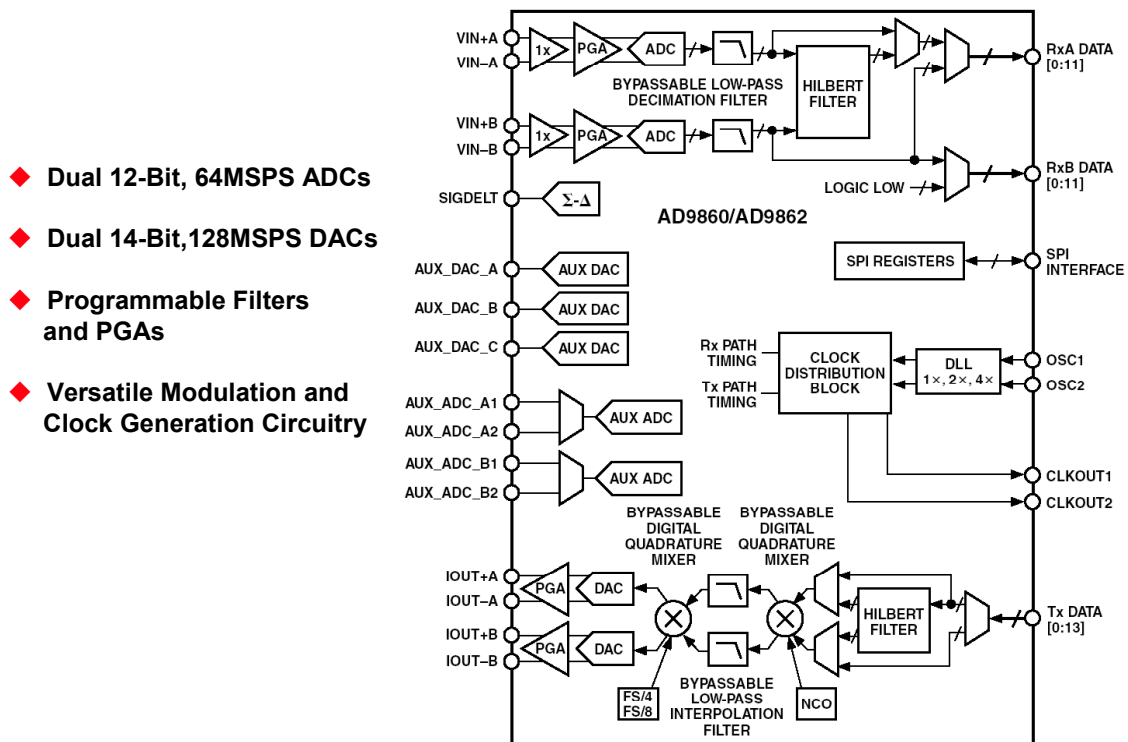*Figure 4.21: AD9860/AD9862: Broadband Wireless OFDM Modem*

- ◆ **Dual 12-Bit, 64MSPS ADCs**
- ◆ **Dual 14-Bit,128MSPS DACs**
- ◆ **Programmable Filters and PGAs**
- ◆ **Versatile Modulation and Clock Generation Circuitry**

Figure 4.22: AD9860/AD9862 MxFE™ for Broadband Communications

In that device, putting dual DACs and dual ADCs on the same piece of silicon guarantees matching performance, which is important for applications that require IQ modulation and demodulation. With careful chip design, sufficient isolation between transmit and receive path has been achieved. Variable gain amplifiers as well as auxiliary ADCs and DACs have all successfully been integrated. The CMOS process allowed for embedding complex digital upconversion, interpolation and decimation. This eases digital interface requirements significantly by reducing the data rate between the digital and mixed-signal chip. A lower speed interface draws less power and also improves EMI. Radio components like the mixer, power amplifier and low noise amplifier are not integrated on this CMOS chip because they achieve better performance when implemented on bipolar processes.

For many in the IC world, the end of Moore's Law seems unthinkable-ever-shrinking lithography has come to be viewed as an inalienable right. Nevertheless, the signs pointing to the end of Moore's law are there for those who will see them, and prudent designers will adapt to the new realities.

It's worth noting that other industries have faced similar technology limitations and are still thriving. For example, the ever-upward trend in aircraft speed was remarkably predictable for forty years, from the Wright brothers to the end of World War II. Yet the sound barrier posed a technology barrier. While it was possible to fly faster than sound, it has not proven economically practical to do so for commercial aircraft. Instead, the aircraft industry has advanced along other dimensions. The electronics industry will do the same. Smart partitioning will be the industry's way forward.