SECTION II

LINEAR AND NON-LINEAR ANALOG SIGNAL PROCESSING

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SECTION II

LINEAR AND NON-LINEAR ANALOG SIGNAL PROCESSING

AMPLIFIERS USED AS ANALOG SIGNAL PROCESSORS

High performance operational amplifiers can be used to perform such mathematical operations such as addition, subtraction, differentiation, and integration. They can also be used to perform non-linear operations such as rectification and exponentiation. In addition, these operations can be performed on signals having bandwidths of greater than 100MHz because of recent advances in linear IC process technology as well as circuit topologies.

An inverting adder can be made with an op amp and a few resistors as shown in Figure 2.1, or, an instrumentation amplifier can be used with another op amp to form a non-inverting adder. A simple subtractor can be made by using an op amp in the differential mode as shown in Figure 2.2, or an instrumentation amplifier can be used for high input impedance.

OP AMP AND INSTRUMENTATION AMP ADDERS

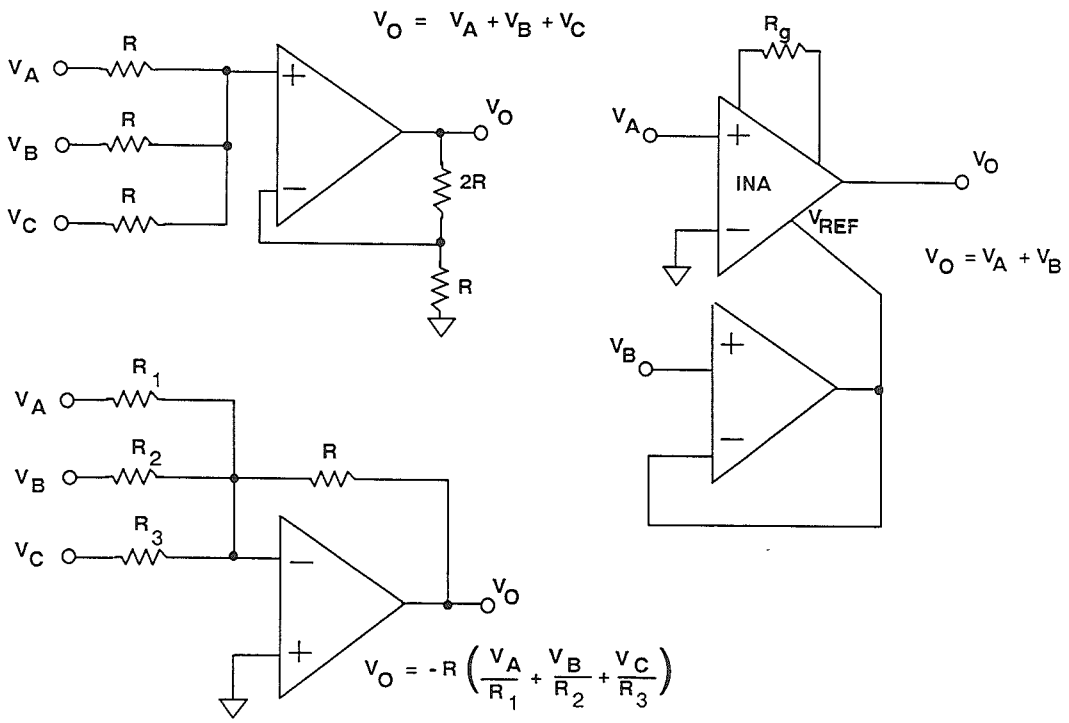


Figure 2.1

OP AMP AND INSTRUMENTATION AMP SUBTRACTORS

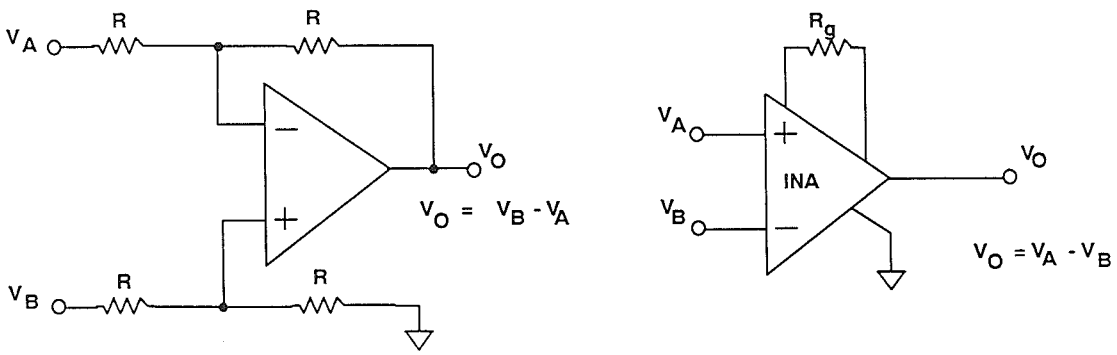


Figure 2.2

OP AMP DIFFERENTIATORS

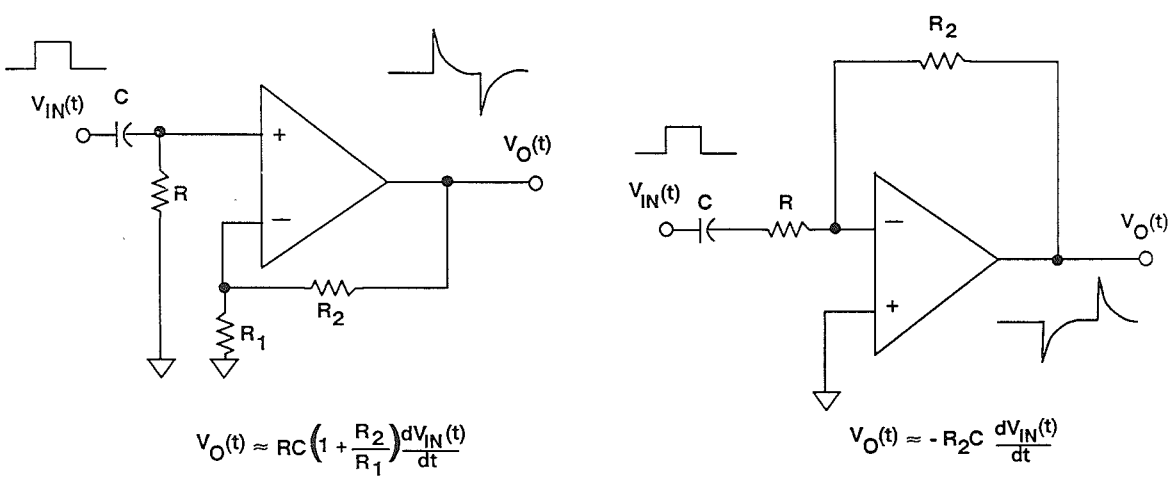


Figure 2.3

OP AMP INTEGRATOR

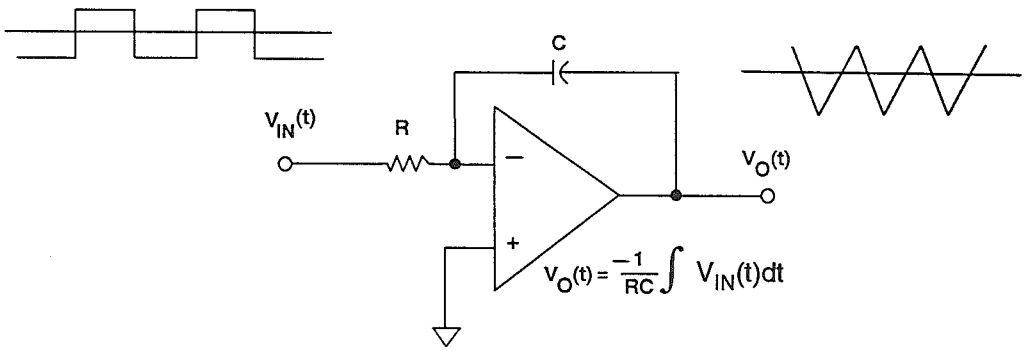


Figure 2.4

Figure 2.3 shows two versions of a simple differentiator, and Figure 2.4 shows the classic op amp circuit used for integration.

The circuit of Figure 2.5 is a typical absolute-value circuit. It comprises a diode network and a differencing circuit. Later, we will see how a multiplier can be used to perform the same function without the problems associated with the forward voltage drops of the diodes.

The peak detector circuit of Figure 2.6 can accurately capture the amplitude of input pulses as narrow as 200ns and can hold their value with a droop rate of less than 20μV/ms. The high bandwidth and 200V/μs slewrate of the AD843 op amp allows the detector's output to "keep up" with its input thus minimizing overshoot. The low (less than 1nA) input current of the AD843 (because of its FET input) ensures that the droop rate is limited only by the reverse leakage of diode D2, which is typically less than 10nA for the type shown. A more detailed description of the operation of this peak detector is given in Reference 1.

OP AMP ABSOLUTE VALUE CIRCUIT (FULL WAVE RECTIFIER)

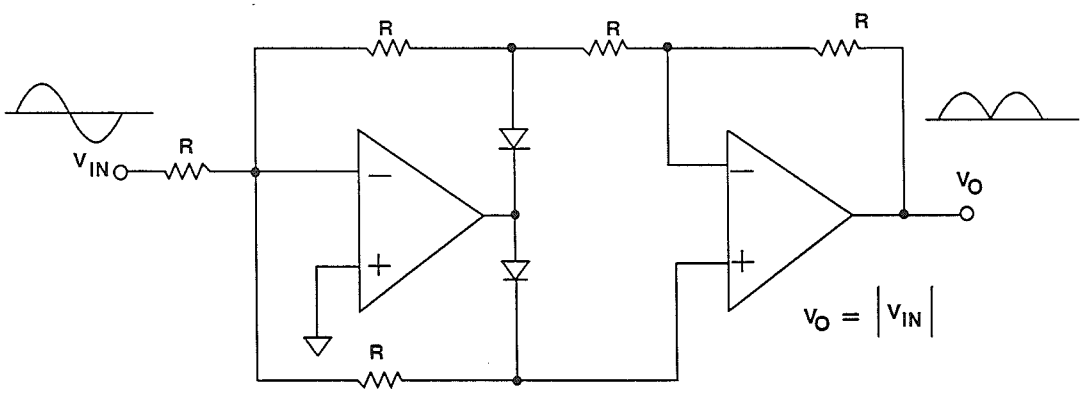


Figure 2.5

A FAST PEAK DETECTOR CIRCUIT

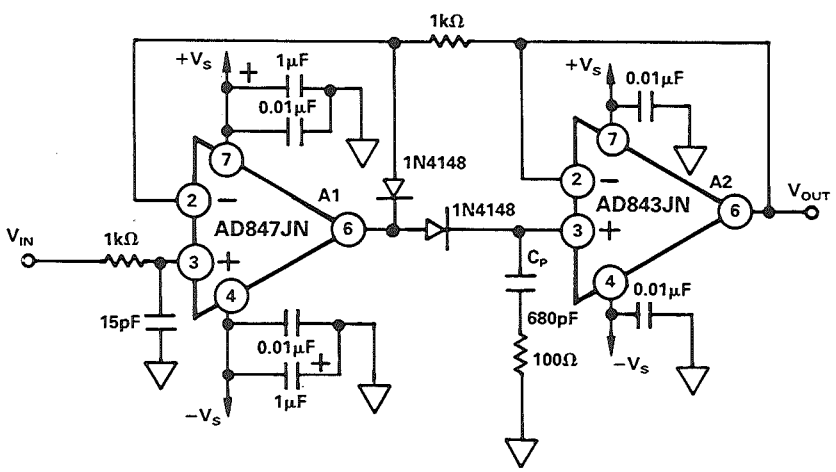


Figure 2.6

DISK DRIVE READ AMPLIFIERS

An excellent example of an analog signal processor can be found in disk drive read electronics. A block diagram of a typical system is shown in Figure 2.7. Data is stored as a stream of non-return-to-zero (NRZ) pulses, where each pulse requires a magnetic flux change on the disk. In the read mode, these flux reversals are sensed by the *head,* and a voltage is output to the preamplifier. The output from the head is a signal varying in amplitude, and adversely affected by the noise in the system. Amplitude variations are caused by deviations in height between the head and disk media, media integrity, and electrical noise. Therefore the output of the preamplifier also varies in amplitude. Although the preamplifier output represents digital data from the disk, analog conditioning is required in order to avoid intolerable errors.

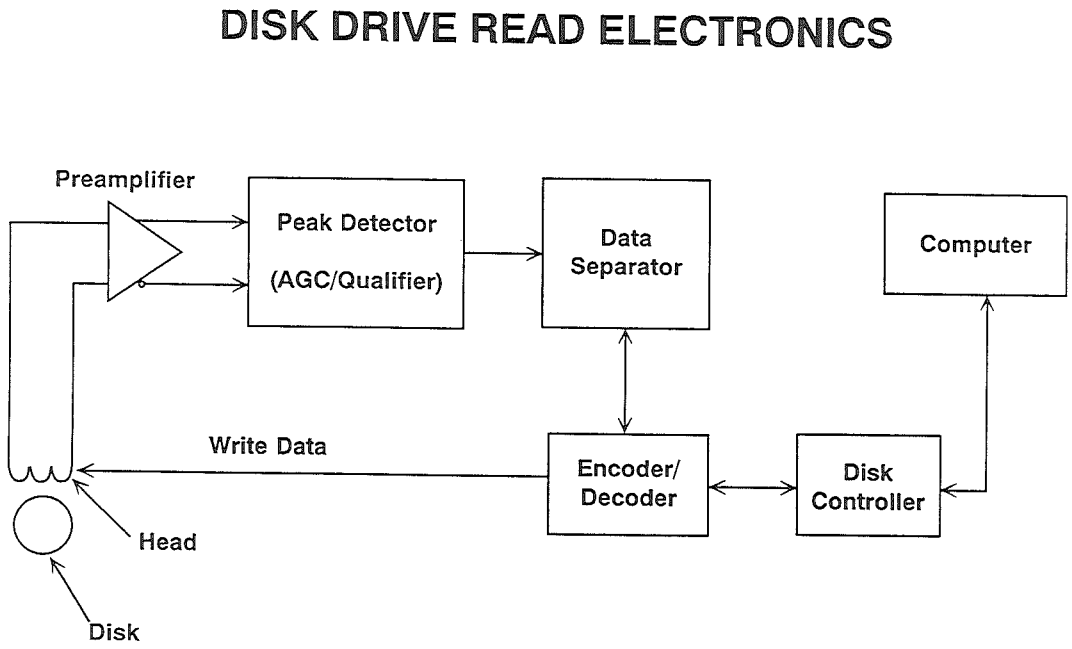


Figure 2.7

One half of the peak detection circuitry's function is to establish an automatic gain control (AGC) loop which produces a signal of constant amplitude. This may be implemented as shown in Figure 2.8 using a full-wave rectifier (FWR), a sample-and-hold (SHA) and a variable-gain-amplifier (VGA). The other half of the peak detector's function is to qualify the signal and output a digital pulse for every bit stored on the disk. Since the read signal is rectified prior to being applied to the data qualifier, a single comparator can be used to qualify both the positive and (rectified) negative peaks. This is accomplished by verifying that the input signal has achieved a minimum amplitude, and strobing the output only when a signal peak has been detected. The AGC'd signal is differentiated to produce a zero-crossing at the signal peaks. This peak and amplitude detection scheme is necessary to minimize data errors caused by noise-induced zero-crossings. That is, the level comparators must make sure the zero-crossings did indeed occur at the signal peaks.

PEAK DETECTOR

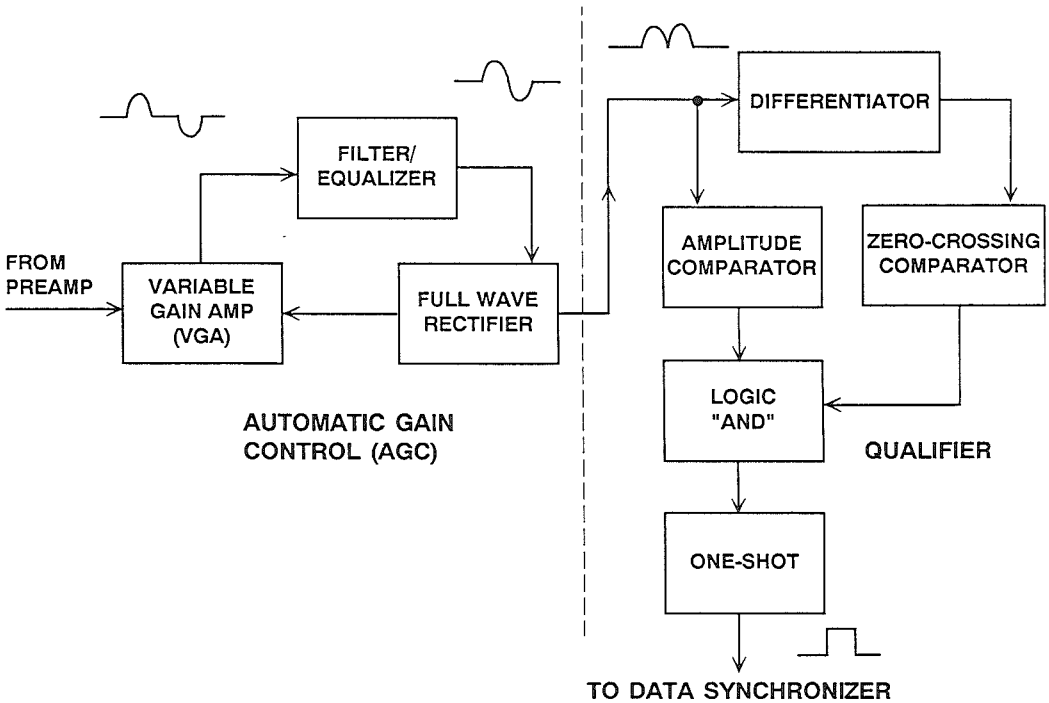


Figure 2.8

DATA SEPARATOR

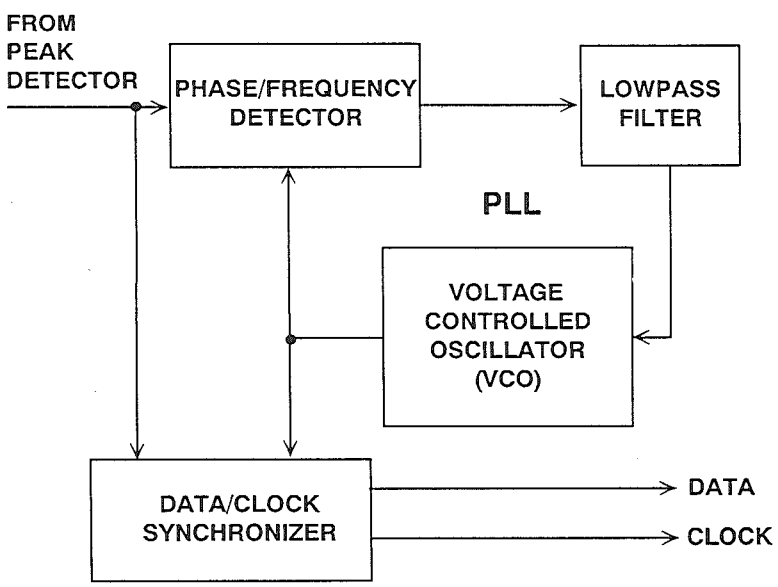


Figure 2.9

The data separator is used to extract clock information that is imbedded in the data. The input to this device is the digital pulse stream from the pulse detector's qualifier. The output is synchronized data and clock information. This is implemented using a phase-locked loop as shown in Figure 2.9.

The encoder/decoder is used for both write (encoder) and read (decoder) operations. In the write mode, NRZ data from the disk controller is coded and output to the head. In the read mode, the synchronized clock and (encoded) data outputs from the data separator are input to the encoder/decoder, whose output, in original NRZ format is passed on to the disk controller.

The AD890 (Precision Wideband Channel Processing Element) and the AD891 (Hard Disk Data Channel Qualifier) operate together to perform the pulse detection function at a rate of up to 50Mb/s. In addition, the AD891 can be used as a stand-alone variable gain amplifier having an 80MHz bandwidth with a 30dB maximum gain and a 40dB control range.

The AD892E (ECL) and the AD892T (TTL) integrate the AGC and peak detection functions of the AD890 and the AD891 onto a single chip. The AD892E can be used up to 30Mb/s, and the AD892T up to 25Mb/s.

The AD897 is a fully integrated 40Mb/s read channel which contains the AGC, peak detector, and phase locked loop. A functional block diagram of the device is shown in Figure 2.10.

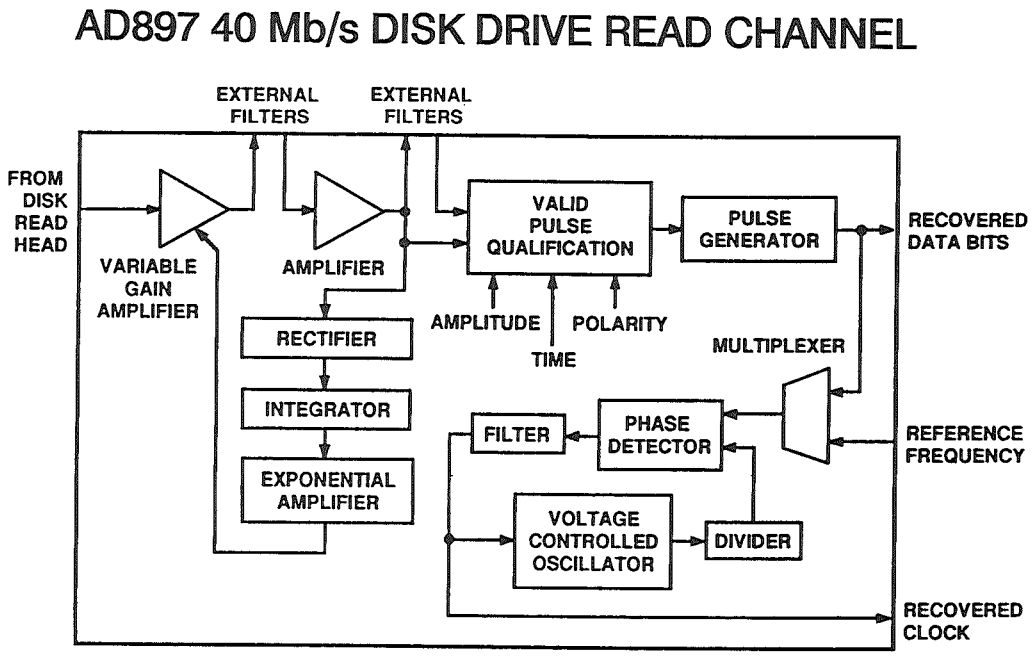


Figure 2.10

ANALOG MULTIPLIERS

A multiplier is a device having two input ports and an output port. The signal at the output is the product of the two input signals. If both input and output signals are voltages, the transfer characteristic is the product of the two voltages divided by a scaling factor, K, which has the dimension of voltage (see Figure 2.11). From a mathematical point of view, multiplication is a "four quadrant" operation - that is to say that both inputs may be either positive or negative, as may be the output. Some of the circuits used to produce electronic multipliers, however, are limited to signals of one polarity. If both signals must be unipolar, we have a "single quadrant" multiplier, and the output will also be unipolar. If one of the signals is unipolar, but the other may have either polarity, the multiplier is a "two quadrant" multiplier, and the output may have either polarity (and is "bipolar"). The circuitry used to produce one- and two-quadrant multipliers may be simpler than that required for four quadrant multipliers, and since there are many applications where full four quadrant multiplication is not required, it is common to find accurate devices which work only in one or two quadrants.

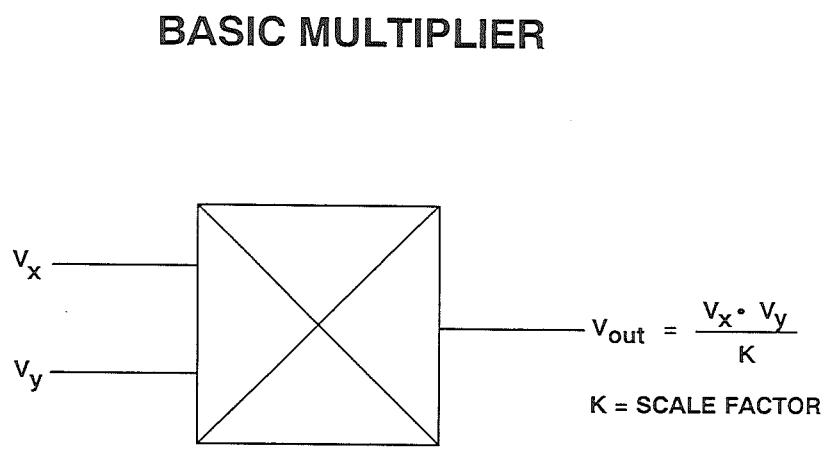


Figure 2.11

TYPES OF MULTIPLIERS

TYPE	V_x	V_y	V_{out}
Single Quadrant	Unipolar	Unipolar	Unipolar
Two Quadrant	Bipolar	Unipolar	Bipolar
Four Quadrant	Bipolar	Bipolar	Bipolar

Figure 2.12

The simplest electronic multipliers use logarithmic amplifiers. The computation relies on the fact that the antilog of the sum of the logs of two numbers is the product of those numbers (see Figure 2.13).

COMPUTATION WITH LOG AND ANTILOG CIRCUITS

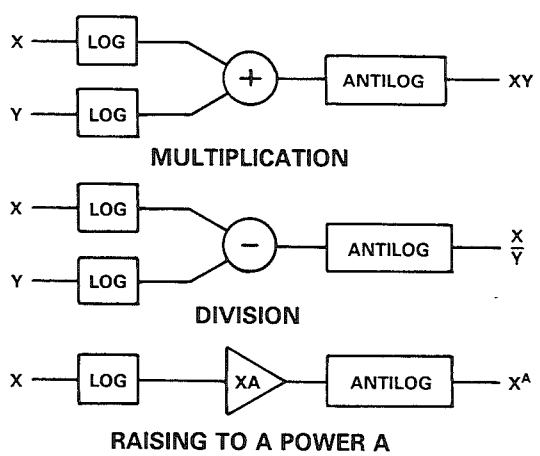


Figure 2.13

The disadvantages of this type of multiplication are the very limited bandwidth and single quadrant operation. A far better type of multiplier uses the "Gilbert Cell". This structure was invented by Barrie Gilbert in the late 1960s. (See References 2 and 3).

There is a linear relationship between the collector current of a silicon junction transistor and its transconductance (gain) which is given by

$dI_c / dV_{be} = qI_c / kT$, where
I_c = the collector current
V_{be} = the base-emitter voltage
q = the electron charge (1.60219E-19)
k = Boltzmann's constant (1.38062E-23)
T = the absolute temperature.

This relationship may be exploited to construct a multiplier with a long-tailed pair of silicon transistors, as shown in Figure 2.14.

BASIC TRANSCONDUCTANCE MULTIPLIER CIRCUIT

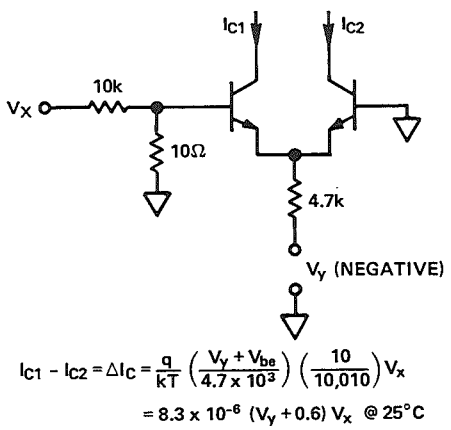


Figure 2.14

This is a rather poor multiplier because (1) the Y input is offset by the V_{be} - which changes non-linearly with V_y; (2) the X input is non-linear as a result of the exponential relationship between I_c and V_{be}; and (3) the scale factor varies with temperature.

Gilbert realized that this circuit could be linearized and made temperature stable by working with currents, rather than voltages, and by exploiting the logarithmic I_c / V_{be} properties of transistors (See Figure 2.15.)

THE GILBERT CELL - A LINEAR TWO-QUADRANT MULTIPLIER

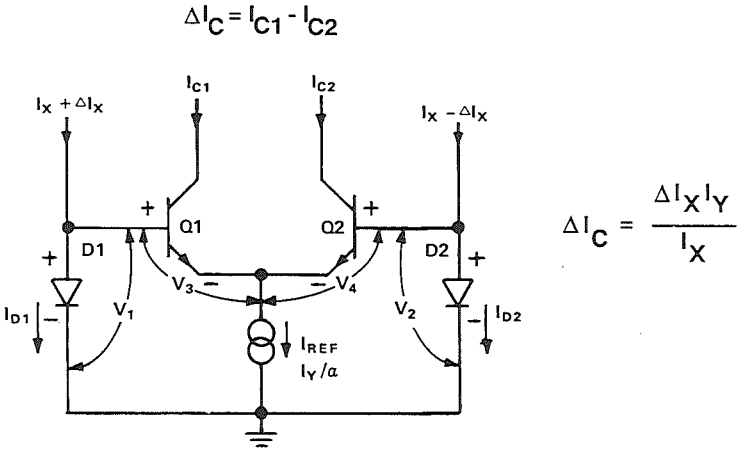


Figure 2.15

The X input to the Gilbert Cell takes the form of a differential current, and the Y input is a unipolar current. The differential X currents flow in two diode connected transistors, and the logarithmic voltages compensate for the exponential V_{be} / I_c relationship. Furthermore the q / kT scale factors cancel. This gives the Gilbert Cell the linear transfer function

$$\Delta I_c = \frac{\Delta I_x I_y}{I_x}$$

As it stands the Gilbert Cell has three inconvenient features: (1) Its X input is a differential current; (2) Its output is a differential current; and (3) Its Y input is a unipolar current - so the cell is only a two quadrant multiplier.

By cross-coupling two such cells and using two voltage-to-current converters (as shown in Figure 2.16), we can convert the basic architecture to a four quadrant device with voltage inputs, such as the AD534. At low and medium frequencies a subtractor amplifier may be used to convert the differential current at the output to a voltage. Because of its voltage output architecture, the bandwidth of the AD534 is only about 1MHz.

In Figure 2.16, Q1A & Q1B, and Q2A & Q2B form the two core long-tailed pairs of the two Gilbert Cells, while Q3A and Q3B are the linearizing transistors for both cells. In Figure 2.16 there is an operational amplifier acting as a differential current to single-ended voltage converter, but for higher speed applications the cross-coupled collectors of Q1 and Q2 form a differential open collector current output (as in the AD834 500MHz multiplier).

The translinear multiplier relies on the matching of a number of transistors and currents. This is easily accomplished on a monolithic chip. Even the best IC processes have some residual errors, however, and these show up as four dc error terms in such multipliers (see Figure 2.17).

In early Gilbert Cell multipliers these errors had to be trimmed by means of resistors and potentiometers external to the chip, which was somewhat inconvenient. With modern analog processes, which permit the laser trimming of SiCr thin film resistors on the chip itself, it is possible to trim these errors during manufacture so that the final device has very high accuracy. Internal trimming has the additional advantage that it does not reduce the high frequency performance, as may be the case with external trimpots.

4-QUADRANT TRANSLINEAR MULTIPLIER, THE AD534

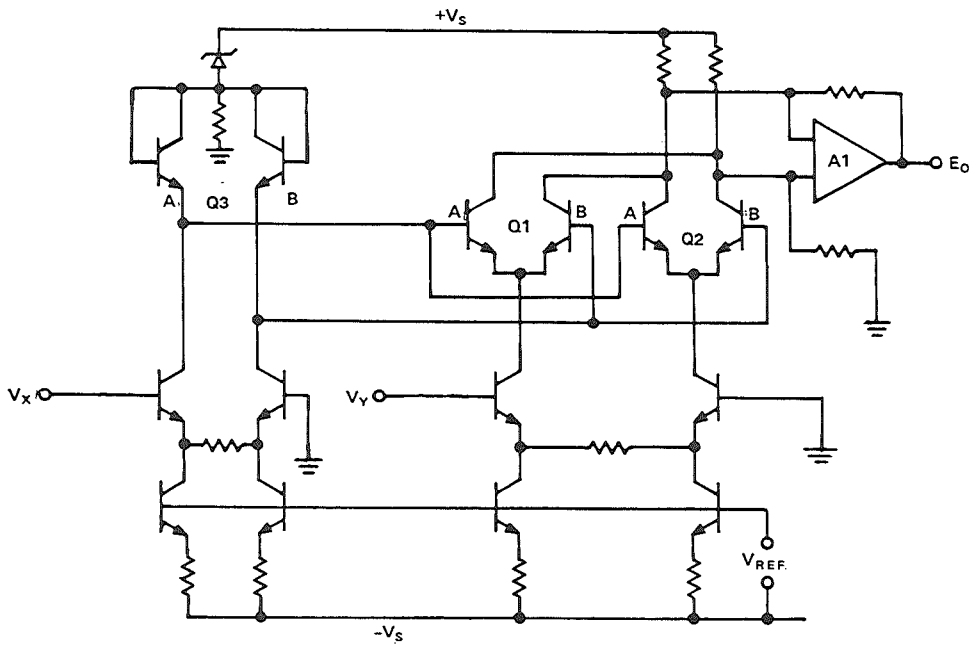


Figure 2.16

TRIMMABLE ERRORS IN MULTIPLIERS

- X-Input Offset Voltage: Y Feedthrough
- Y-Input Offset Voltage: X Feedthrough
- Z-Input (Output Amplifier) Voltage Offset: dc Output Offset Voltage
- Resistor Mismatch: Gain Error

Figure 2.17

The AD633 is a low cost 1MHz four quadrant multiplier. The AD734 is a 10MHz precision four quadrant multiplier/divider with a voltage output, and the AD834 is a 4 quadrant multiplier with differential X inputs, differential Y inputs, differential open collector current outputs, and a bandwidth of over 500MHz. Offset voltages are laser wafer trimmed, and accuracy is better than 0.1%.

KEY FEATURES OF THE TRANSLINEAR MULTIPLIER

- High Accuracy: Better that 0.1% Possible
- Wide Bandwidth (Over 60MHz Voltage Output, Over 500MHz Current Output)
- Simplicity, Low Cost, and Ease of Use

Figure 2.18

Multipliers can be used quite efficiently as power meters, by applying the voltage to one input and the current to the other input. Figure 2.19 shows an audio frequency power meter that measures the power output for an audio amplifier into an 8Ω load resistor. The 10kΩ-18kΩ voltage divider scales the amplifier's output swing to a maximum of 10V (from a maximum of 28V, representing about 100W peak power), well within the AD633's input range. The voltage is measured across the load, with the tap of the divider connected to X1 and the lower end of the load to X2. Current is measured across the 0.1Ω shunt. The AD711 op amp amplifies the signal to manageable levels and to drive the multipliers Y1 input. The output of the multiplier is (X1 - X2)Y1/10, which is proportional to the product of the load voltage and the load current, hence the power dissipated in the load.

AUDIO POWER METER USING AD633 MULTIPLIER

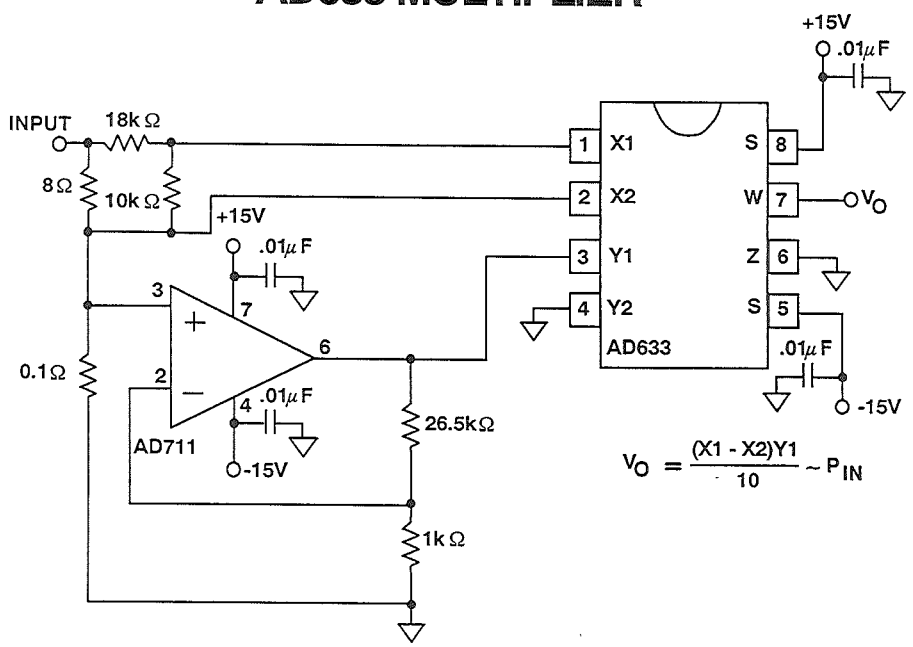


Figure 2.19

Multipliers can be placed in the feedback loop of op amps to form several useful functions. Figure 2.20 shows a multiplier and an op amp configured as a divider in both inverting and non-inverting mode. This circuit illustrates the principle of analog computation that a function generator in a negative feedback loop computes the inverse function (provided, of course, that the function is monotonic over the range of operation (see Figure 2.21).

MULTIPLIERS CONFIGURED AS DIVIDERS

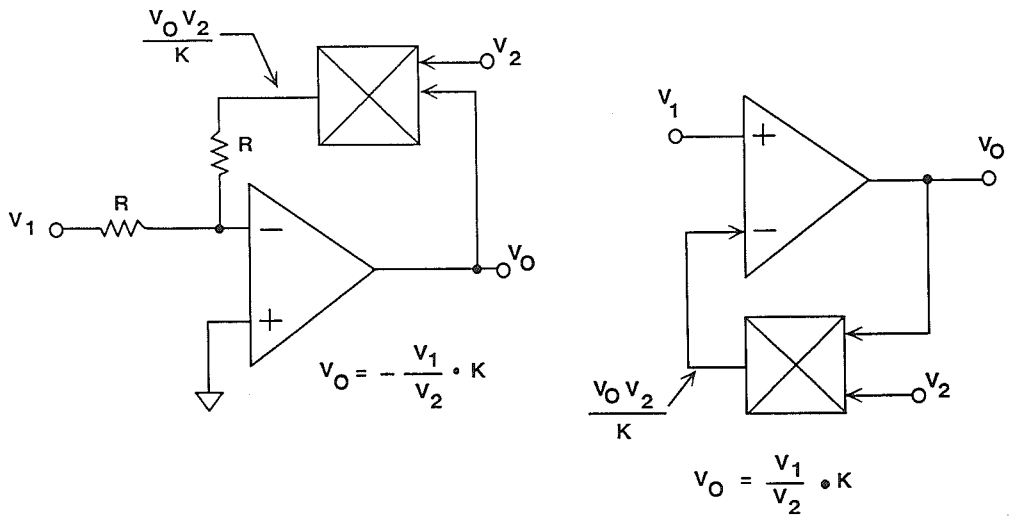
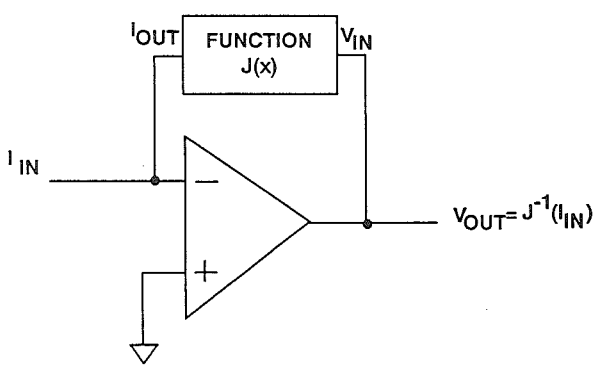


Figure 2.20

A FUNCTION GENERATOR IN A NEGATIVE-FEEDBACK LOOP GENERATES THE INVERSE FUNCTION



NOTE: FUNCTION MUST BE MONOTONIC OVER THE RELEVANT RANGE

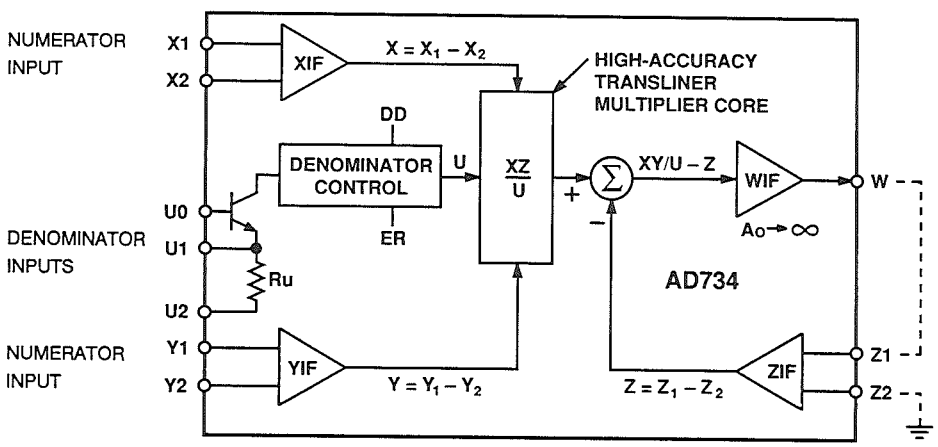
Figure 2.21

The AD734 is a 10MHz four-quadrant multiplier with an external input to dynamically change the scale factor, thereby accomplishing a direct-divide function. A functional block diagram of the device is shown in Figure 2.22.

A modulator is closely related to a multiplier. The output of a multiplier is the instantaneous product of its inputs. The output of a modulator is the instantaneous product of a signal on one of its inputs (known as the signal input) and the *sign* of the signal on the other input (known as the carrier input). A modulator may be modelled as an amplifier whose gain is switched positive and negative by the output of a comparator on its carrier input (as in the case of the AD630 balanced modulator) - or as a multiplier with a high-gain limiting amplifier between the carrier output and one of its ports. Both configurations are shown in Figure 2.23. Most high speed integrated circuit modulators consist of the translinear multiplier with a limiting amplifier in the carrier path. A precision rectifier, or absolute value circuit, can be made using a modulator as shown in Figure 2.24.

A multiplier can be used as a variable-gain amplifier as shown in Figure 2.25. The control voltage is applied to one input, and the signal to the other. The AD539 two-quadrant multiplier (60MHz bandwidth) and the AD844 current feedback amplifier can be used in a 20MHz variable gain amplifier configuration as shown in Figure 2.26. The frequency response of the variable gain amplifier for gains of +4 to -46dB as well as the transient response is shown in Figure 2.27. A current feedback (or transimpedance) amplifier is ideally suited for this application since its bandwidth remains relatively constant over a wide range of closed-loop gains.

10 MHz MULTIPLIER WITH DIRECT DIVIDE CAPABILITY



$$W = \left[\frac{(X1 - X2)(Y1 - Y2)}{U1 - U2} - (Z1 - Z2)\right] A_0$$

Figure 2.22

TWO MODULATOR MODELS

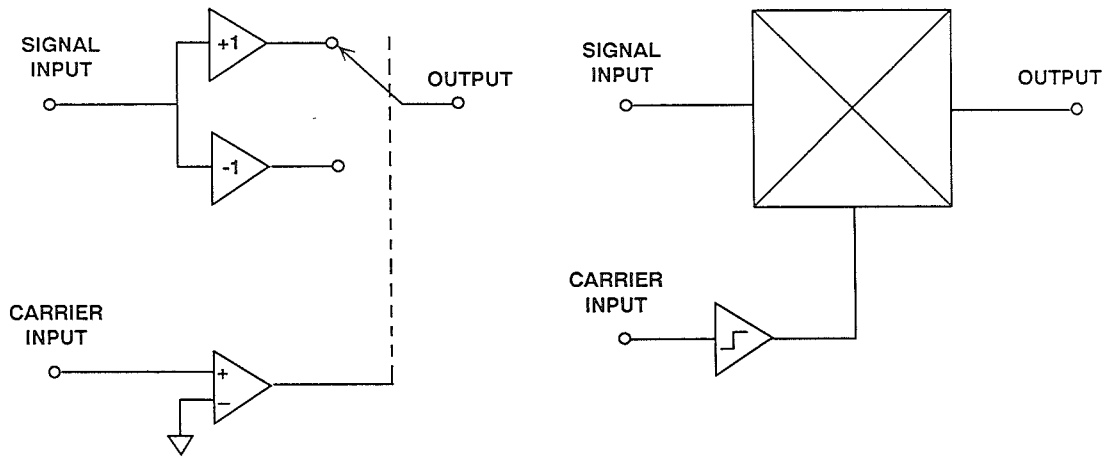


Figure 2.23

MODULATOR AS A PRECISION RECTIFIER (ABSOLUTE VALUE CIRCUIT)

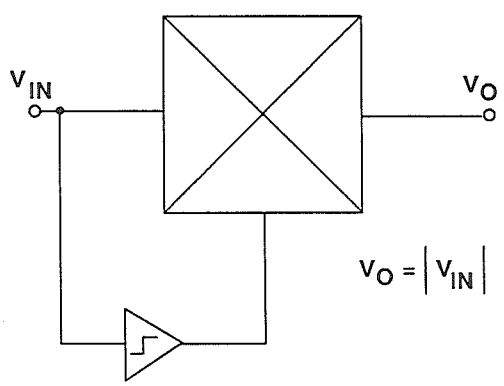
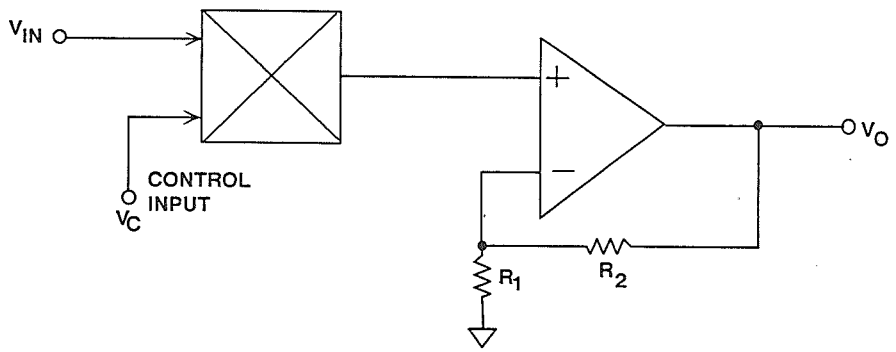


Figure 2.24

MULTIPLIER AS A VARIABLE GAIN AMPLIFIER



$$V_O = \frac{V_{IN}}{K} \bullet \left(1 + \frac{R_2}{R_1}\right) V_C$$

Figure 2.25

20MHz VARIABLE GAIN AMPLIFIER USING THE AD539

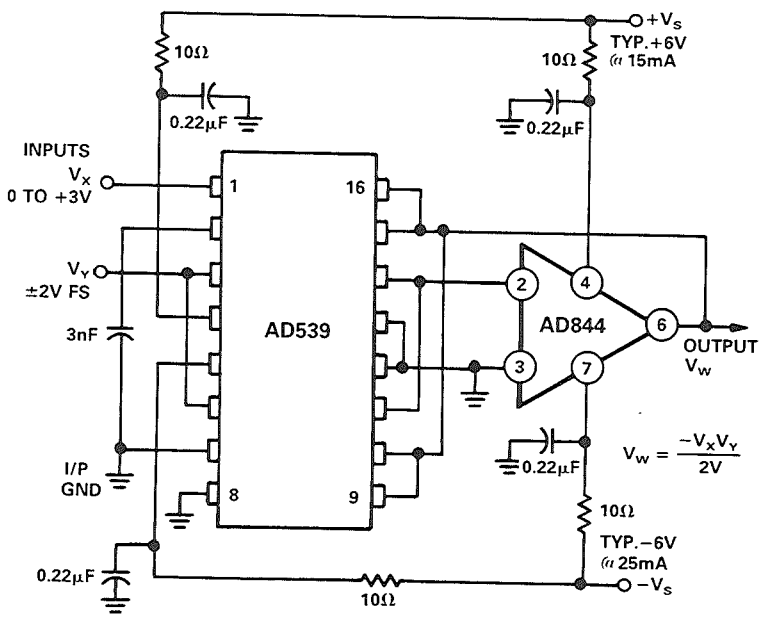
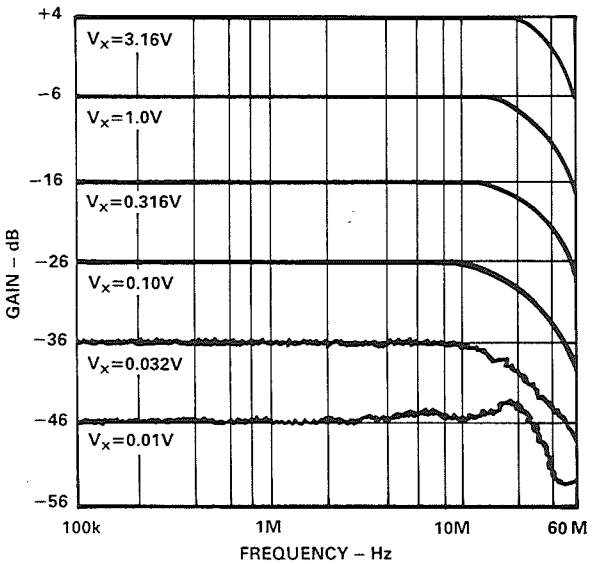
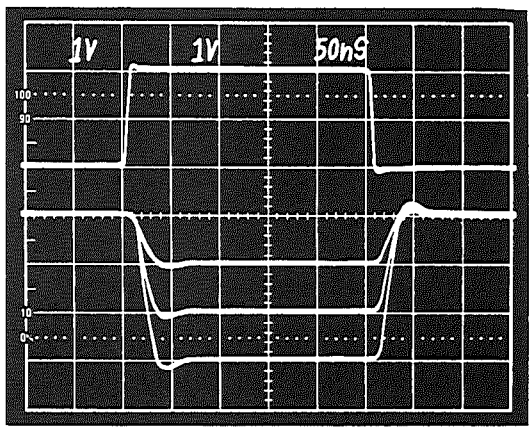


Figure 2.26

VGA AC AND TRANSIENT RESPONSE



VGA ac Response



VGA Transient Response with V_X = 1V, 2V, and 3V

Figure 2.27

RMS TO DC CONVERTERS

The rms or root mean square is a fundamental measurement of the magnitude of an ac signal. Defined practically, the rms value assigned to the ac signal is the amount of dc required to produce an equivalent amount of heat in the same load. Defined mathematically, the rms value of a voltage is defined as the value obtained by squaring the signal, taking the average, and then taking the square root. The averaging time must be sufficiently long to allow filtering at the lowest frequencies of operation desired. A complete discussion of rms to dc converters can be found in Reference 5, but we will now show a few examples of how efficiently analog circuits discussed so far can perform this function.

The first method, called the explicit method, is shown in Figure 2.28. The input signal is first squared by a multiplier. The average value is then taken by using an appropriate filter, and the square root is taken using an op amp with a second multiplier in the feedback loop. This circuit has limited dynamic range because the stages following the squarer must try to deal with a signal that varies enormously in amplitude. This restricts this method to inputs which have a maximum dynamic range of approximately 10:1 (20dB). However, excellent bandwidth (greater than 100MHz) can be achieved with high accuracy if a multiplier such as the AD834 is used as a building block (see Figure 2.29).

Figure 2.30 shows the circuit for computing the rms value of a signal using the implicit method. Here, the output is fed back to the direct-divide input of a multiplier such as the AD734. In this circuit, the output of the multiplier varies linearly (instead of as the square) with the rms value of the input. This considerably increases the dynamic range of the implicit circuit as compared to the explicit circuit. The disadvantage of this approach is that it generally has less bandwidth than the explicit computation.

EXPLICIT RMS COMPUTATION

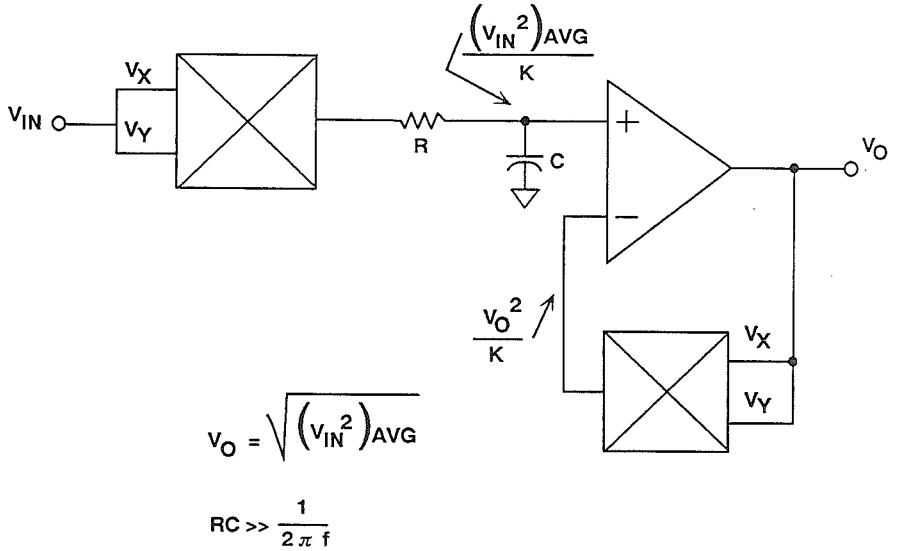


Figure 2.28

WIDEBAND R.M.S. MEASUREMENT WITH THE AD834

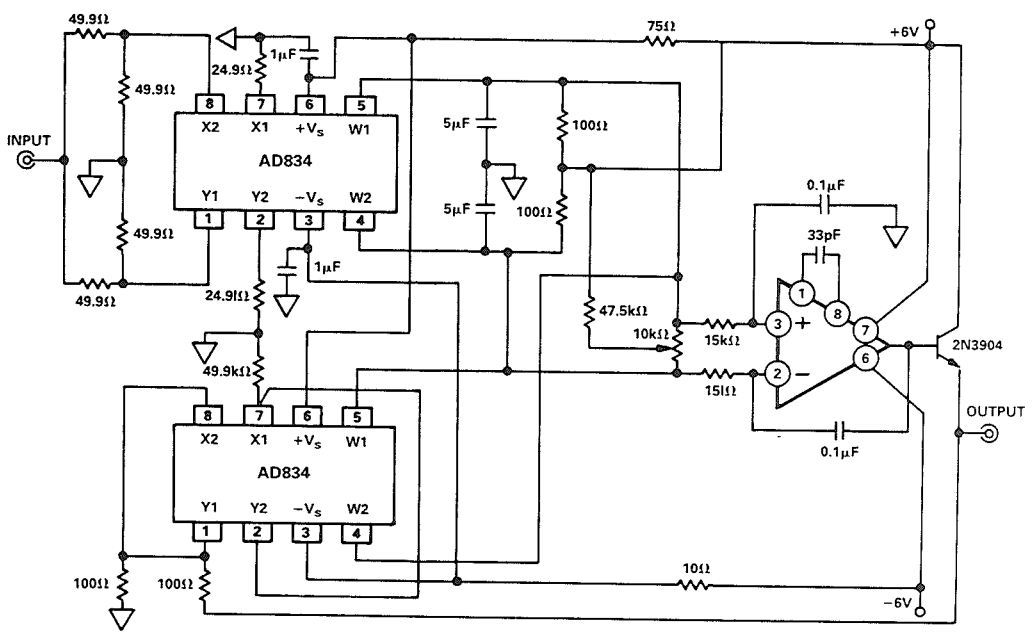


Figure 2.29

IMPLICIT RMS COMPUTATION

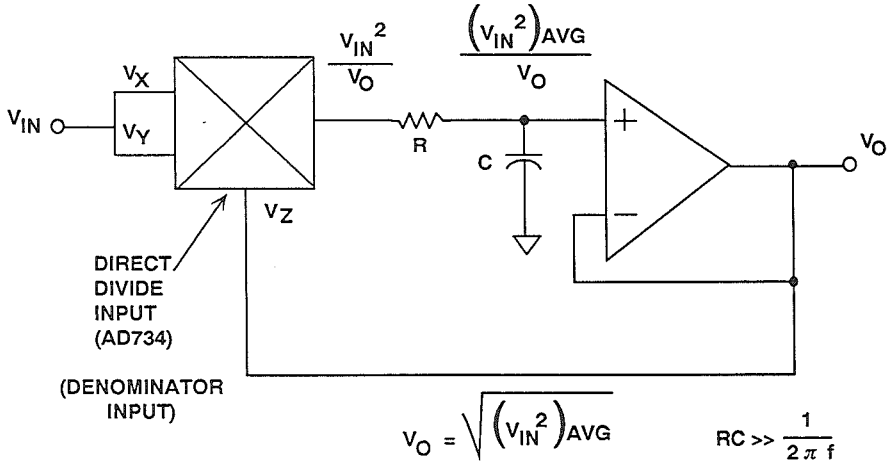


Figure 2.30

LOGARITHMIC CONVERTERS

Log amps find wide applications where signals having wide dynamic ranges (greater than 100dB, perhaps) must be processed by elements such as ADCs which may have more limited dynamic ranges. Log amps have maximum incremental gain for small signals; the gain decreases in inverse proportion to the magnitude of the input. This permits the amplifier to accept signals with a wide input dynamic range and compress them substantially.

The term "Logarithmic Amplifier" (generally abbreviated to "log amp") is something of a misnomer, and "logarithmic converter" would be a better description. A log amp must satisfy a transfer function of the form

$$V_{out} = V_y \log(V_{in}/V_x)$$

over some range of input values which may vary from 100:1 (40dB) to over 1,000,000:1 (120dB).

With inputs very close to zero, log amps cease to behave logarithmically, and most then have a linear V_{in}/V_{out} law. This behavior is often lost in device noise. Noise often limits the dynamic range of a log amp. The constant V_y has the dimensions of voltage because the output is a voltage. The input, V_{in}, is divided by a voltage V_x, because the argument of a logarithm must be a simple dimensionless ratio.

A graph of the transfer characteristic of a log amp is shown in Figure 2.31. The scale of the horizontal axis (the input) is logarithmic, and the ideal transfer characteristic is a straight line. When $V_{in} = V_x$, the logarithm is zero (log 1 = 0). V_x is therefore known as the *intercept voltage* of the log amp because the graph crosses the horizontal axis at this value of V_{in}.

The slope of the line is proportional to V_y. When setting scales, logarithms to the base 10 are most often used because this simplifies the relationship to decibel values: when $V_{in} = 10\ V_x$ the logarithm has the value of 1, so the output voltage is V_y. When $V_{in} = 100V_x$ the output is $2V_y$ and so forth. V_y can

LOG AMP TRANSFER FUNCTION

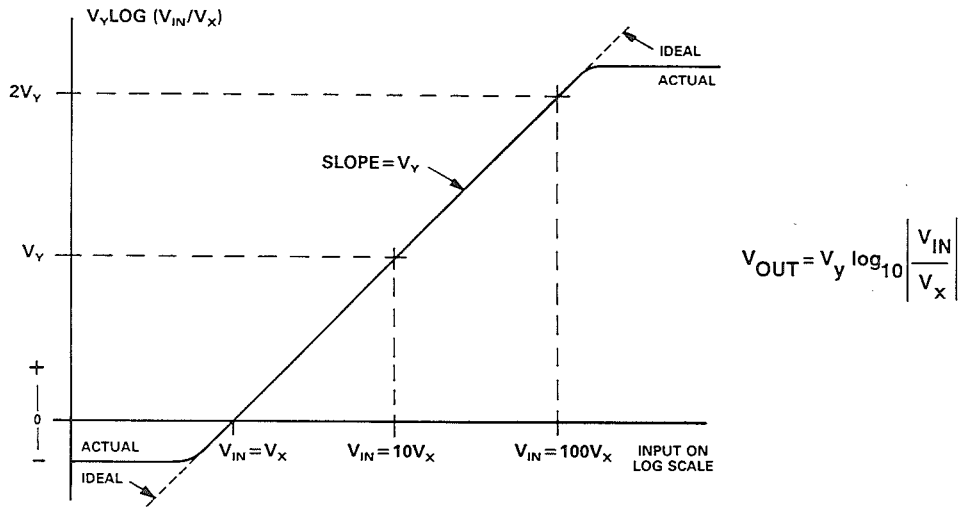


Figure 2.31

therefore be viewed either as the "slope voltage" or as the "volts per decade factor."

Log amps can respond to negative inputs in three different ways: (1) They can give a fullscale negative output as shown in Figure 2.32. (2) They can give an output which is proportional to the log of the absolute value of the input and disregards its sign as shown in Figure 2.33. This type of log amp can be considered to be a full-wave detector with a logarithmic characteristic, and is often referred to as a detecting log amp. (3) They can give an output which is proportional to the log of the absolute value of the input and has the same sign as the input as shown in Figure 2.34. This type of log amp can be considered to be a video amp with a logarithmic characteristic, and may be known as a logarithmic video amplifier or, sometimes, a "true log amp."

There are three basic architectures which may be used to produce log amps: the basic diode log amp, the successive detection log amp, and the "true log amp" which is based on cascaded semi-limiting amplifiers.

The voltage across a silicon diode is proportional to the logarithm of the current through it. If a diode is placed in the feedback path of an inverting op-amp, the output voltage will be proportional to the log of the input current as shown in Figure 2.35. In practice, the dynamic range of this configuration is limited to 40-60dB because of non-ideal diode characteristic, but if the diode is replaced with a diode-connected transistor as shown in Figure 2.36, the dynamic range can be extended to 120dB or more. This circuit has several major drawbacks; external compensation networks are required in order to obtain reasonable dc performance, and frequency response is limited to a few hundred kHz because of the feedback capacitance. Several such log amps can be combined on a single chip to perform an analog computer which performs both log and antilog operations as in the AD538 shown in Figure 2.37. The temperature variation in the log operations is unimportant, since it is compensated by similar variation in the antilogging. The AD538 can multiply, divide, and raise to powers.

BASIC LOG AMP
(SATURATES NEGATIVE WITH NEGATIVE INPUT)

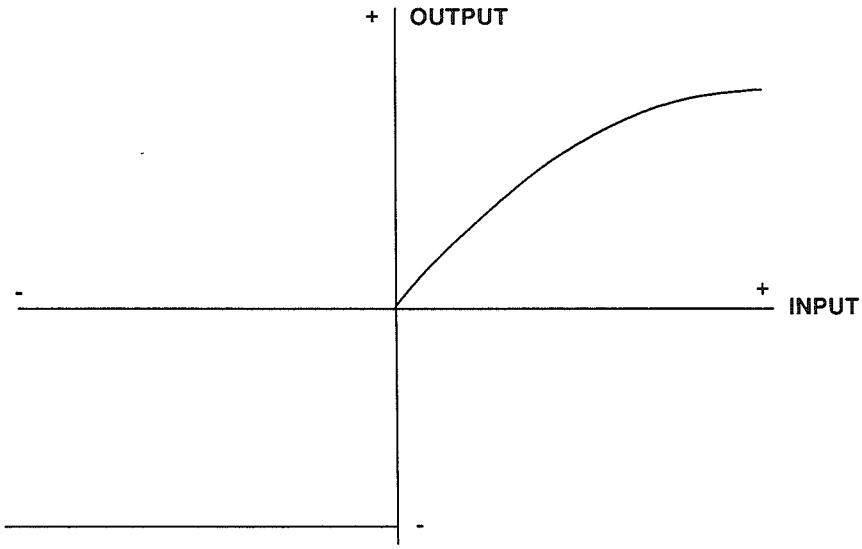


Figure 2.32

DETECTING LOG AMP
(OUTPUT POLARITY INDEPENDENT OF INPUT POLARITY)

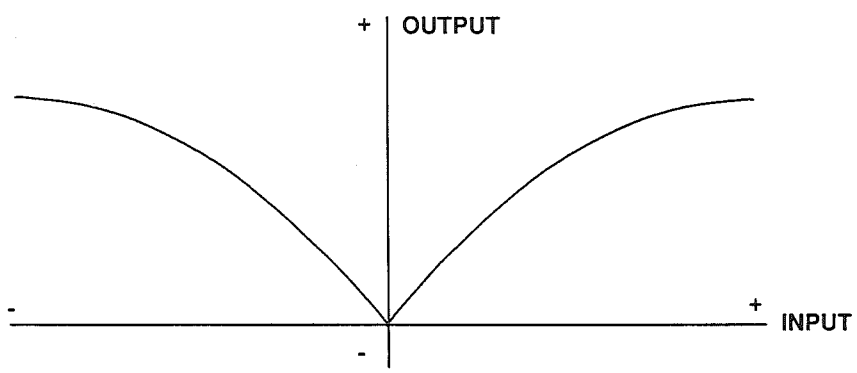


Figure 2.33

LOG VIDEO AMP OR "TRUE LOG AMP" (SYMMETRICAL RESPONSE TO POSITIVE OR NEGATIVE SIGNALS)

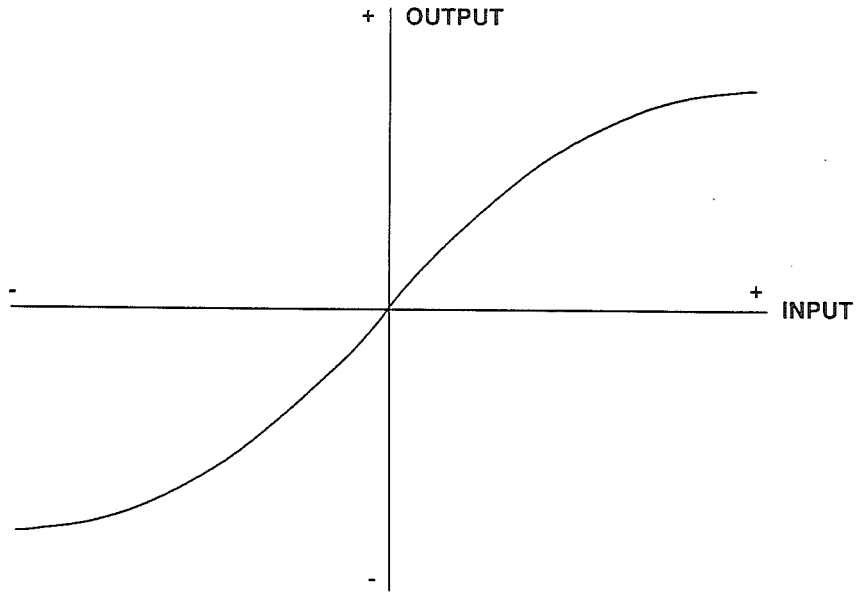


Figure 2.34

THE DIODE/OP-AMP LOG AMP

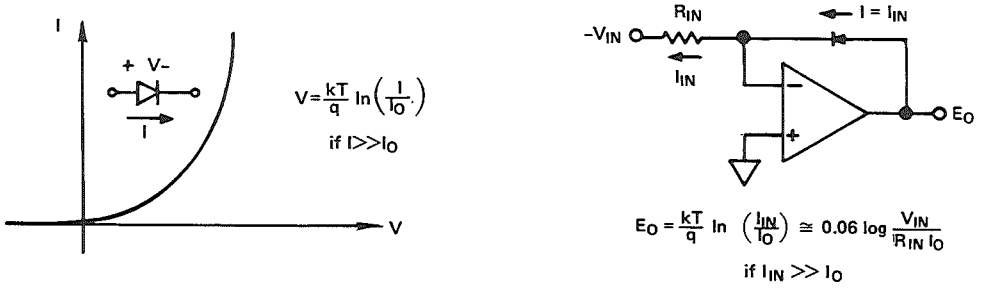


Figure 2.35

TRANSISTOR LOG AMP

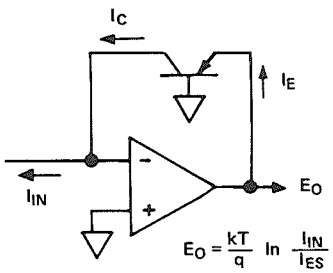
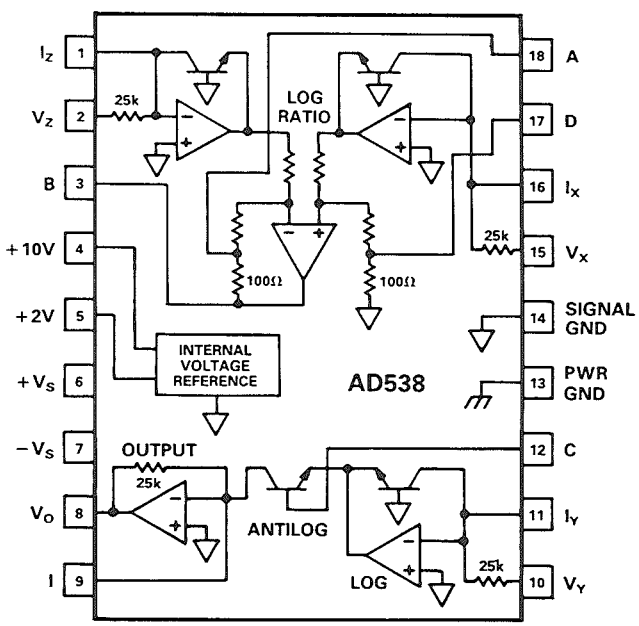


Figure 2.36

THE AD538



$$V_{out} = V_y \left(\frac{V_z}{V_x}\right)^m$$

Figure 2.37

For high frequency applications, therefore, detecting and "true log" architectures are used. Although these differ in detail, the general principle behind their design is common to both: instead of one amplifier having a logarithmic characteristic, these designs use a number of similar cascaded linear stages having well-defined large signal behavior.

Consider N cascaded limiting amplifiers, the output of each driving a summing circuit as well as the next stage as shown in Figure 2.38. If each amplifier has a gain of A dB, the small signal gain of the strip is NA dB. If the input signal is small enough for the last stage not to limit, the output of the summing amplifier will be dominated by the output of the last stage.

BASIC MULTI-STAGE LOG AMP ARCHITECTURE

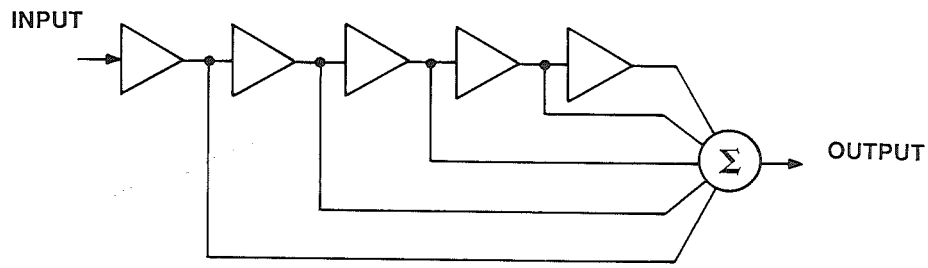


Figure 2.38

As the input signal increases, the last stage will limit. It will now make a fixed contribution to the output of the summing amplifier, but the incremental gain to the summing amplifier will drop to (N-1)A dB. As the input continues to increase, this stage in turn will limit and make a fixed contribution to the output, and the incremental gain will drop to (N-2)A dB, and so forth - until the first stage limits, and the output ceases to change with increasing signal input.

The response curve is thus a set of straight lines as shown in Figure 2.39. The total of these lines, though, is a very good approximation to a logarithmic curve, and in practical cases is an even better one, because few limiting amplifiers, especially high frequency ones, limit quite as abruptly as this model assumes.

The choice of gain, A, will also affect the log linearity. If the gain is too high the log approximation will be poor, if it is too low, too many stages will be required to achieve the desired dynamic range. Generally, gains of 10 to 12dB (3x to 4x) are chosen.

The specifications for log amps will, of course, include noise, dynamic range, frequency response (some of the amplifiers used as successive detection log amp stages have low frequency as well as high frequency cutoff), the slope of the transfer characteristic (expressed in V/dB or mA/dB depending on whether we are considering a voltage - or current output device), the intercept point (the input level at which the output voltage or current is zero), and the log linearity. (See Figure 2.40).

BASIC MULTI-STAGE LOG AMP RESPONSE (UNIPOLAR CASE)

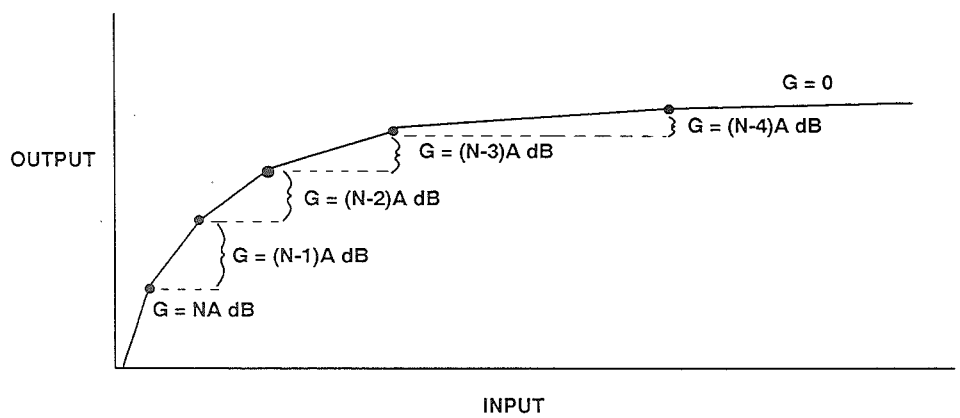


Figure 2.39

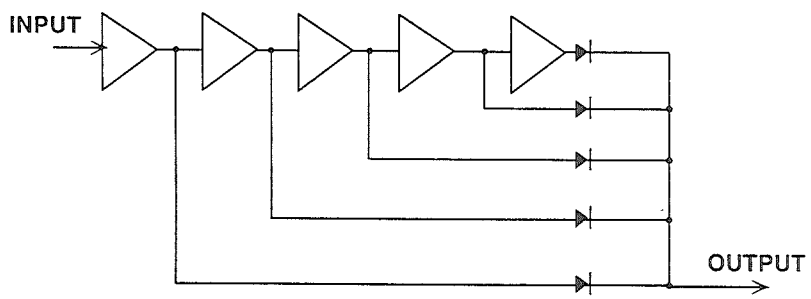
KEY PARAMETERS OF LOG AMPS

- **NOISE**
  The Noise Referred to the Input (RTI) of the Log Amp. It May Be Expressed as a Noise Figure or as a Noise Spectral Density (Voltage, Current, or Both) or as a Noise Voltage, a Noise Current, or Both
- **DYNAMIC RANGE**
  Range of Signal Over Which the Amplifier Behaves in a Logarithmic Manner (Expressed in dB)
- **FREQUENCY RESPONSE**
  Range of Frequencies Over Which the Log Amp Functions Correctly
- **SLOPE**
  Gradient of Transfer Characteristic in V/dB or mA/dB
- **INTERCEPT POINT**
  Value of Input Signal at Which Output is Zero
- **LOG LINEARITY**
  Deviation of Transfer Characteristic (Plotted on log/lin Axes) from a Straight Line (Expressed in dB)

Figure 2.40

The successive detection log amp consists of cascaded limiting stages as described above, but instead of summing their outputs directly, these outputs are applied to detectors, and the detector outputs are summed as shown in Figure 2.41. If the detectors have current outputs, the summing process may involve no more than connecting all the detector outputs together. The log output of a successive detection log amp generally contains amplitude information, and the phase and frequency information is lost.

SUCCESSIVE DETECTION LOGARITHMIC AMPLIFIER



Detectors may be full- or half-wave but should be current output devices (not simple diodes) so that the detector outputs may be summed without additional summing components being necessary.

Figure 2.41

In the past, it has been necessary to construct high performance, high frequency successive detection log amps (called log strips) using a number of individual limiting amplifiers. These are typically assembled in complex and costly hybrids. Recent advances in IC processes have allowed this complete function to be integrated into a single chip.

The AD640 log amp contains five limiting stages (10dB per stage) and five full-wave detectors in a single IC package, and its logarithmic performance extends from dc to 145MHz. Furthermore, its amplifier and full-wave detector stages are balanced so that, with reasonable well-considered layout, instability from feedback via supply rails is unlikely. A block diagram of the AD640 is shown in Figure 2.42. Unlike all previous integrated circuit log amps, the AD640 is laser trimmed to high absolute accuracy of both slope and intercept, and is fully temperature compensated. Key features of the AD640 are summarized in Figure 2.43.

BLOCK DIAGRAM OF THE AD640

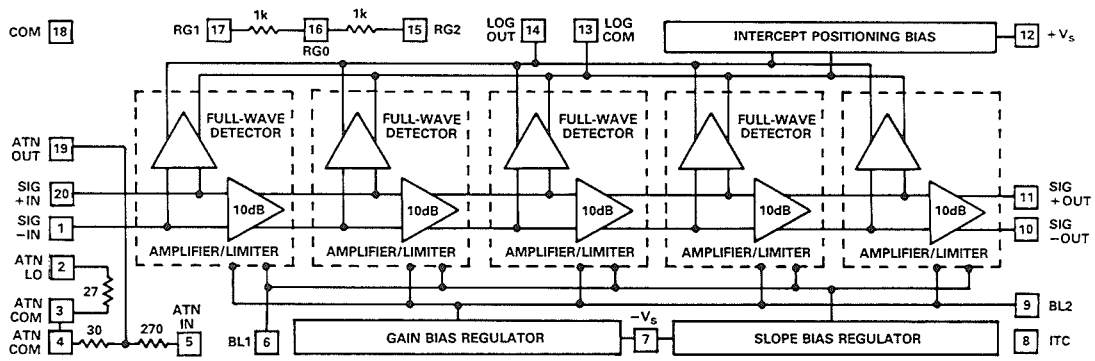


Figure 2.42

AD640 FEATURES

- 45dB Dynamic Range - Two AD640s Cascadable to 95dB
- Bandwidth dc to 145MHz - 120MHz when Cascaded
- Laser-Trimmed Slope of 1mA/decade - Temperature Stable
- Less than 1dB Log Non-Linearity
- Balanced Circuitry for Stability
- Minimal External Component Requirement

Figure 2.43

Each of the five stages in the AD640 has a gain of 10dB and a full-wave detected output. The transfer function for the device is shown in Figure 2.44 along with the error curve. Note the excellent log linearity over an input range of 1 to 100mV (40dB). Although well suited to rf applications, the AD640 is dc-coupled throughout. This allows it to be used in LF and VLF systems, including audio measurements, sonar, and other instrumentation applications requiring operation to low frequencies or even dc.

DC LOGARITHMIC TRANSFER FUNCTION AND ERROR CURVE FOR SINGLE AD640

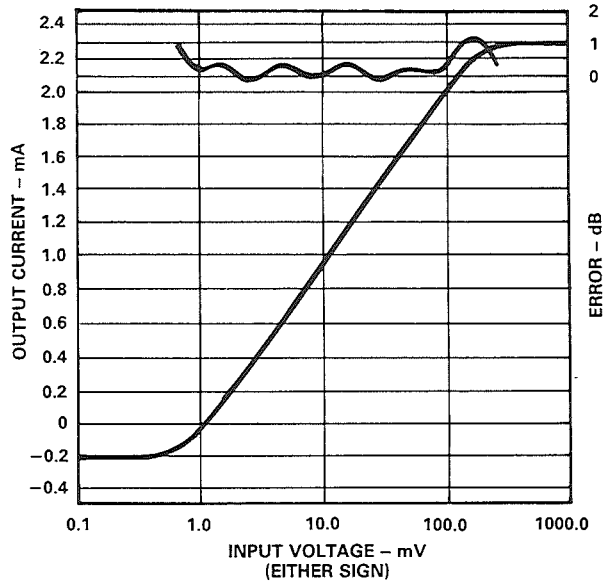


Figure 2.44

When two AD640s are cascaded , the second will be delivering an output from the noise of the first. If the full potential dynamic range is to be realized, the bandwidth must be limited because of noise. This may be done with high-pass, low-pass, or band-pass filters, depending on the required response, but, the voltage gain of these filters in their passband must be unity, or there will be a kink in the log response. Figure 2.45 shows a 70dB log amp for broadband operation from 50 to 150MHz. The 100MHz passband limits the possible dynamic range, but the performance is still exceptional. Figure 2.46 shows a 95dB 10Hz to 100kHz log amp using two cascaded AD640s.

70 dB LOG AMP FOR 50-150 MHz USING TWO AD640

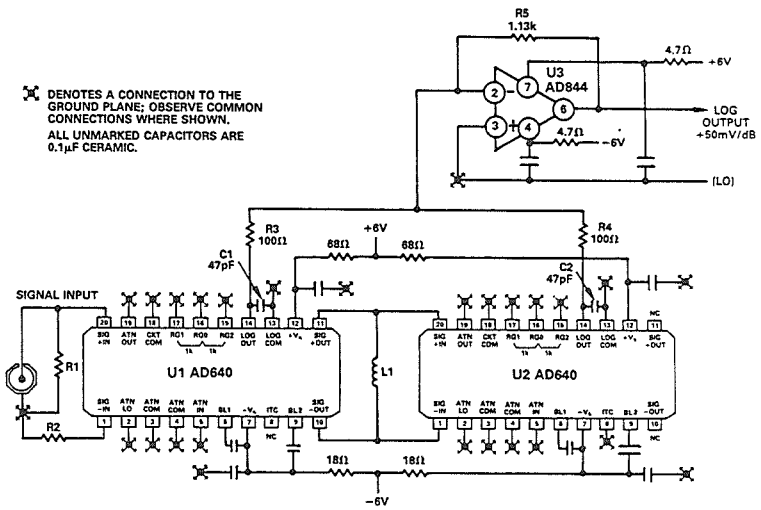


Figure 2.45

95 dB L.F. LOG AMP (10Hz - 100kHz) USING TWO AD640

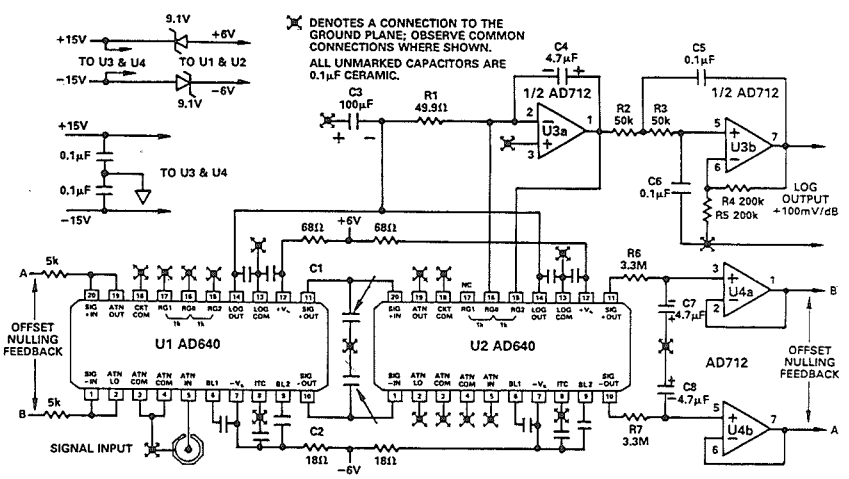
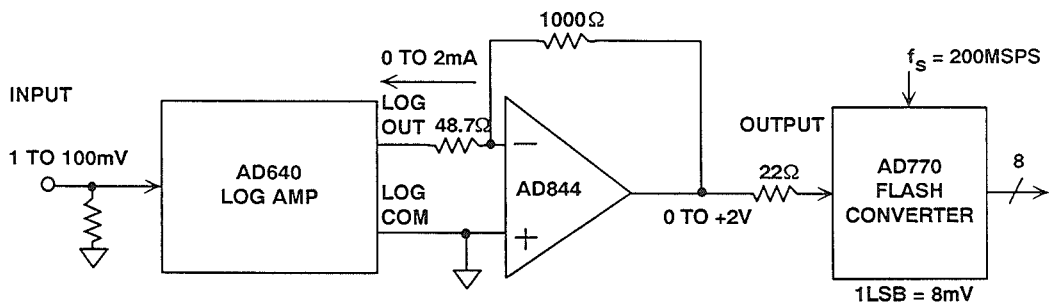


Figure 2.46

An external op amp can be used to convert the AD640 output current to a buffered output voltage as shown in Figure 2.47. The input to the AD640 (1mV to 100mV, or 40dB) results in an op amp output of 0 to 2V. If this output is applied to an 8 bit flash ADC having a corresponding input range, the weight of the ADC least significant bit (LSB) is 0.157dB reflected to the input of the AD640. For input signals near zero, the LSB value (reflected to the AD640 input) is approximately 0.02mV, while for signals approaching 100mV, the LSB value is approximately 2mV. This corresponds to an effective dynamic range of $20\log_{10}(100mV/0.02mV)$, or 74dB. The 50dB dynamic range of the 8 bit flash converter has therefore been increased to 74dB (equivalent to a 12bit ADC) through the use of the 40dB AD640 and the op amp.

A "true log", or log video amp is made up of individual cascaded gain stages, each having a small signal gain of A and a large signal (incremental) gain of unity (0dB). Each stage can be modelled as shown in Figure 2.48 as two parallel amplifiers, a limiting one with gain, and a unity gain buffer, which together feed a summing amplifier. These stages, when cascaded, form a log amp without the necessity of summing from the individual stages.

AD640 DRIVING AD770 FLASH CONVERTER



DYNAMIC RANGE

$20\log\left(\frac{111.68}{0.02}\right)$

= 75dB

	INPUT (mV)	OUTPUT (mV)
0.02	1.02	8
	1.04	16
	•	•
	•	•
	•	•
2.00	109.64	2040
	111.68	2048

Figure 2.47

STRUCTURE AND PERFORMANCE OF TRUE LOG AMPLIFIER ELEMENT AND OF A LOG AMP FORMED BY CASCADING SEVERAL SUCH ELEMENTS

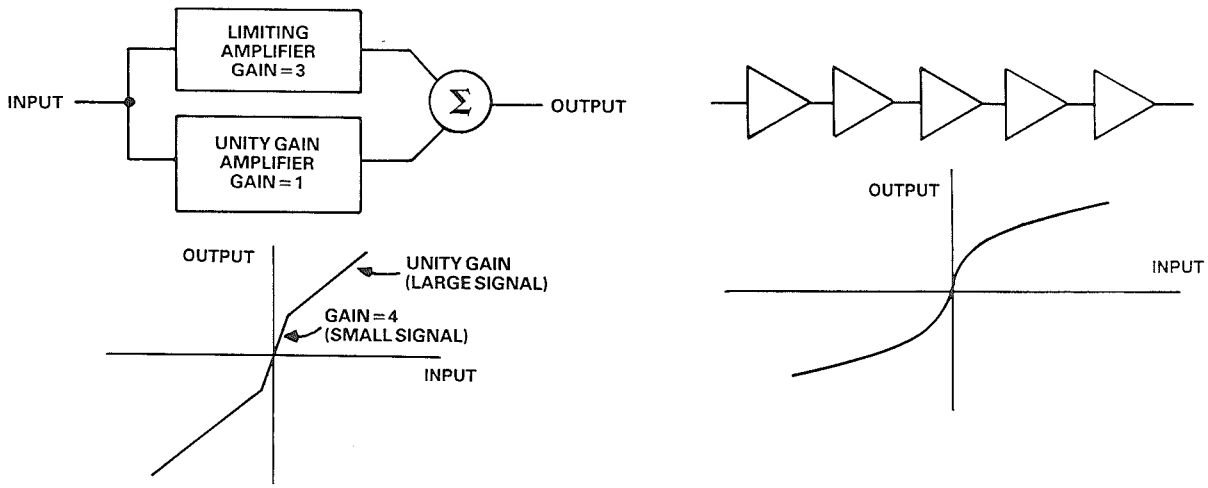


Figure 2.48

VARIABLE GAIN AMPLIFIER (ULTRASOUND APPLICATION)

A block diagram of a typical ultrasound system is shown in Figure 2.49. A burst of ultrasound energy (1 to 13MHz) is generated in an electromechanical piezoelectric transducer which physically contacts the outer body surface. The velocity of propagation of the ultrasound waves in most soft-body tissues (air and bones are the exception) is about 1500m/sec. Echoes are produced at interfaces between various types of soft-body structures. The round-trip time of each echo is used to determine its distance from the transducer.

Soft-body tissues attenuate the burst of ultrasound energy by approximately 1dB/cm/MHz. For the thicker parts of the body, as in abdominal imaging, frequencies of 1 to 2MHz are common. For imaging of shorter path lengths, as in studies of the eye or other superficial structures, frequencies as high as 20MHz can be used. Because of soft-body tissue attenuation, the receiving transducer will see a dynamic range of 100dB when scanning from 1 to 10cm at 10MHz, independent of the tissue variations that need to be observed. Add the 50dB dynamic range typical for variations in tissue, and the transducer must have close to 150dB dynamic range. For this reason, the transducer output is usually applied to a Time Gain Amplifier (TGA) whose gain in dB is directly proportional to the amount of time elapsed from the transmission of the burst (see Figure 2.50).

For reflections that are near the surface, there will be little attenuation. For deep signal returns, gain is applied to compensate for the path attenuation. The TGA thus compensates for normal signal attenuation associated with delay/distance. The receiver (ADC) therefore only sees the intensity variations associated with the different tissue types. In scans where the propagation path is primarily soft tissue structures of comparable attenuation, such as the abdomen, a fixed gain versus time function is

B-SCAN ULTRASOUND SYSTEM BLOCK DIAGRAM

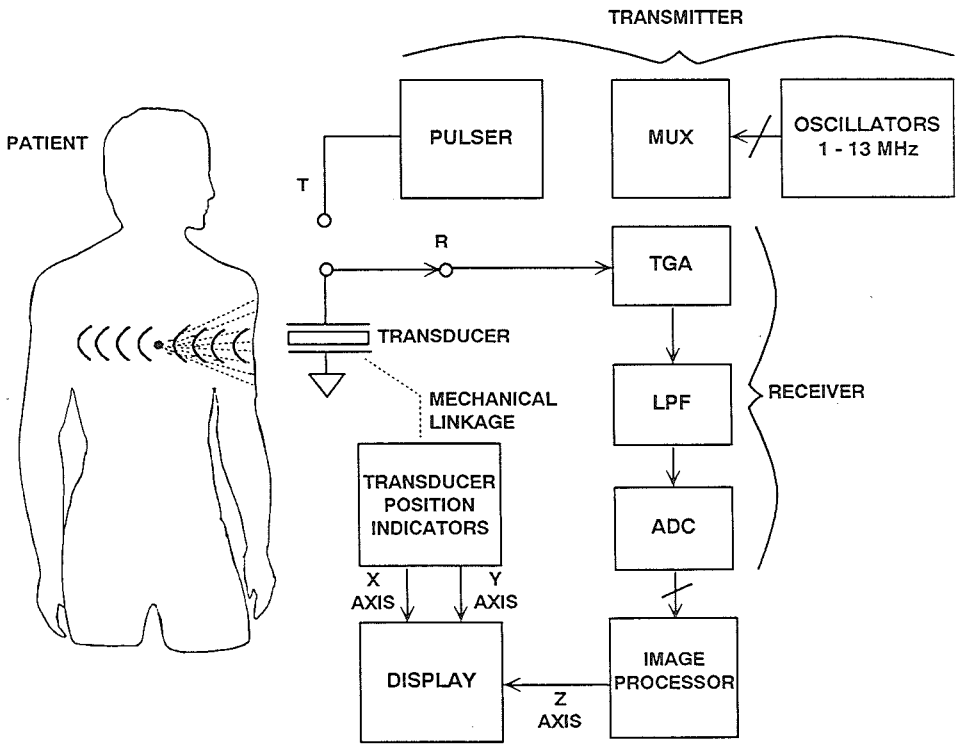


Figure 2.49

TIME GAIN AMPLIFIER

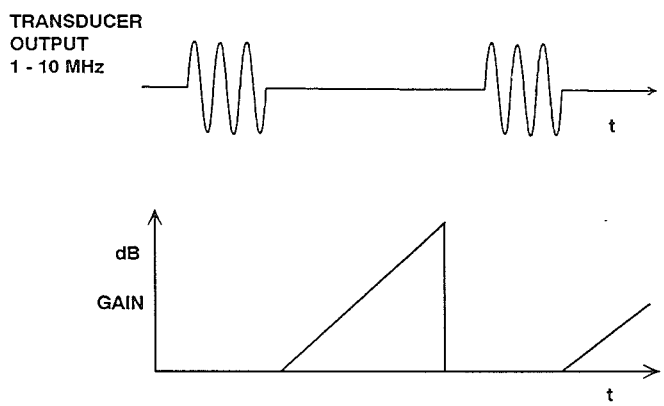


Figure 2.50

usually adequate. In other cases involving blood pools or fixed regions, it is often desirable to vary the gain versus time function. Many commercial systems make this option available. In some cases it is even desirable for the operator to calibrate the TGA on a per-patient basis in order to achieve the best diagnostic image.

In phased array ultrasound systems, the angular information is precisely determined by phasing the delays from a number of transducers (transmitted and received) to electronically select the angle to be processed. The first generation of phased array elements used analog beam forming techniques as shown in Figure 2.51. Delays at the transmitter and receiver are adjusted using variable delay filters. The next generation of phased arrays will be digital. Low cost, low power, high performance ADCs and DSPs make it practical to digitize the rf directly and digitally control the delay requirements as shown in Figure 2.52. This technique is often referred to as digital beamforming and is also being considered for use in radar systems.

The AD600 is a low-noise, variable gain amplifier optimized for use in ultrasound systems as the TGA. A block diagram is shown in Figure 2.53, and key specifications are given in Figure 2.54. The AD600 can be configured either as a dual channel device, with each channel providing 40dB of gain range, or as a single channel device providing 80dB of gain range.

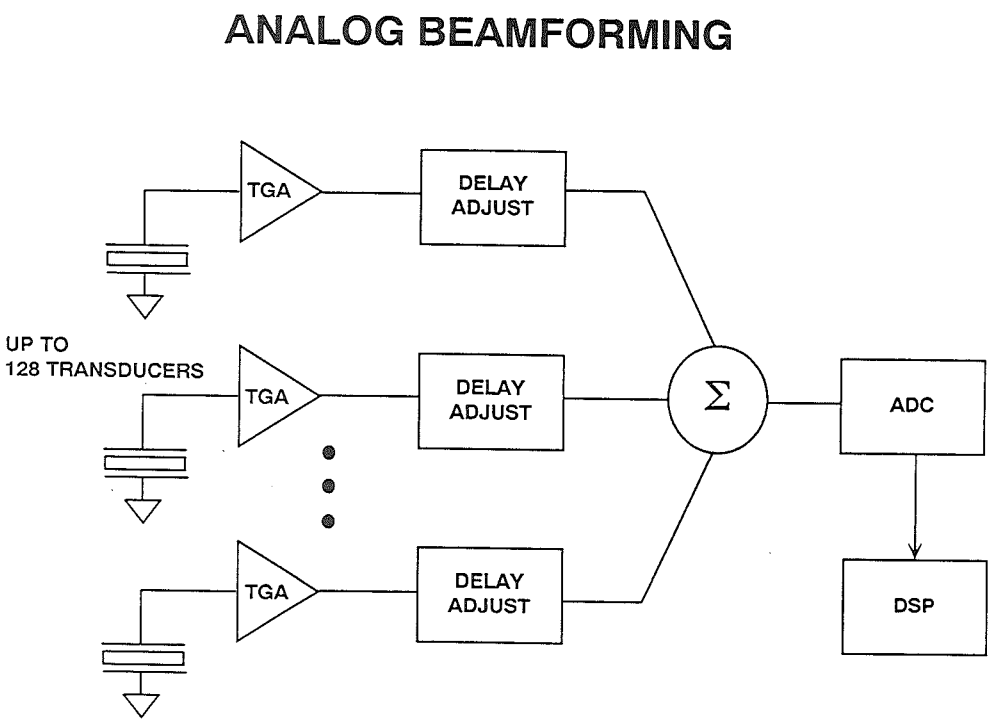


Figure 2.51

DIGITAL BEAMFORMING

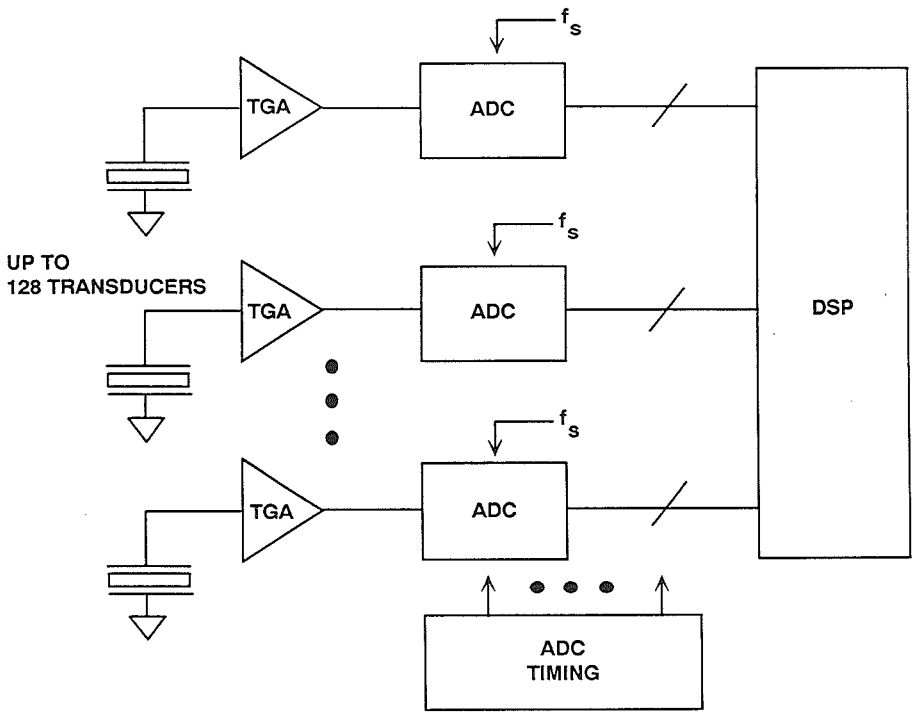


Figure 2.52

AD600 VARIABLE GAIN LOW NOISE WIDEBAND AMPLIFIER

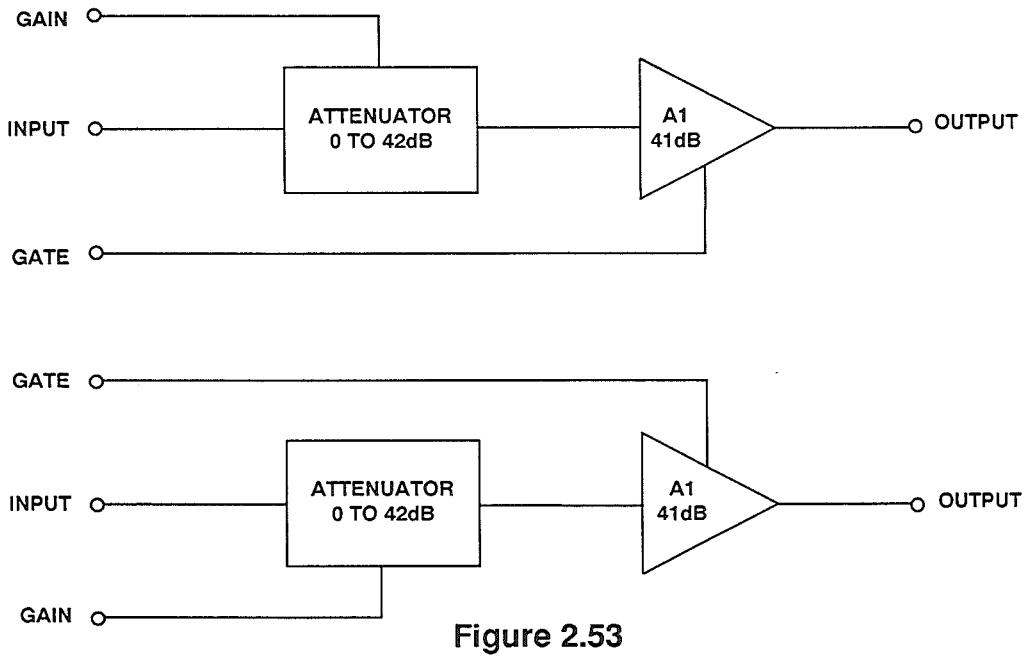


Figure 2.53

AD600 VARIABLE GAIN AMPLIFIER KEY SPECIFICATIONS

- Two independently controlled variable gain amplifiers
- Dual channel configuration with 40dB gain control range
- Single channel configuration with 80dB gain control range
- Signal gating for each channel
- 30MHz 3dB bandwidth
- Low Distortion: -60dB THD
- 32dB per volt scaling factor
- ± 2.5V output into 200Ω load
- ± 5V supplies, 125mW power consumption
- Ideal for Ultrasound applications

Figure 2.54

Each variable gain amplifier comprises a low distortion fixed-gain (41dB) feedback amplifier , preceded by a voltage-controlled attenuator (0 to -42dB), and gain-control circuitry for smoothly interpolating the attenuator. The differential high impedance control inputs have a scale factor of 32dB/V. In addition to the gain-control inputs, each amplifier has an independent gating function which blocks transmission and sets the amplifier's dc output level to within a few millivolts of the output ground. An internal voltage reference is used to calibrate all scaling parameters. The 3dB bandwidth of each variable amplifier is nominally 35MHz and is essentially independent of gain setting. Typical input noise spectral density is $1.4nV/\sqrt{Hz}$. Signal to noise ratio in a 1MHz bandwidth is 76dB, and total harmonic distortion is greater than 60dB.

Figure 2.55 shows the AD600 interfaced with the AD9060 (10 bits, 60MSPS) flash converter. The gain-control input is a linear ramp which is generated at the appropriate time with respect to the transmission. This example clearly demonstrates the power of the combination of analog and digital signal processing to solve a system problem. In order to provide the same dynamic range without the TGA (i.e. the ADC interfaces directly to the transducer via a fixed-gain preamp), the ADC would have to have a dynamic range of approximately 100dB. This implies a 16 bit ADC which would have to operate at a sampling frequency of at least 30MSPS — a requirement which is clearly beyond the present state of the art in ADC technology!

SINGLE CHANNEL AD600/AD9060 INTERFACE FOR ULTRASOUND

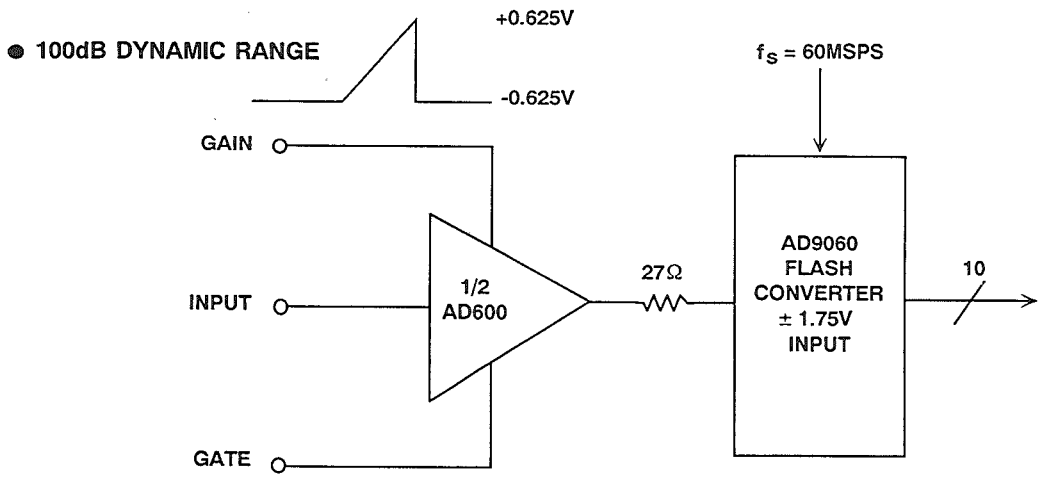


Figure 2.55

PASSIVE AND ACTIVE ANALOG FILTERING

Filtering is an important part of analog signal processing. Filtering can be used to reduce unwanted signals, limit bandwidth, help recover wanted signals, minimize aliasing in sampled data systems, and smooth the output of DACs. There are five classes of filters. *Lowpass* filters pass all frequencies below the cutoff frequency and block all frequencies above the cutoff frequency. *Highpass* filters are the inverse of the lowpass filters. They block the low frequencies and pass those above the cutoff frequency. *Bandpass* filters pass those frequencies between the lower cutoff and upper cutoff frequencies and reject all others. *Bandstop* filters are the inverse of bandpass filters. They reject frequencies between the cutoff frequencies and pass all others. *Allpass* filters pass all frequencies equally but introduce a predictable phase delay to the signal.

CLASSES OF PASSIVE AND FILTERS

- Lowpass
- Highpass
- Bandpass
- Bandstop
- Allpass

Figure 2.56

Traditional filters were passive, that is designed with no active elements. Active components were too costly and had very poor performance characteristics. Inductors, capacitors, and resisters were used to synthesize the filter. This approach has several difficulties because inductors become physically large for low frequency filters and have poor characteristics at high frequencies. There is a great deal of interaction between the different sections of the filter. Impedance levels must be precisely controlled. Close component tolerances are difficult to manufacture and maintain. Despite these limitations passive filters are still dominant at high frequencies, primarily due to dynamic performance limitations of op amps.

PASSIVE FILTERS

- Designed with Inductors, Capacitors, Resistors
- Large Inductors Required for Low Frequency Filters
- Interaction Between Filter Stages
- Component Tolerances Difficult to Manufacture and Maintain
- Still the Only Solution at High Frequencies Due to Active Component Limitations

Figure 2.57

Active filters answer some of the limitations of the passive filter by offering isolation between stages and eliminating the need for inductors. Their use at high frequencies is limited by the dynamic performance of the active elements.

ACTIVE FILTERS

- Eliminate Need for Inductors
- Good Interstage Isolation
- High Frequency Use Limited by Op Amp Dynamic Performance

Figure 2.58

A filter can be specified in terms of five parameters as shown in Figure 2.59. The *cutoff frequency* F_c is the frequency at which the filter response leaves the error band (or the -3dB point for a Butterworth filter). The *stopband frequency* F_s is the frequency at which the minimum attenuation in the stopband is reached. The *passband ripple* A_{max} is the variation (error band) in the passband response. The *minimum passband attenuation* A_{min} defines the signal attenuation within the stopband. The *order* M of the filter is the number of poles in the transfer function.

KEY FILTER DESIGN PARAMETERS

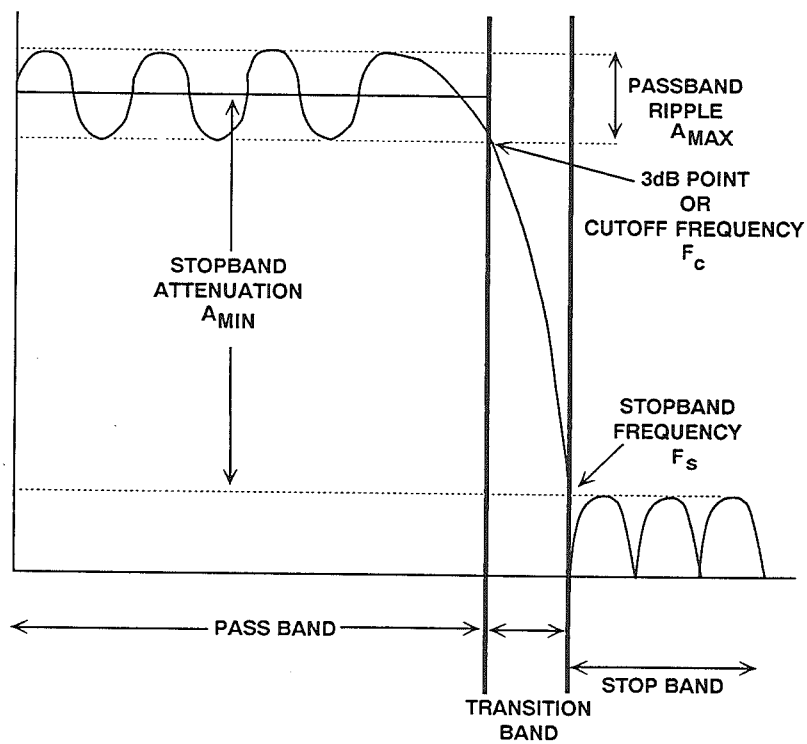


Figure 2.59

FILTER SPECIFICATIONS

- Cutoff Frequency, F_c
- Stopband Frequency, F_s
- Passband Ripple, A_{max}
- Stopband Attenuation, A_{min}
- Filter Order, M

Figure 2.60

Typically, one or more of the above parameters will be variable. For instance, if you were to design an antialiasing filter for an ADC you will know the cutoff frequency, the stopband frequency, and the minimum attenuation. You can then go to a chart or computer program to determine the other parameters.

There are many transfer functions that may satisfy the requirements of a particular filter. The *Butterworth* filter is the best compromise between attenuation and phase response. It has no ripples in the passband or the stopband and is called the *maximally flat filter* because of this. The Butterworth filter achieves its flatness at the expense of a relatively wide transition region from passband to stopband.

The *Chebyshev* filter has a smaller transition region than the same-order Butterworth filter, but it has ripples in either its passband or stopband. This filter gets its name because the Chebyshev filter minimizes the height of the maximum ripple—this is the Chebyshev criterion.

The Butterworth filter and the Chebyshev filter are all-pole designs. By this we mean that the zeros of the transfer function are at one of the two extremes of the frequency range (0 or ∞). For a lowpass filter the zeros are at $f = \infty$. We can add finite frequency transfer function zeros as well as poles to get an *Elliptical Filter*. This filter has a shorter transition region than the Chebyshev filter because it allows ripple in both the stopband and passband. The Elliptical filter also has degraded phase (time domain) response.

These are by no means all possible transfer functions, but they do represent the most common.

POPULAR FILTER DESIGNS

- **Butterworth: All Pole, No Ripples in Passband or Stopband, Maximally Flat Response**
- **Chebyshev: All Pole, Ripple in Passband, Shorter Transition Region than Butterworth for Given Number of Poles**
- **Elliptical: Ripple in Both Passband and Stopband, Shorter Transition Region than Chebyshev, Degraded Phase Response, Poles and Zeros**

Figure 2.61

Once the order of the filter and the specifications of filter have been determined, the design charts (see Reference 10) or computer programs are consulted, and the linear and quadratic factors of poles for the transfer function are determined. All filters, regardless of order, are made up of one- or two-pole sections. The single pole section is defined by its resonant frequency, which is the -3dB point. The pole pair in a two-pole filter section is defined by its resonant frequency (F_o) and Q, which indicates the peaking of the section. Sometimes alpha (α) is used instead of Q ($Q=1/\alpha$).

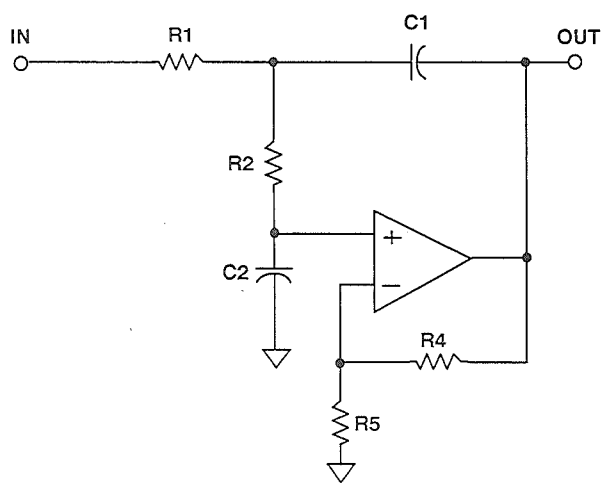
Armed with the various values F_o and Q, you then choose the configuration for the realization of the filter: Butterworth, Chebyshev, or Elliptical.

For passive filters, these values, along with the filter characteristic impedance determine the inductor, capacitor, and resistor values.

For active filters, you must decide which of the realizations you are going to use. The three most common are the *Sallen-Key* (voltage controlled voltage source), *multiple feedback*, and *state variable*. Each realization has its own advantages and disadvantages.

The Sallen-Key configuration shown in Figure 2.62 is the least dependent on the performance of the op amp, and the signal phase is maintained. For this filter the ratio of the largest resistor value to the smallest resistor value and the ratio of the largest capacitor value to the smallest capacitor value is low. The frequency term and Q terms are somewhat independent, but they are very sensitive to the gain parameter. The Sallen-Key is very Q-sensitive to element values for high Q sections. The design equations are also given in Figure 2.62.

VOLTAGE CONTROLLED VOLTAGE SOURCE (SALLEN-KEY) REALIZATION



H = Circuit Gain Below Cutoff

α = Damping Ratio = 1/Q

F_O = Cutoff Frequency

Choose C1

$K = 2\pi F_O C1$

$M = \frac{\alpha^2}{4} + H - 1$

$C2 = M\,C1$

$R1 = \frac{2}{K\alpha}$

$R2 = \frac{\alpha}{2MK}$

Choose R5

$R4 = R5(H - 1)$

For H = 1, R4 = 0, R5 = Open

Figure 2.62

The multiple feedback realization shown in Figure 2.63 uses an op amp in the inverting configuration. The dependence on the op amp parameters are greater than in the Sallen-Key realization. It is hard to generate high Q sections due to the limitations of the open loop gain of the op amp. The maximum to minimum component value ratios are higher than in the Sallen-Key realization. The design equations are also given in Figure 2.63.

The state-variable realization shown in Figure 2.64 offers the most precise implementation, at the expense of many more circuit elements. All parameters can be adjusted independently, and lowpass, highpass, and bandpass outputs are all available simultaneously. The gain of the filter is also independently variable. Since all parameters of the state variable filter can be adjusted independently, component spread is minimized. Also variations due to temperature and component tolerances are minimized. The design equations for the state variable filter are given in Figure 2.64.

Another active filter realization that has recently become more popular is the *Frequency Dependent Negative Resistor* (FDNR), which is a subset of the *General Impedance Converter* (GIC). In the FDNR the passive realization goes through a transformation by 1/s. Therefore inductors, whose impedance is sL, transform into a resistor of value L. Similarly, a resistor of value R becomes a capacitor of value R/s. A capacitor of impedance 1/sC transforms into a frequency dependent variable resistor, which is given the designation D. Its impedance is $1/s^2C$. The transformations to the FDNR configuration and the GIC implementation of the D element are given in Figure 2.65.

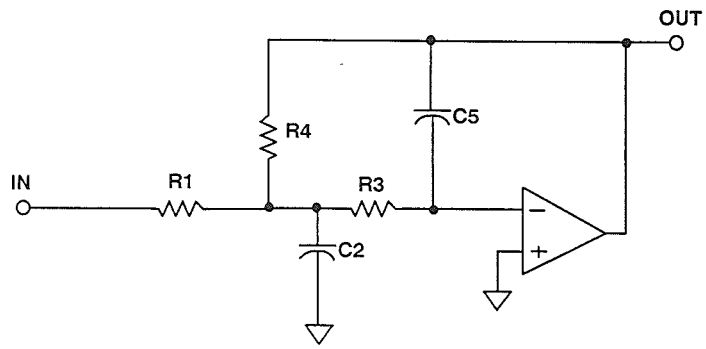
The advantage of the FDNR realization is that there are no op amps in the signal path which can add noise. This realization is also relatively insensitive to component variation. The advantages of the FDNR come at the expense of an increase in the number of components required.

For all of the realizations discussed above, the tabulated filter values are in terms of the lowpass function normalized to a frequency of 1 radian/second with an impedance level of 1. To realize the final design, the filter values are scaled by the appropriate frequency and impedance.

Similarly, the lowpass prototype is converted to a highpass filter by scaling by 1/s in the transfer function. In practice this amounts to capacitors becoming inductors with a value 1/C and inductors becoming capacitors with a value of 1/L for passive designs. For active designs resistors become capacitors with a value of 1/R, and capacitors become resistors with a value of 1/C.

Transformation to the bandpass response is a little more complicated. If the corner frequencies of the bandpass are widely separated (by more than 2 octaves) the filter is made up of separate lowpass and highpass sections. In the case of a narrowband bandpass filter the design is much more complicated and is usually done using a computer program or design tables.

MULTIPLE FEEDBACK REALIZATION



F_O = Cutoff Frequency

α = Damping Ratio = 1/Q

H = Absolute Value of Circuit Gain

Choose C5

$K = 2\pi F_O C1$

$C2 = \frac{4C5}{\alpha^2}(H + 1)$

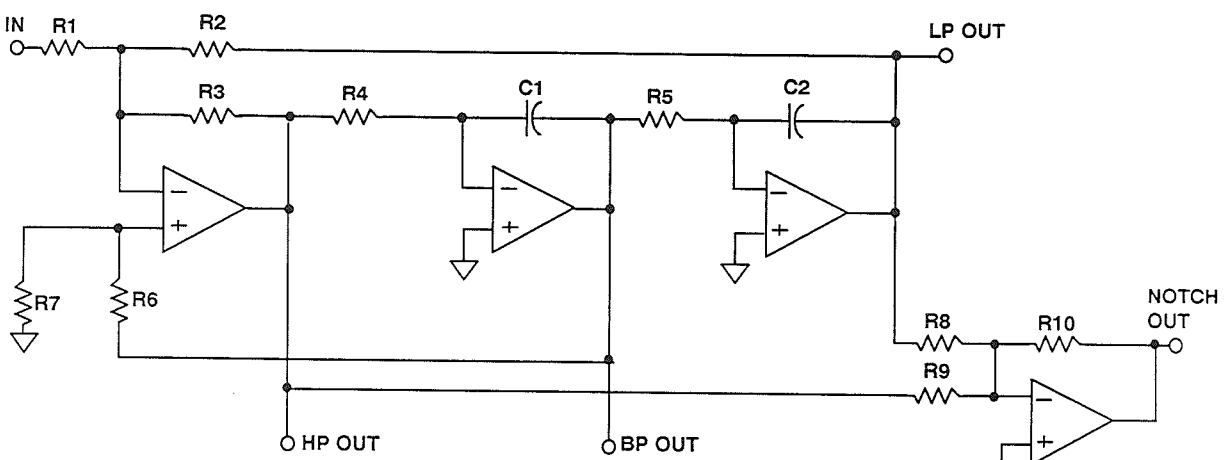
$R1 = \frac{\alpha}{2HK}$

$R3 = \frac{\alpha}{2K(H + 1)}$

$R4 = HR1$

Figure 2.63

STATE VARIABLE REALIZATION



LOWPASS GAIN = -R2/R1

HIGHPASS GAIN = -R3/R1

$$\text{BANDPASS GAIN} = \frac{R6 + R7}{R1R7\left(\frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3}\right)}$$

$$F_O = \frac{1}{2\pi}\sqrt{\frac{R3}{R2 \cdot R4 \cdot R5 \cdot C1 \cdot C2}}$$

$$Q = \frac{1}{\alpha} = \frac{R6 + R7}{R7}\left(\frac{1}{\frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3}}\right)\sqrt{\frac{R4 \cdot C1}{R2 \cdot R3 \cdot R5 \cdot C2}}$$

FOR NOTCH FREQUENCY = F_Z

FOR $F_O = F_Z$, $\frac{R2 \cdot R9}{R3 \cdot R8} = 1$

FOR $F_O > F_Z$, $\frac{R2 \cdot R9}{R3 \cdot R8} < 1$

FOR $F_O < F_Z$, $\frac{R2 \cdot R9}{R3 \cdot R8} > 1$

$$\frac{F_Z^2}{F_O^2} = \frac{R2 \cdot R9}{R3 \cdot R8}$$

Figure 2.64

FREQUENCY DEPENDENT NEGATIVE RESISTOR 1/S IMPEDANCE TRANSFORMATION

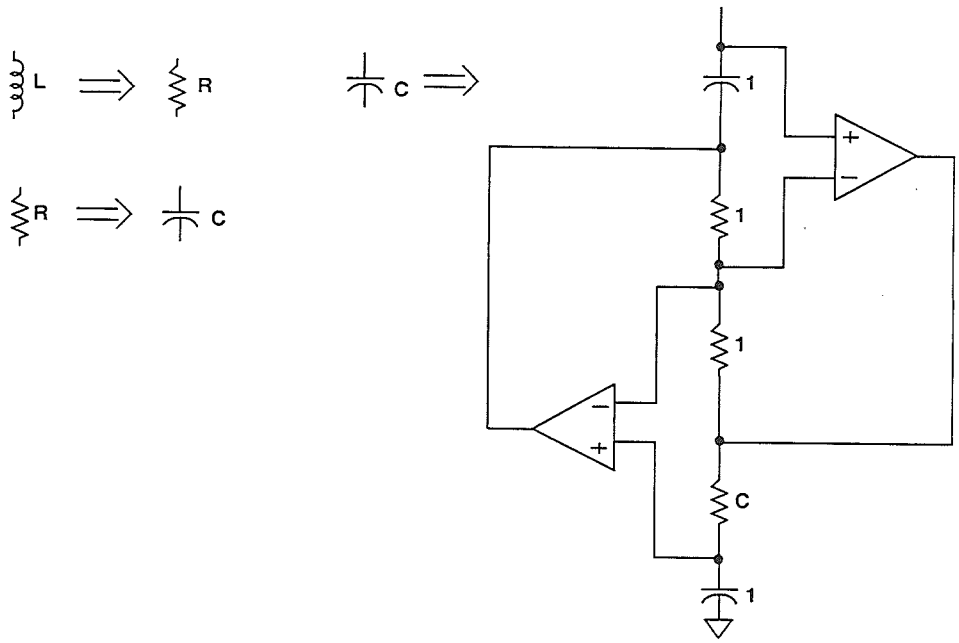


Figure 2.65

SOME ACTIVE FILTER REALIZATIONS

- Sallen-Key: Good Phase Response, Least Dependent on Op Amp Performance, Sensitive to Element Values for High Q Sections
- Multiple Feedback: Less Sensitive to Element Values, High Q Sections Difficult due to Op Amp Open Loop Gain Limitations
- State-Variable: Most Precise, More Components, All Parameters Independently Adjustable
- Frequency Dependent Negative Resistance (FDNR): Op Amps not in Signal Path, More Components, Relatively Insensitive to Component Variations

Figure 2.66

ANTIALIASING FILTER DESIGN EXAMPLE

We will now design a passive and active antialiasing filter based upon the same specifications. The active filter will be designed in four realizations: Sallen-Key, multiple feedback, state variable, and Frequency Dependent Negative Resistance (FDNR). We choose the Butterworth filter in order to give the best compromise between attenuation and phase response.

The specifications for the filter are as follows:

ANTIALIASING FILTER SPECIFICATIONS

- Cutoff Frequency F_c = 8kHz
- Stopband Attenuation F_s at 50kHz = 70dB
- Best Balance Between Attenuation and Phase Response
- Choose Butterworth Design
- From Design Charts, for f = 6.25 (50kHz/8kHz), M = 5

Figure 2.67

Consulting the design charts (Reference 10, p. 82), we see that for 70dB of attenuation at a frequency of 6.25 (50kHz/8kHz) a fifth order filter is required.

We now consult the tuning tables (Reference 10, p. 341) and find:

ALPHA AND F_0 VALUES FROM TUNING TABLES

STAGE	ALPHA	F_0
1	---	1.000
2	1.618	1.000
3	0.618	1.000

Figure 2.68

The first stage is a real pole, thus the lack of an alpha value. It should be noted that this is not necessarily the order of implementation in hardware. In general you would typically put the real pole last and put the second order sections in order of decreasing alpha (increasing Q).

For the passive design we will choose the zero input impedance configuration. From the design table (Reference 10, p. 313) we find the following normalized values for the filter:

NORMALIZED PASSIVE FILTER VALUES FROM TABLES

L1 = 1.5451 C2 = 1.6944

L3 = 1.3820 C4 = 0.8944

L5 = 0.3090

Figure 2.69

These values are for a 1 rad/second filter with a 1 ohm termination. To scale the filter we divide all reactive elements by the desired cutoff frequency, 8kHz (50265 rad/sec). We also need to scale the impedance. For this example, we choose a value of 1000 ohms. To scale the impedance we multiply all resistor and inductor values and divide all capacitor values by the impedance scaling factor. After scaling, the circuit looks like Figure 2.70.

For the Sallen-Key active realization, we use the design table shown in Figure 2.62. The values for C1 in each section are chosen to give reasonable resistor values. The implementation is shown in Figure 2.71. For the Sallen-Key realization to work correctly, it is assumed to have a zero-impedance driver and a return path for dc. Both of these criteria are approximately met when you use an op amp to drive the filter.

EXAMPLE FILTER PASSIVE IMPLEMENTATION

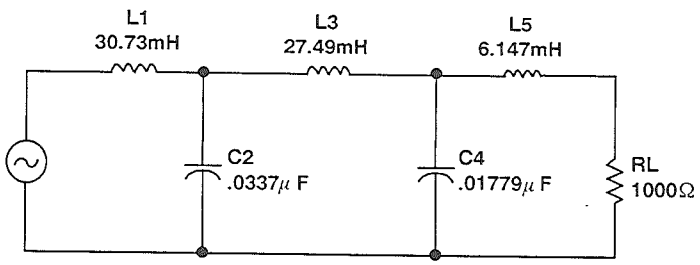


Figure 2.70

EXAMPLE FILTER
SALLEN-KEY IMPLEMENTATION

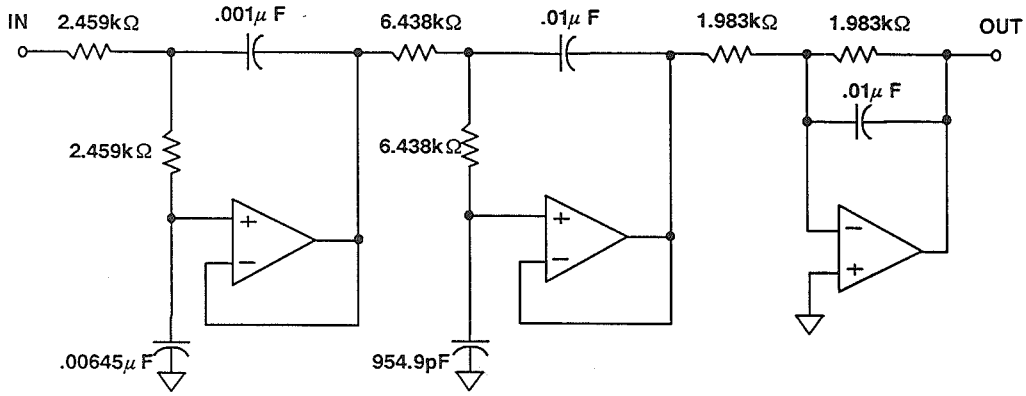


Figure 2.71

EXAMPLE FILTER
MULTIPLE FEEDBACK IMPLEMENTATION

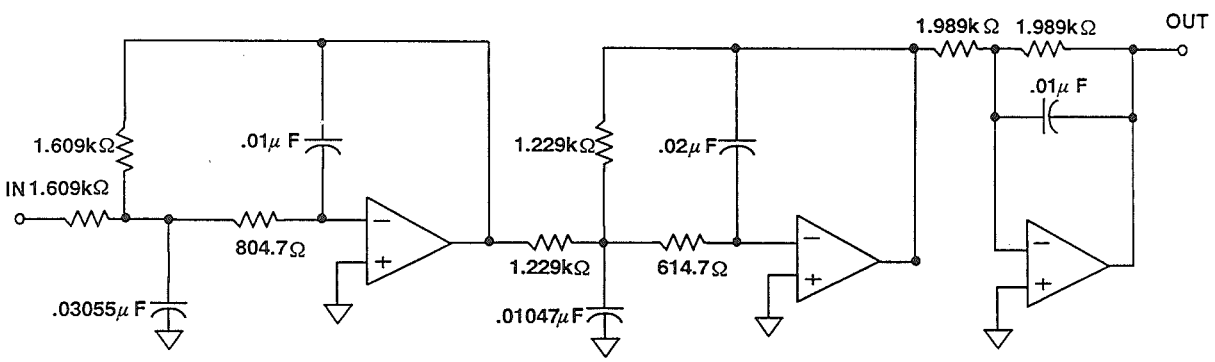


Figure 2.72

EXAMPLE FILTER
STATE VARIABLE IMPLEMENTATION

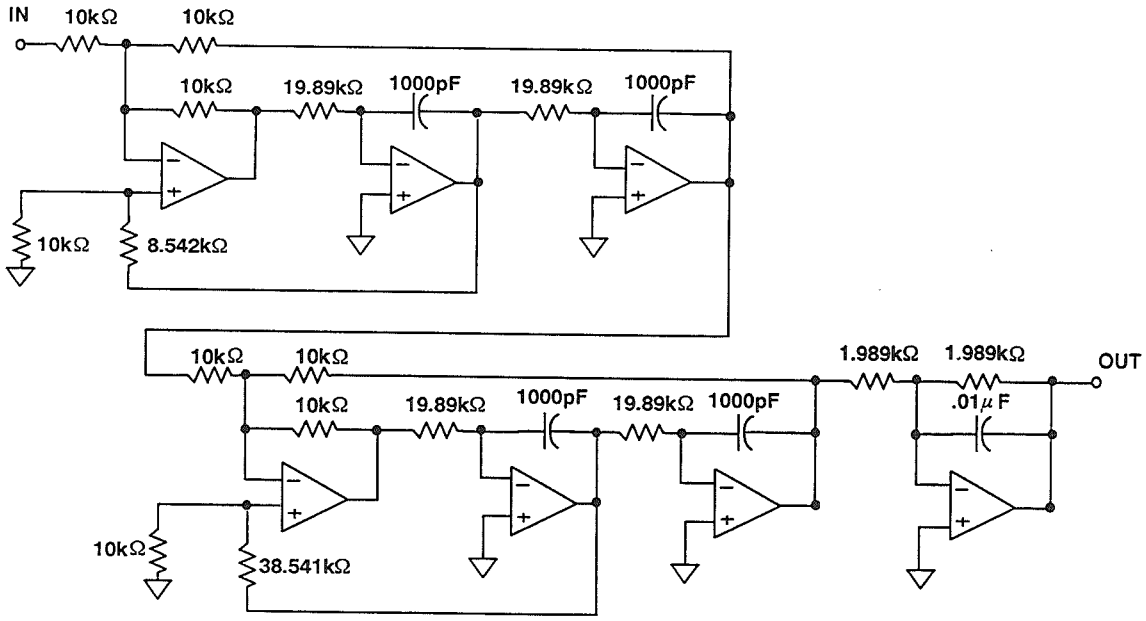


Figure 2.73

EXAMPLE FILTER
FDNR IMPLEMENTATION

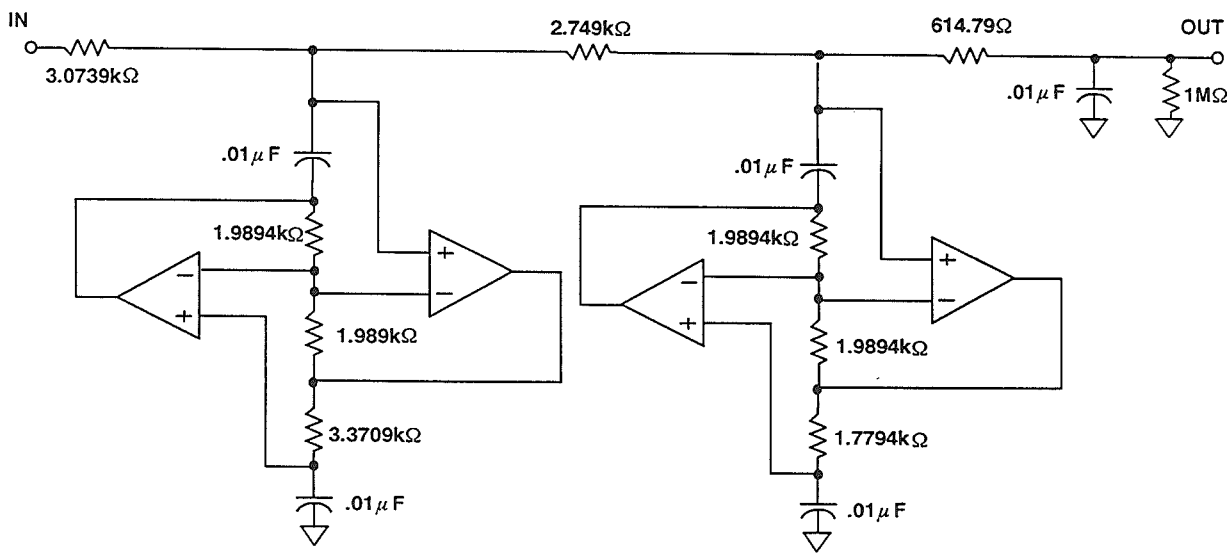


Figure 2.74

Figure 2.72 shows a multiple feedback realization of our filter. It was designed using the equations in Figure 2.63.

The state variable realization is shown in Figure 2.73, and the Frequency Dependent Negative Resistance (FDNR) realization is shown in Figure 2.74. In the conversion process from passive to FDNR, the D element is normalized for a capacitance of 1F. We then scale the filter to a more reasonable value (0.01μF in this case).

In all of the filters above the values shown are the exact calculated values. These exact values are rarely obtainable. We must therefore either substitute the nearest standard value or use series/parallel combinations. Any variation from the ideal values will cause a shift in the filter response characteristic, but often the effects are minimal. The computer can be used to evaluate these variations on the overall performance and determine if they are acceptable.

In active filter applications using op amps, the dc accuracy of the amplifier is often critical to optimal filter performance. The amplifier's offset voltage will be passed by the filter and may be amplified to produce excessive output offset. For low frequency applications requiring large value resistors, bias currents flowing through these resistors will also generate an output offset voltage.

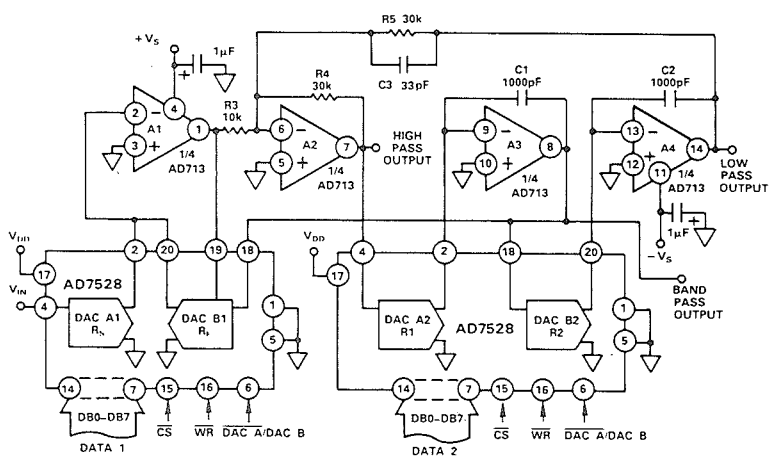
In addition, at higher frequencies, an op amp's dynamics must be carefully considered. Here, slewrate, bandwidth, and open loop gain play a major role in op amp selection. The slewrate must be fast as well as symmetrical to minimize distortion.

A PROGRAMMABLE STATE VARIABLE FILTER

A realization of a programmable state variable filter using DACs is shown in Figure 2.75. DACs A1 and B1 control the gain and Q of the filter characteristic, while DACs A2 and B2 must accurately track for the simple expression for f_c to be true. This is readily accomplished using two AD7528 DACs and one AD713 quad op amp. Capacitor C3 compensates for the effects of op amp and gain-bandwidth limitations.

This filter provides lowpass, highpass, and bandpass outputs and is ideally suited for applications where digital control of filter parameters is required. The programmable range for component values shown is f_c = 0 to 15kHz, and Q = 0.3 to 4.5.

A PROGRAMMABLE STATE VARIABLE FILTER CIRCUIT



CIRCUIT EQUATIONS

$C_1 = C_2$, $R_1 = R_2$, $R_4 = R_5$

$$f_C = \frac{1}{2\pi R_1 C_1}$$

$$Q = \frac{R_3}{R_4} \cdot \frac{R_F}{R_{FBB1}}$$

$$A_0 = -\frac{R_F}{R_S}$$

NOTE:
DAC equivalent resistance equals
256 x (DAC Ladder resistance) / DAC Digital Code

Figure 2.75

SEVEN-POLE FDNR 20kHz ANTIALIASING FILTER

Figure 2.76 shows a 7-pole antialiasing filter for a 2x oversampling (88.2kSPS) digital audio application. This filter has less than 0.05dB passband ripple and 19.8 ± 0.3µs delay, dc-20kHz. The filter will handle a 5V rms signal (V_s = ±15V) with no overload at any internal nodes. The frequency response of the filter is shown in Figure 2.77.

20kHz FDNR AUDIO ANTIALIASING FILTER

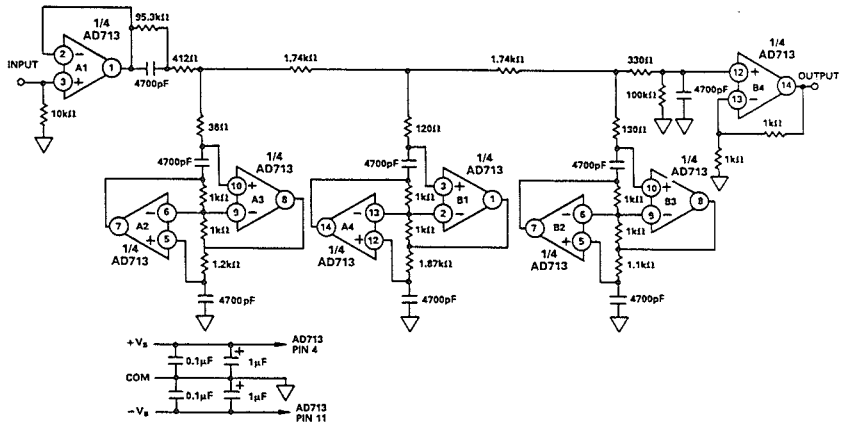


Figure 2.76

AUDIO ANTIALIASING FILTER RESPONSE

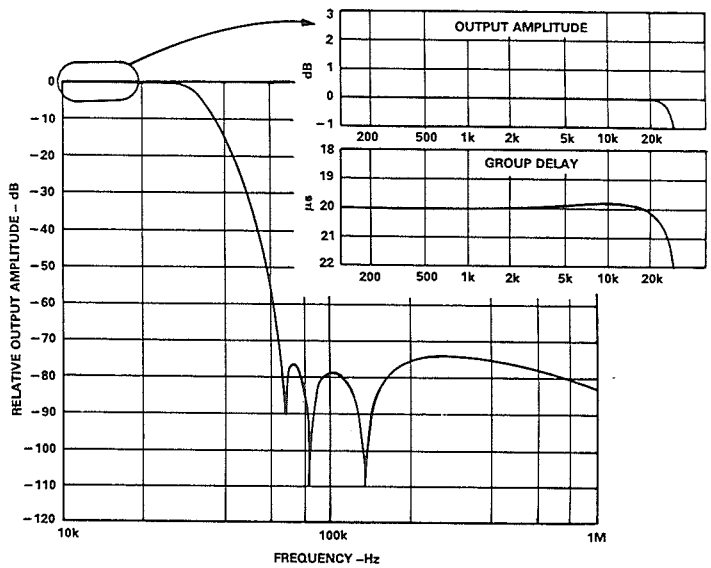


Figure 2.77

A WIDEBAND SALLEN-KEY FILTER

Figure 2.78 shows an AD843 FET input op amp used in a 1MHz Sallen-Key filter. This circuit also works well with the AD841, AD845, or AD847. The circuit is designed to be a maximum-flatness filter with a Q of 0.575 and a dc gain of 1.26. The frequency response of the filter to a 0dBm input signal is shown in Figure 2.79.

1 MHz SALLEN KEY FILTER

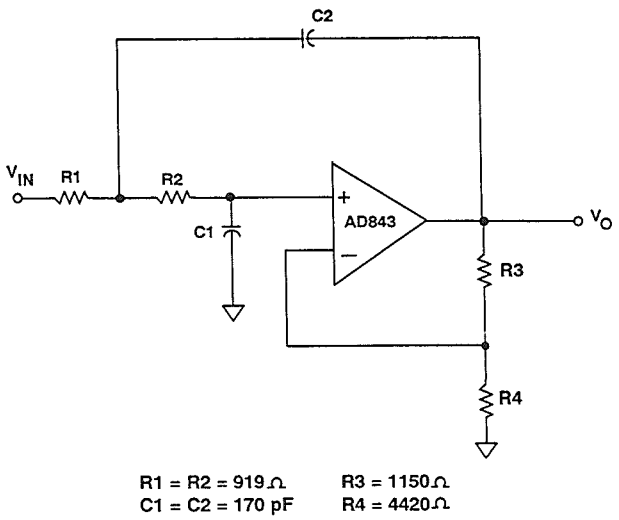


Figure 2.78

SALLEN-KEY SMALL SIGNAL FREQUENCY RESPONSE

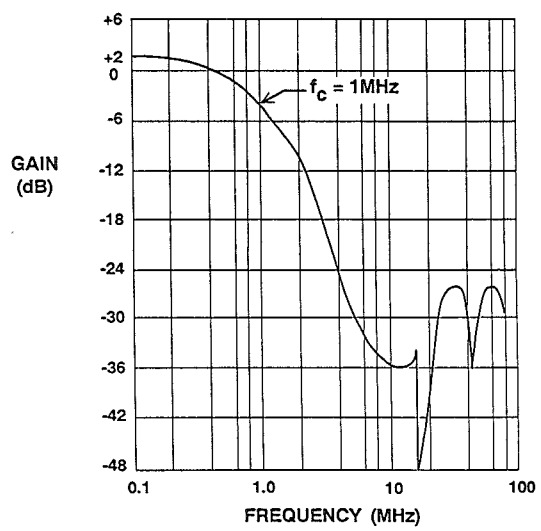


Figure 2.79

REFERENCES

1. Robert M. Clarke, Industry's Fastest Monolithic FET-Input Op Amp, **Analog Dialogue** 23-4, 1989, p.13.

2. Barrie Gilbert, **ISSCC Digest of Technical Papers 1968**, pp. 114-115 February 16, 1968

3. Barrie Gilbert, **Journal of Solid State Circuits**, Vol. SC-3, Dec. 1968, pp. 353-372.

4. Daniel H. Sheingold, Editor, **Nonlinear Circuits Handbook**, Analog Devices, 1974.

5. Charles Kitchin and Lew Counts, **RMS to DC Conversion Application Guide**, Second Edition, Analog Devices, 1986.

6. Richard Smith Hughes, **Logarithmic Amplifiers**, Artech House, Inc., Dedham, MA., 1986

7. William L Barber and Edmund R. Brown, A True Logarithmic Amplifier for Radar IF Applications, **IEEE Journal of Solid State Circuits**, Vol. SC-15, No. 3, June 1908, pp. 291-295.

8. **Broadband Amplifier Applications,** Plessey Co. Publication P.S. 1938, Sept. 1984.

9. **High Speed Design Seminar**, Analog Devices, 1990.

10. A. I. Zverev, **Handbook of Filter Synthesis**, John Wiley, 1967.

11. **AD7528 Dual 8-Bit CMOS DAC Application Note**, Analog Devices.

12. **8th Order Programmable Lowpass Analog Filter Using 12-Bit DACs**, Analog Devices.

13. **CMOS DAC Application Guide**, Analog Devices.

14. A. B. Williams, **Electronic Filter Design Handbook**, McGraw-Hill, 1981.

15. M. E. Van Valkenburg, **Introduction to Modern Network Synthesis**, John Wiley and Sons, 1960.

16. A. I. Zverev and H. J. Blinchikoff, **Filtering in the Time and Frequency Domain**, John Wiley and Sons, 1976.

17. A. Budak, **Passive and Active Network Analysis and Synthesis**, Houghton Mifflin Company, Boston, 1974.

18. L. P. Huelsman and P. E. Allen, **Introduction to the Theory and Design of Active Filters**, McGraw Hill, 1980.

19. M. S. Ghausi and K. R. Laker, **Modern Filter Design: Active RC and Switched Capacitors**, Prentice Hall, 1981.