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SECTION V

DACs FOR DSP APPLICATIONS

In order to be suitable for today's mixed-signal DSP applications, DACs must meet stringent performance specifications. In addition to traditional dc and ac specifications such as resolution, linearity, monotonicity, and settling time, DACs must be evaluated in terms of their frequency-domain dynamic performance such as SNR, THD, and oversampling ratio. DACs must be easy to interface to a variety of DSP chips with little or no additional "glue logic." Communications applications such as modems and digital mobile radio have been a driving force in the development of high performance ac-specified voiceband 12 and 14 bit DACs. The rapidly developing field of digital audio (especially compact disk players) has been a driving force in the development of low-cost, high-performance DACs having resolutions of 16 to 20 bits with complete SNR and THD dynamic specifications. In the high speed area, the raster-scan display market has a requirement for 8 and 10 bit videodacs complete with on-board memory and other functions which are specific to these applications. In the rapidly evolving direct digital synthesis market (DDS), 12 bit DACs with update rates exceeding 100MSPS are required for the generation of spectrally pure sinewaves. In addition to the above applications, the process control area continues to expand and demand high performance DACs.

HIGH-PERFORMANCE DAC APPLICATIONS

- Voiceband: Modems, Speech Synthesis, Digital Mobile Radio — 12 and 14 bits
- Audio: Professional, Compact Disk Players — 16 to 20 bits
- Raster Scan Display Systems — 8 and 10 bits
- Direct Digital Synthesis — 10 and 12 bits, > 100MSPS

Figure 5.1

DAC ARCHITECTURE

Most DACs consist of two basic elements: a set of current or voltage switches, and a method for binary division. Figure 5.2 shows two methods for constructing a DAC. In the first method, the current switches carry equal currents, and the binary scaling is done with an R-2R resistor network. The second method utilizes binarily weighted current sources whose switched outputs are summed together. In the second method, the binary current scaling is often done with an R-2R network in the emitters of the switching transistors.

In DACs fabricated on bipolar processes, current switching is most often done using non-saturating differential transistor pairs as shown in Figure 5.3. Although high performance NPN transistors are more common in bipolar processes, recent complementary bipolar (CB) processes have allowed the development of high speed DACs (such as the AD568 and AD668) based around PNP differential pairs as the basic switch element.
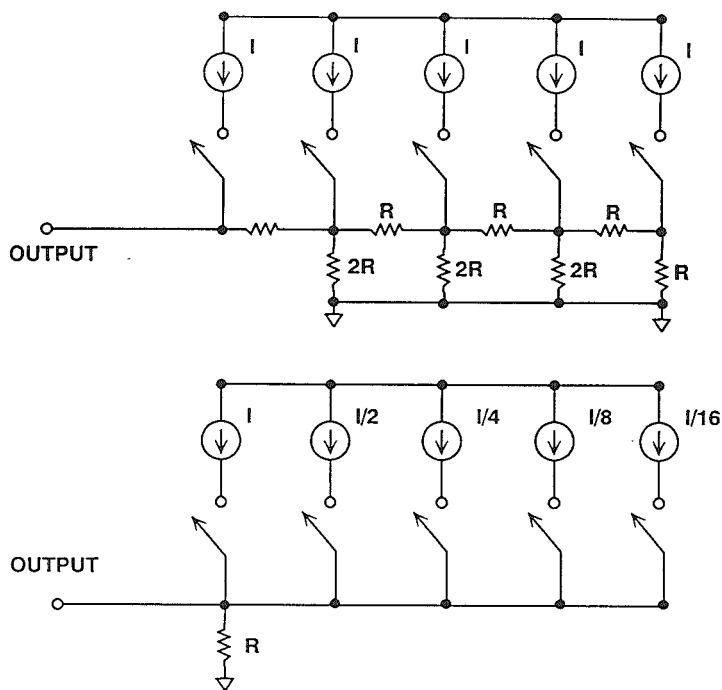
BIPOLAR DAC ARCHITECTURES

Figure 5.2

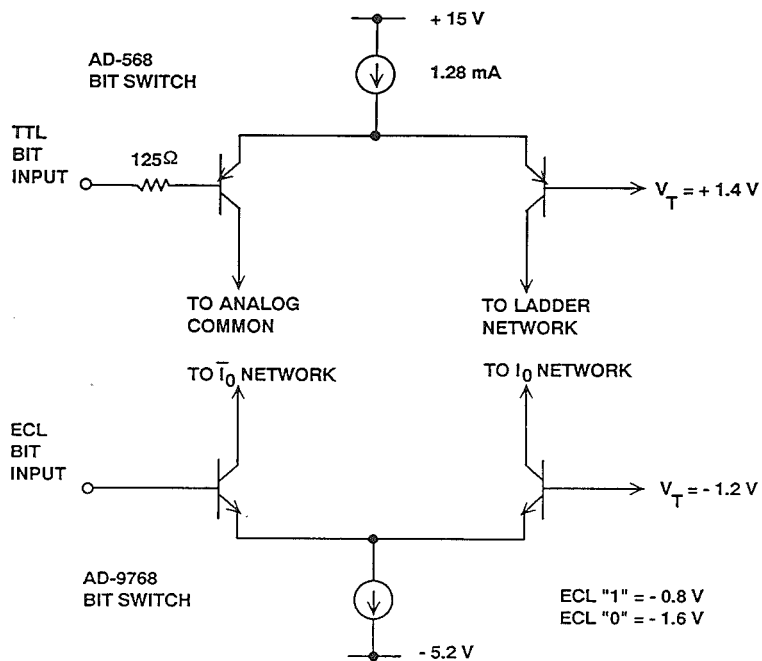## TTL AND ECL BIT SWITCHES

Figure 5.3
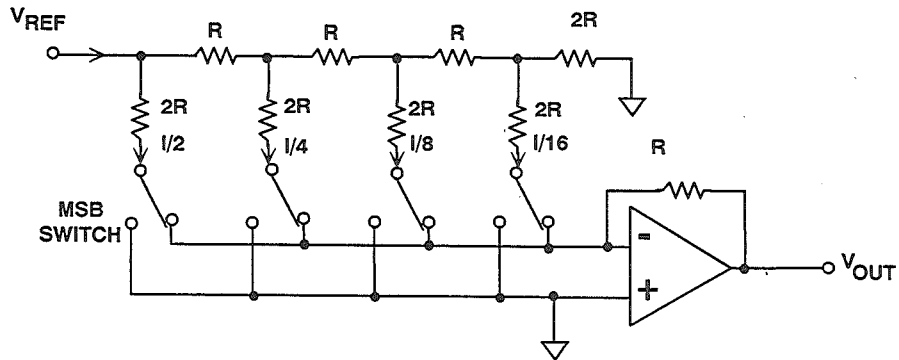
CURRENT-STEERING CMOS DAC
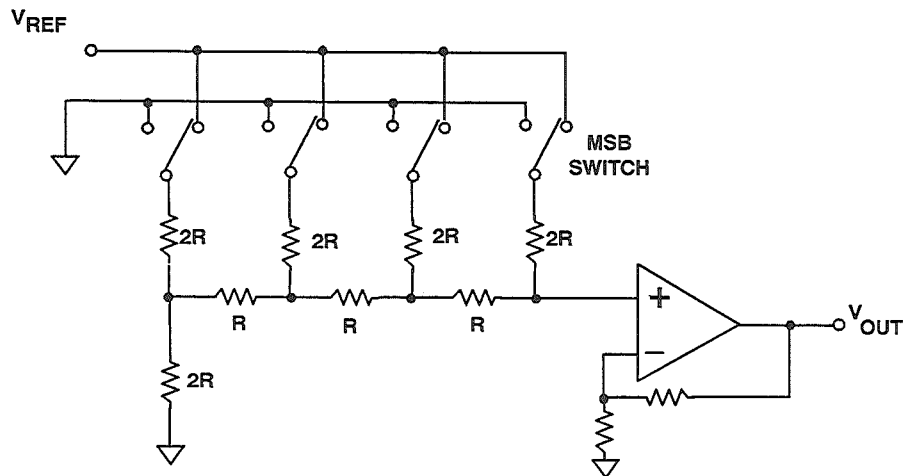

Figure 5.4

VOLTAGE-SWITCHING CMOS DAC

Figure 5.5

CMOS DACs are most commonly based on the current-mode steering circuit shown in Figure 5.4. An external reference is applied to the V_{ref} pin, and the R-2R ladder divides the input current I into binary-weighted currents as shown. The output drives the virtual ground of an inverting op amp. The finite "on" resistance of the FET switches is compensated for by placing an equivalent compensating FET in series with the feedback resistor R. CMOS DACs can also be realized which operate in the voltage-mode as shown in Figure 5.5.

For high-performance DACs in the voiceband and audio range, BiMOS processes (bipolar and CMOS devices on the same process) offer the advantages of low-power CMOS for the digital circuits (such as parallel-to-serial converters and latches) along with the low-glitch fast-switching performance of bipolar transistors. A typical current switch cell for such a DAC (the AD1860 18-bit audio DAC) is shown in Figure 5.6. The outputs of CMOS latches are level shifted by the two FETs and converted into a low-level $\pm0.8V$ differential drive for the NPN differential pair.
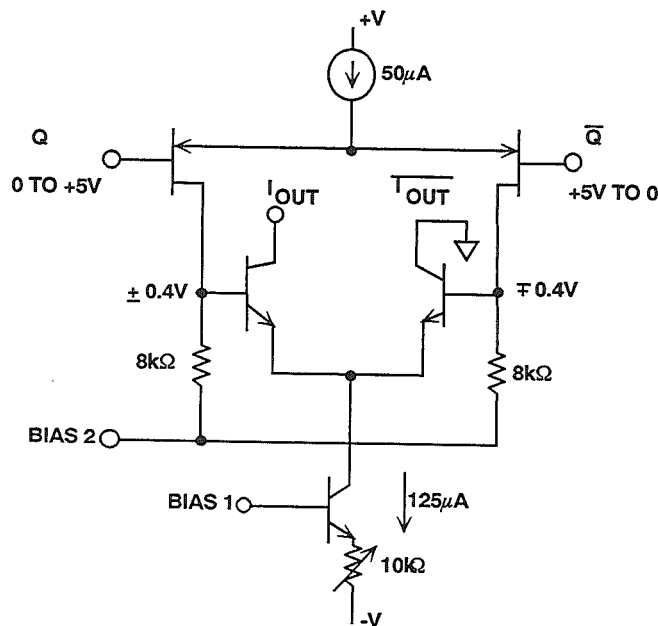
BiMOS CURRENT SWITCH

Figure 5.6

Glitch Reduction by Segmentation

If real estate, cost, power, and capacitance were of no consideration, the ideal "glitch-less" DAC would consist of $2^N - 1$ equally weighted current switches preceded by latches and decoding logic as shown in Figure 5.7. The glitch produced by switching between levels is code-independent and, therefore, does not generate harmonics of the sinewave being reconstructed. A set of latches is required after the binary decoding logic in order to equalize the delays to the actual switches themselves.

The scheme shown in Figure 5.7 is obviously not practical for high resolution DACs, but a significant amount of glitch reduction can be achieved by applying the concept to the first few MSBs. A block diagram of the segmentation technique used in the AD1860 18 bit audio DAC is shown in Figure 5.8.

The AD1860 uses a combination of segmentation and R-2R division to achieve excellent linearity and low distortion. The four MSBs are decoded into a 15 bit "thermometer" code after the serial-to-parallel conversion. The 15 decoded lines (representing the 4 MSBs) and the 14 LSB lines are then fed to a 29 bit latch. The 15 thermometer decoded lines each drive current switches having equal weights. The 14 LSB lines drive a conventional binary-weighted R-2R DAC. This combination of segmentation and conventional R-2R architecture along with laser trimmed thin film resistors allows the AD1860 to meet stringent audio specifications without the need for an external SHA deglitcher. A summary of key performance specifications for the AD1860 is given in Figure 5.9.
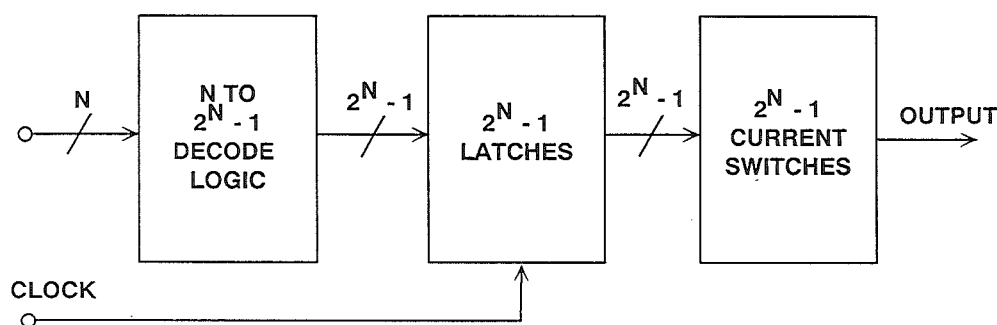
IDEAL DAC FOR MINIMUM GLITCH

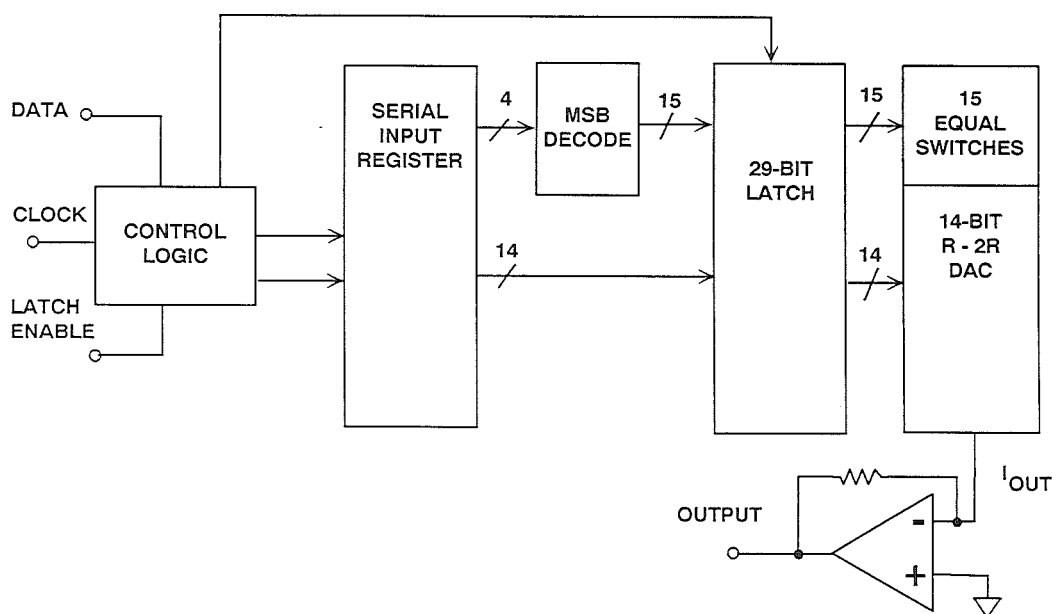Figure 5.7

SEGMENTATION IN AD1861 18-BIT AUDIO DAC

Figure 5.8

AD1861 18-BIT AUDIO DAC KEY SPECIFICATIONS

- 108dB SNR
- 0.002% THD + N @ 0dB Signal Amplitude
- Up to 16x Oversampling Capability (768kSPS)
- ±3V or ±1mA Output Capability
- 110mW Power Dissipation
- 16 Pin DIP Package

Figure 5.9

Figure 5.10 shows how the segmentation architecture is applied to the AD7840 14 bit CMOS DAC. The three MSBs of the input binary word are decoded into a 7 bit thermometer code to drive the seven switches A-G. The 11 LSBs switch an 11 bit R-2R ladder structure. A functional block diagram of the AD7840 is shown in Figure 5.11, and key specifications are given in Figure 5.12.

SEGMENTATION IN THE AD7840 14-BIT DAC

Figure 5.10

AD7840 FUNCTIONAL BLOCK DIAGRAM

Figure 5.11

AD7840 14 BIT CMOS DAC KEY SPECIFICATIONS

- ■ Complete 14 Bit Voltage Output DAC
- ■ Parallel and Serial Interface Capability
- ■ 80dB SNR
- ■ Easy Interface to DSP Processors
- ■ 100kSPS Update Rate
- ■ 100mW, ±5V Supplies

Figure 5.12

Segmentation can also be applied to voltage-mode output Bi-CMOS DACs as shown in Figure 5.13 for the AD569 16 bit DAC. The DAC consists of two resistor strings, each of which is divided into 256 equal segments. The 8 MSBs of the digital input word select one of the 256 segments on the first string. The taps at the top and bottom of the selected segment are connected to the inputs of the two buffer amplifiers A1 and A2. The buffered voltages from the segment endpoints are applied across the second resistor string, where the 8 LSBs of the digital input word select one of the 256 output taps. Output buffer A3 buffers this

voltage and delivers it to the output. Buffer amplifiers A1 and A2 leap-frog up the first string to preserve monotonicity at the segment boundaries. For example, when increasing the digital code from $00FF_H$ to 0100_H, (the first segment boundary), A1 remains connected to the same tap on the first resistor, while A2 jumps over it and is connected to the tap which becomes the top of the next segment. This design guarantees monotonicity even if the amplifiers have offset voltages. In fact, amplifier offset only contributes to integral linearity error. Key specifications for the AD569 are summarized in Figure 5.14.
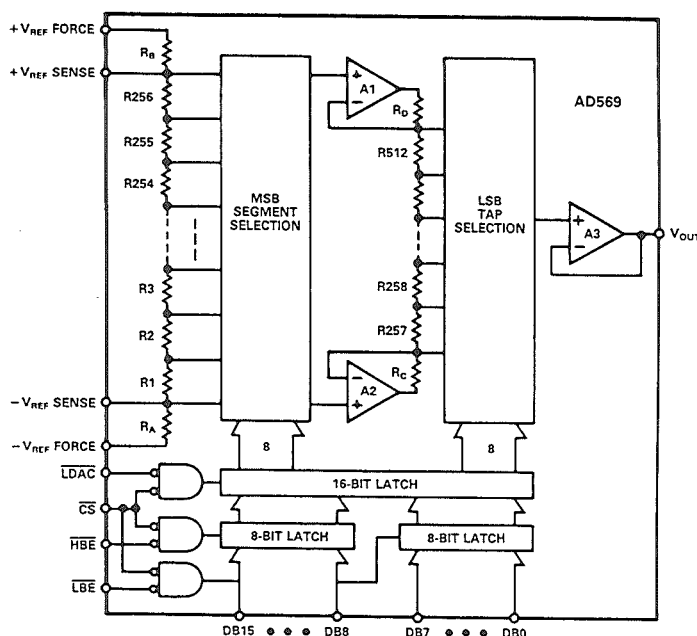
SEGMENTATION IN THE AD569 16-BIT DAC

Figure 5.13

AD569 DAC KEY SPECIFICATIONS

- ■ Guaranteed 16 Bit Monotonicity
- ■ Linear to 13 Bits
- ■ 3μs Settling to 16 Bits (0.001%)
- ■ 500nV-sec Glitch Impulse Area
- ■ 8 and 16 Bit Bus Compatibility
- ■ Low Power: 250mW

Figure 5.14

The AD7846 is another 16 bit DAC which uses the segmented architecture, and a block diagram is shown in Figure 5.15. The 4 MSBs in the DAC latch select one of the segments in a 16-resistor string. Both taps of the segment are buffered by amplifiers and fed to a 12 bit DAC which provides a further 12 bits of resolution. As with the AD569, a leap-frog approach is used to prevent non-monotonicity at the segment switching points. A summary of key specifications for the AD7846 is given in Figure 5.16.

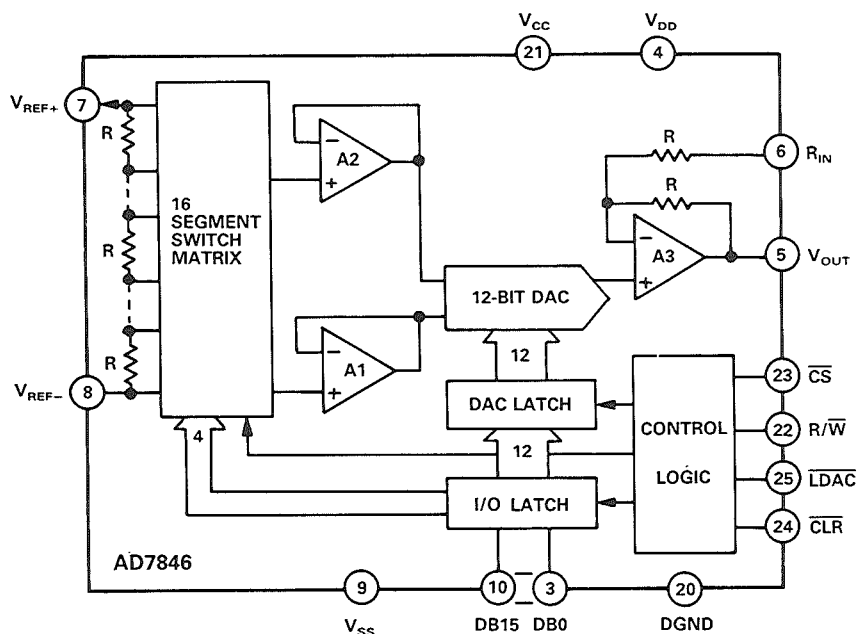## SEGMENTATION IN THE AD7846 16-BIT DAC

Figure 5.15

AD 7846 DAC KEY SPECIFICATIONS

- Guaranteed 16 Bit Monotonicity
- Linear to 15 Bits
- 9µs Settling to 0.003%
- 400nV-sec Glitch Impulse Area
- Microprocessor Compatible With Readback Capability
- Low Power: 100mW

Figure 5.16

GLITCH REDUCTION BY DIGITAL OFFSET

Regardless of the architecture used to design a high performance DAC, the most troublesome code-dependent glitch typically occurs at the midscale code transition, i.e. from 0111...1 to 1000...0. In an audio system which operates with bipolar signals, the midscale glitch noise is particularly troublesome, since it can introduce distortion for very low-level passages. If a small digital offset is added to the DAC input, then the DAC midscale glitch noise will occur at a slightly higher input signal which is less objectionable. Unfortunately, one end of the DACs range will be clipped by an amount equal to the injected digital offset as shown in Figure 5.17.

DAC WITH 1/16 FS DIGITAL OFFSET

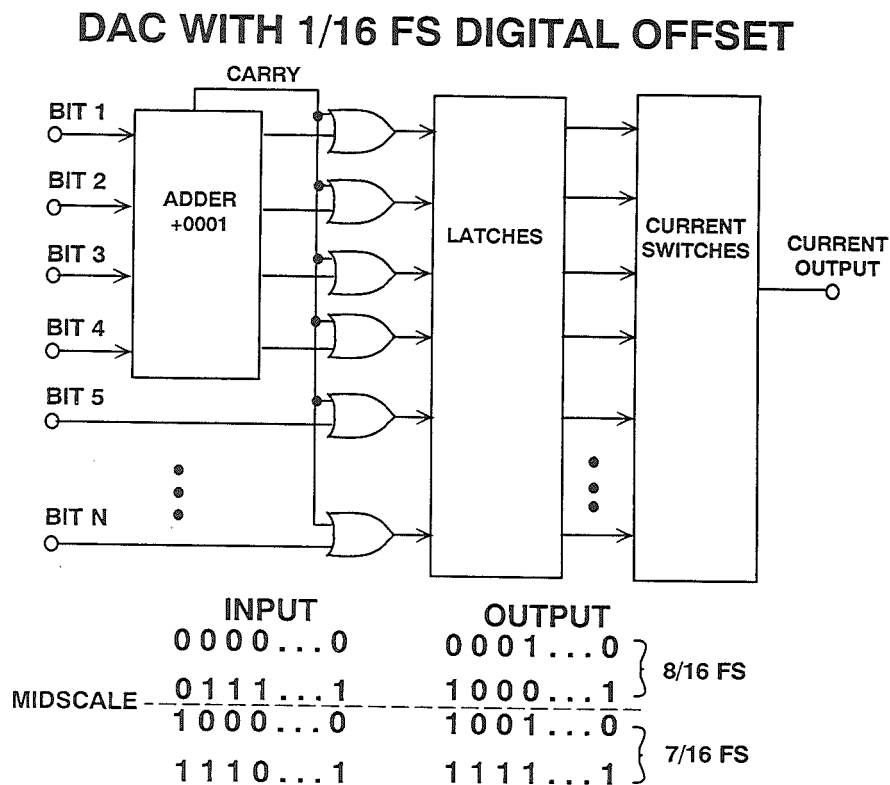|	INPUT	OUTPUT	
	0 0 0 0 . . . 0	0 0 0 1 . . . 0	8/16 FS
MIDSCALE	0 1 1 1 . . . 1	1 0 0 0 . . . 1	
	1 0 0 0 . . . 0	1 0 0 1 . . . 0	7/16 FS
	1 1 1 0 . . . 1	1 1 1 1 . . . 1	

Figure 5.17

The AD1862 20 bit digital audio DAC uses a combination of segmentation and digital offset to achieve a high level of performance. The novel architecture prevents clipping and allows the full range of the 20 bit DAC to be utilized. A block diagram of the AD1862 is shown in Figure 5.18. The digital offset is accomplished by adding 0001 (1/16th full-scale) to the four MSBs. The three MSBs are then segmented into a 7 bit thermometer code output which is latched and then drives seven equal current switches. Bit 4 (after the addition), and bits 5 through 20 are latched and then drive a conventional R-2R DAC. In order to prevent clipping at the positive end of the range, the carry output of the adder drives an additional current switch having a weight corresponding to bit 4. Finally, an offset current equal to 1/16th fullscale is subtracted from the DAC output to compensate for the constant digital offset. This architecture results in exceptional THD + N performance as shown in 5.19. Key performance specifications for the AD1862 are summarized in Figure 5.20.

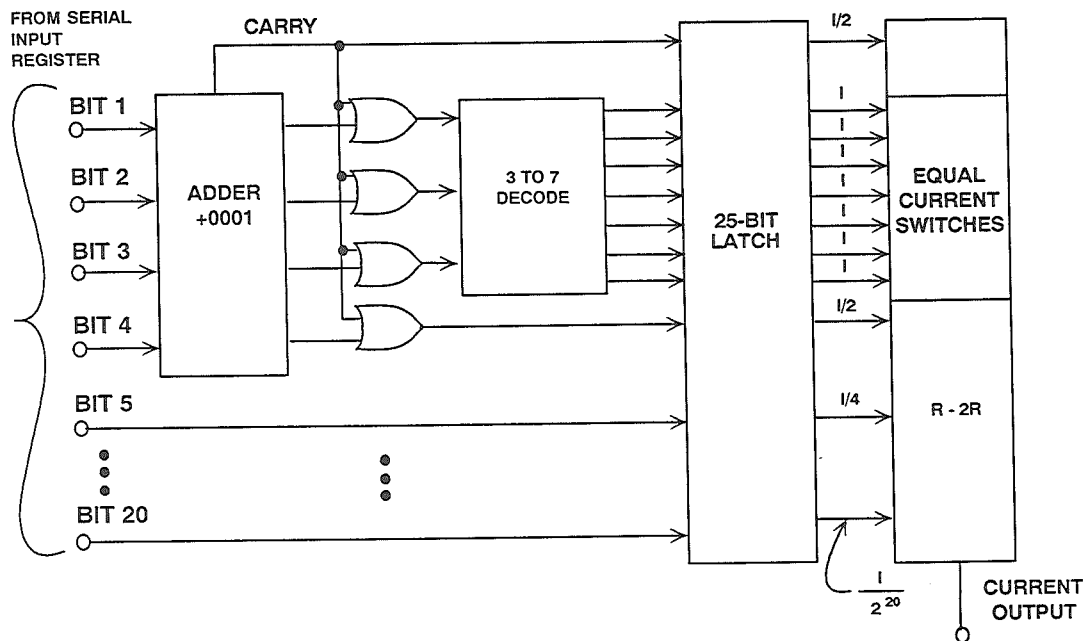## AD1862 20-BIT AUDIO DAC DIGITAL OFFSET AND SEGMENTATION

Figure 5.18

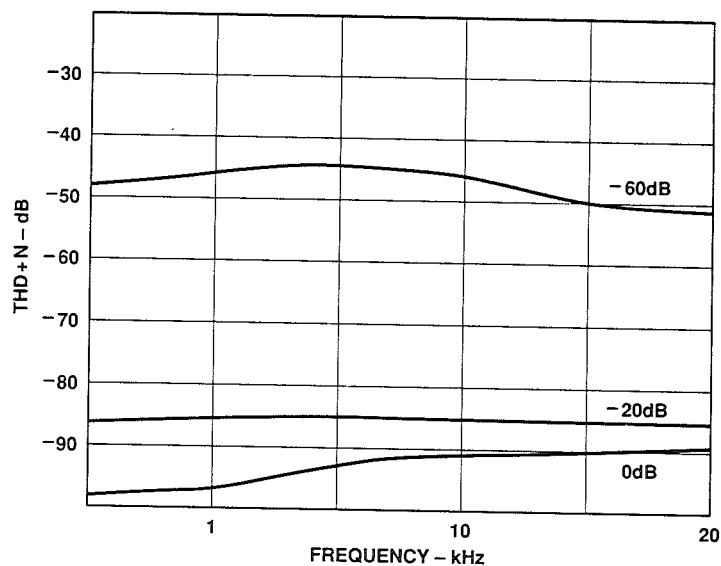## THD + N VERSUS INPUT FREQUENCY
FOR AD1862 20-BIT AUDIO DAC

Figure 5.19

AD1862 20-BIT AUDIO DAC KEY SPECIFICATIONS

- 119dB SNR
- 0.0016% THD + N @ 0dB Signal Amplitude
- 16x Oversampling Capability (705.6kSPS)
- ±1dB Gain Linearity @ -90dB Amplitude
- ±1mA Output Current
- 288mW Power Dissipation
- 16 Pin DIP Package

Figure 5.20

DEGLITCHING DACs WITH TRACK-AND HOLDS

As has been previously mentioned, code-dependent glitches can be effectively removed with a SHA as shown in Figure 5.21. Just prior to latching new data into the DAC, the SHA is placed in the hold mode so that the DAC switching glitches are isolated from the output. The switching transients produced by the SHA are code-independent and occur at the update frequency, hence, they are easily filterable. Although the terms *sample-and-hold* and *track-and-hold* are often used interchangeably, some sample-and-holds have poor track- or sample-mode performance. In order to be used as a DAC deglitcher, the device must function as a true track-and-hold with good track-mode performance.
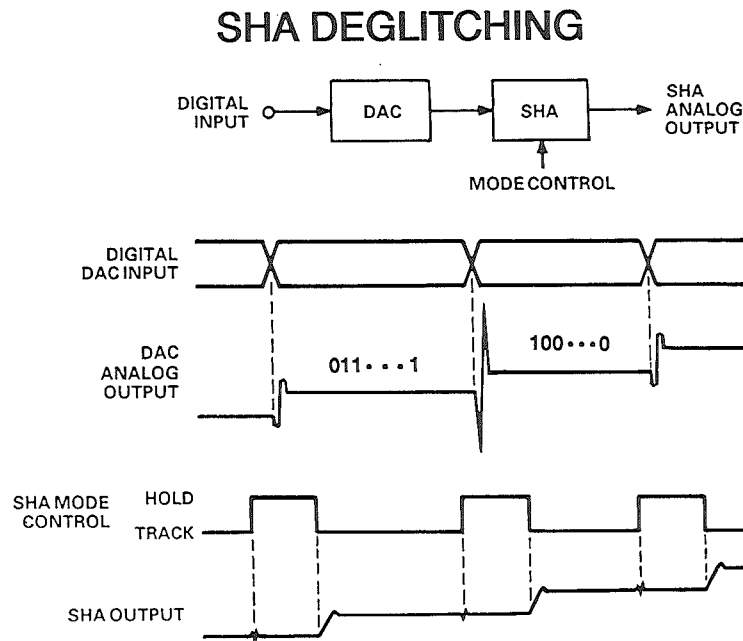
SHA DEGLITCHING

Figure 5.21

A high-performance low-cost SHA deglitcher circuit is shown in Figure 5.22. This circuit will operate with high-speed DACs such as the AD568 and AD668 (12 bit DACs) at update rates up to 10Mhz with harmonic suppression of 70 to 75dB.

A SHA deglitcher suitable for 14 bit performance at 100kSPS is shown connected to the AD7840 14 bit DAC in Figure 5.23. Input frequencies up to 20kHz can be reconstructed while maintaining an SNR of 82dB.
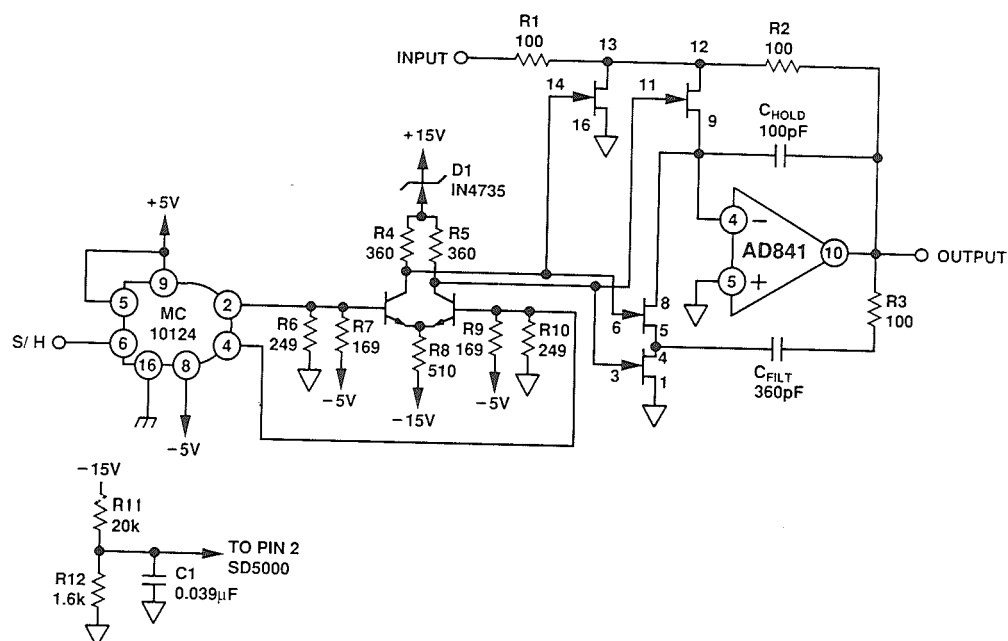
10 MSPS DEGLITCHING CIRCUIT

Figure 5.22

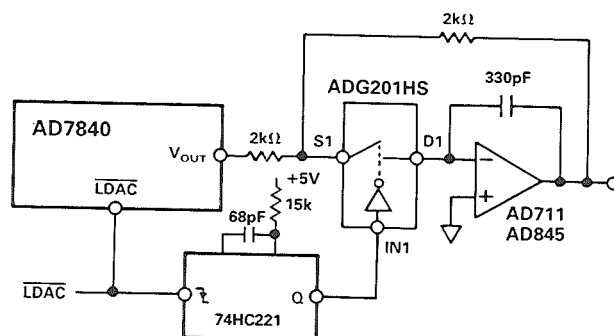# DEGLITCHING A 14-BIT, 100kSPS DAC

Figure 5.23

SUMMARY OF GLITCH REDUCTION TECHNIQUES

- Low Voltage Swings to Drive Switches
- Current-Mode Switching
- Input Latches Directly Before Switches to Reduce Skew
- Segmentation of Higher-Order Bits
- Digital Offset
- SHA Deglitching

Figure 5.24

MULTIPLYING DACs

Virtually all DACs produce an output voltage (or current) which is proportional to the product of a reference voltage (either internal or external to the device) and the digital input word. A multiplying DAC is simply a DAC whose reference voltage can be varied externally over a specified range (see Figure 5.25). This feature can be used in several ways. The DAC can be used as a digital potentiometer (or programmable gain amplifier) which attenuates the signal applied to the reference input terminal proportionally to the digital input word. The ability to digitally control the amplitude of ac signals depends on the bandwidth of the reference voltage input. In order to be useful as a general purpose digital attenuator, the DAC

should be able to operate with a positive, negative, or zero reference voltage. The CMOS DAC architecture of the AD7845 shown in Figure 5.26 allows this flexibility, while some DACs fabricated on bipolar processes typically allow reference voltages of one polarity only, and sometimes values near zero are restricted.

True MDACs constructed on CMOS processes with R-2R ladder networks allow for bipolar reference inputs, and if the DAC is also operated in the bipolar output mode, then true four-quadrant multiplication can be realized as shown in Figure 5.27. Key features of the AD7845 are summarized in Figure 5.28.
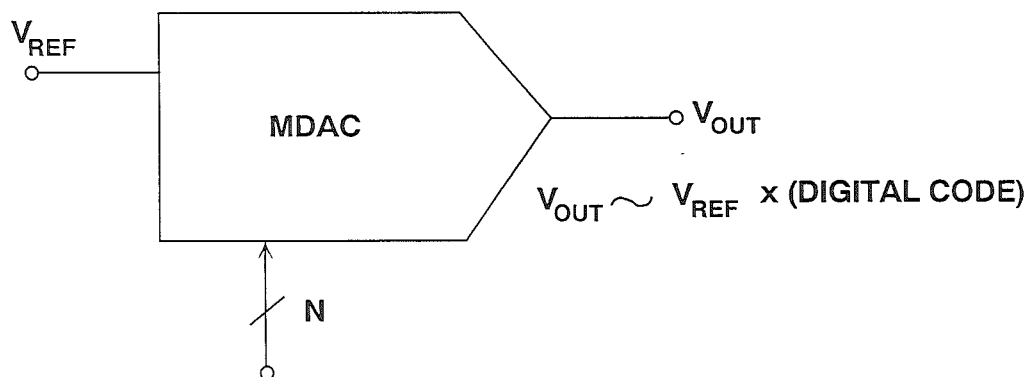
MULTIPLYING DAC

$$V_{OUT} \sim V_{REF} \times (DIGITAL\ CODE)$$

Figure 5.25
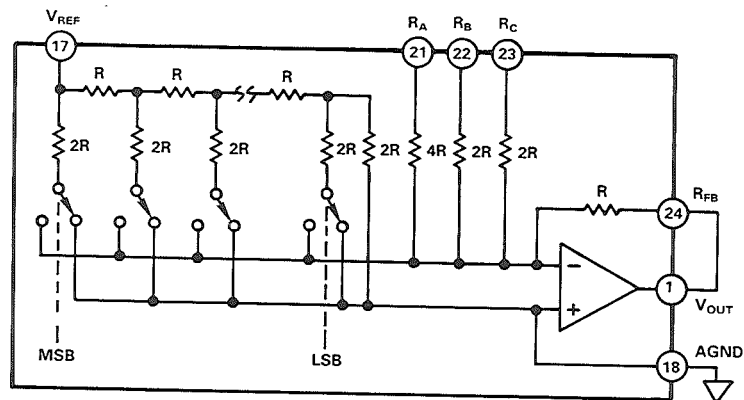
AD7845 12-BIT MULTIPLYING DAC

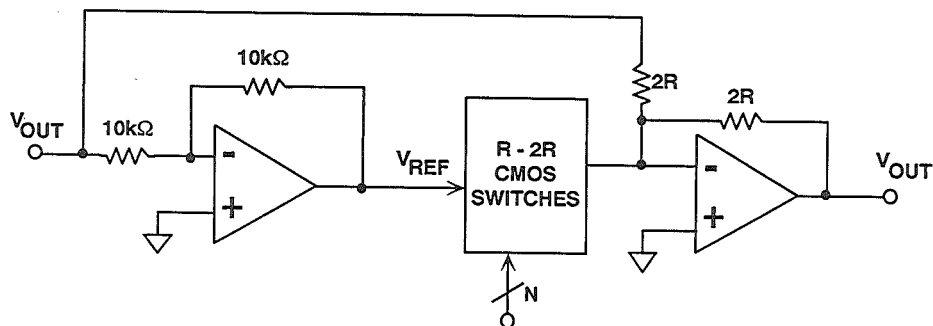Figure 5.26

4-QUADRANT MDAC CONFIGURATION

Figure 5.27

KEY FEATURES OF THE AD7845 12-BIT MDAC

- **12 Bit CMOS MDAC with Output Amplifier**
- **4-Quadrant Multiplication**
- **250kHz Full Power Reference Voltage Bandwidth (20V p-p)**
- **90dB Total Harmonic Distortion for 1kHz 6V rms Sinewave**

Figure 5.28

LOGDACs

A LOGDAC is a multiplying DAC with a gain proportional to the exponential of the digital input. Equal changes of digital input produce equal *ratios* of analog gain change. In other words, the weight of the least significant bit (LSB) is expressed in dB relative to fullscale. A linear DAC can be used to generate a logarithmic attenuation function as shown in Figure 5.29 for a 6-bit DAC. This is accomplished by properly selecting only 7 out of the 64 possible input codes as shown. The proper 6-bit code can thus be specified with a 3-bit code, and a ROM decoder can be used to make the translation. For this example, the weight of the LSB corresponds to 6dB.

A block diagram of the AD7111 8-bit LOGDAC is shown in Figure 5.30. This DAC is a CMOS multiplying DAC which can attenuate an analog input signal over the range 0 to 88.5dB in 0.375dB steps. The circuit consists of a 17-bit R-2R CMOS multiplying DAC with decoding logic which translates the 8-bit binary input word into a 17-bit word which actually drives the internal DAC. An input code of 0 (decimal) corresponds to 0dB attenuation, while an input code of 239 (decimal) corresponds to an attenuation of 88.5dB. For input codes of 240 through 255, the output is zero. Key specifications for the AD7111 LOGDAC are shown in Figure 5.31.
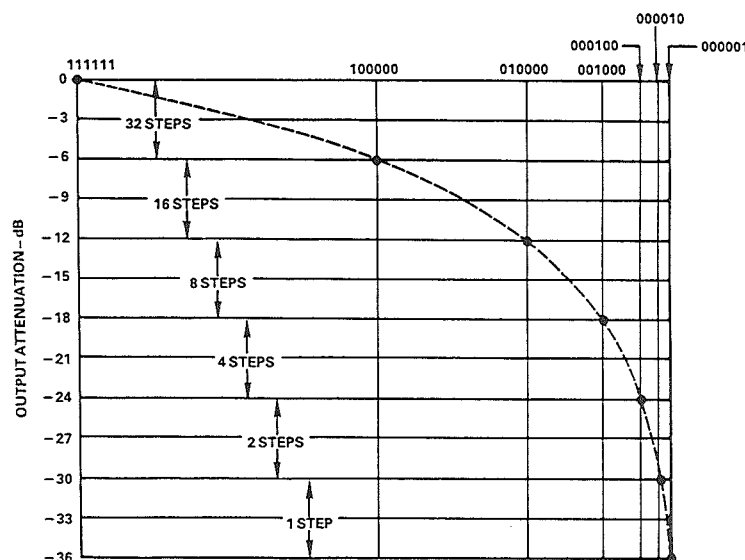
ATTENUATION VERSUS SELECTED INPUT CODES FOR LINEAR 6-BIT MDAC

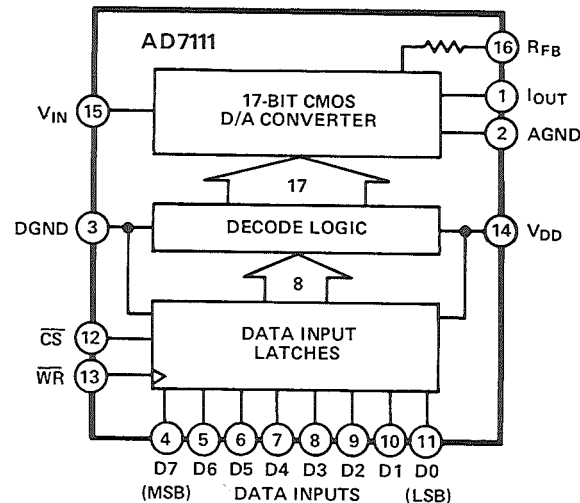
Figure 5.29

AD7111 8-BIT LOGDAC

Figure 5.30

KEY SPECIFICATIONS FOR THE AD7111 LOGDAC

- 88.5dB Dynamic Range
- 0.375dB Resolution, 8-Bit Input, 239 Levels
- 90dB THD for 6V rms 1kHz Input, 0dB Attenuation

Figure 5.31

APPLICATIONS OF MDACs AND LOGDACs

- Digital Attenuators
- Programmable Power Supplies
- Programmable Gain Amplifiers
- Digitally Controlled AGC Systems

Figure 5.32

REFERENCES

1. **High Speed Design Seminar**, Analog Devices, 1990.

2. Phil Burton, **CMOS DAC Application Guide**, 3rd Edition, Analog Devices, 1984.

3. Daniel H. Sheingold, Editor, **Analog-Digital Conversion Handbook**, Prentice-Hall, 1986.

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